SWITCHING POWER SUPPLIES FOR SPECIAL VEHICAL APPLICATIONS

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Abstract: The paper presents switching power supplies with MC34063 and µA78S40 monolithic switching regulator subsystems and DC-DC step-up converter that can be used in special vehicle applications. General description of MC34063 and µA78S40 operation modes, mathematical design and PSpice under ORCAD simulation of the whole switching power supply, a numerical example and the practical implementation are included. Some practical considerations are also presented.

1. INTRODUCTION

The use of switching regulators is becoming more pronounced over that of linear regulators because the size reductions in new equipment designs require greater conversion efficiency. Another major advantage of the switching regulator is that it has increased application flexibility of output voltage. The output can be less than, greater than or of opposite polarity to that of the input voltage.

The MC34063 and µA78S40 monolithic switching regulator subsystems are intended for use and control dc to dc converters. These devices achieves regulation by varying both the on-time and the total switching cycle time (mixed PWM+PFM control) of the output switch Q1, representing a significant advancement in the ease of implementing highly efficient and yet simple switching power supplies [1].

The paper presents switching power supplies with MC34063 and µA78S40 monolithic switching regulator subsystems using a DC-DC step-up converter that makes the output voltage \( V_{\text{out}} \) greater than the input voltage \( V_{\text{in}} \).

2. GENERAL DESCRIPTION OF SWITCHING REGULATOR SUBSYSTEMS

The MC34063 (fig.1a) is a monolithic control circuit containing all active functions required for dc to dc converters regulation. This device contains an internal temperature compensated Reference Regulator that provides 1,25V, comparator Comp, controlled duty cycle oscillator OSC with an active peak current limit circuit, driver \( Q_2 \) and a high current output switch \( Q_1 \). This series was specifically designed to be incorporated in step-up, step-down, step up/down and voltage inverting converter applications. These functions are contained in an 8-pin dual in-line package.

The µA78S40 (fig.1.b) is identical to the MC34063 with addition of an on-board catch diode and an uncommitted operational amplifier. This device is an 16-pin dual in-line package which allows the reference and the noninverting input of the comparator to be pinned-out. These additional features greatly enhance the flexibility of this part and allow the implementation of more sophisticated applications [5].

Fig.1. Functional block diagrams for a) MC34063 and; b) µA78S40 monolithic switching regulator subsystems
3. BRIEF FUNCTIONAL DESCRIPTION OF MC34063 AND µA78S40 OPERATION MODES

The easiest functional description can be given following the typical operation waveforms (fig.2).

![Typical operating waveforms of MC34063 and µA78S40](image)

**Fig.2. Typical operating waveforms of MC34063 and µA78S40**

As long as the output voltage $V_{out}$ is below the nominal level the comparator output presents a Logic „1” at the „B” input of the AND gate. The result is that during the charge time of the external timing capacitor $C_T$ a Logic „1” at the „A” input of the AND gate will be also present. This causes the „Q” output of the latch to go to a Logic „1” enabling the driver $Q_2$ and the output switch $Q_1$. The output voltage increases to it’s nominal level. One can observe in fig.2 that during the discharge time of the external timing capacitor $C_T$ a Logic „0” at the „A” input of the AND gate will be present that causes the „Q” output of the latch to go to a Logic „0” disabling the driver $Q_2$ and the output switch $Q_1$ and the output voltage decreases to and below the nominal output voltage level. The whole functional operation starts again. One can also observe in fig.2 that the nominal level never stay still; it always exists an output ripple voltage $V_{ripple}$. In order to diminish it an output filter for the output voltage must be introduced in the schematics of the switching power supplies with MC34063 and µA78S40 monolithic switching regulator subsystems. Fig.2 also emphasizes a mixed control (PWM+PFM) of the output switch $Q_2$.

4. MATHEMATICAL THEORY OF THE DC-DC STEP-UP CONVERTER CONTROLLED BY MC34063 AND µA78S40

The symbols used in mathematical treatment of dc-dc step-up converter controlled by MC34063 and µA78S40 basic configuration (fig.3) are: $V_{in}$ – input voltage, $V_{out}$ – output voltage, $t_{on}$ – on-time of the output switching transistor $Q_1$, $t_{off}$ – off-time of $Q_1$, $T_0$ – total switching cycle time of $Q_1$, $f_{min}$ – minimum operating frequency, $V_{sat}$ – $V_{CE}$ Saturation voltage, $V_F$ – $V_{AK}$ Saturation voltage drop on diode $D_1$, L- output filter inductor, $I_L$ – inductor current, $C_0$ – output filter capacitor, $I_{pk}$ – peak inductor current, $I_{pk}(switch)$ – peak switch current of $Q_1$, $I_{bg}$ – oscillator charge current, $I_{disch}$ – oscillator discharge current, $V_{ripple}$ – ripple of output voltage $V_{out}$, ESR – Equivalent Series Resistance of $C_0$, $R_L$ – load resistance. Energy is stored in the inductor $L$ during the time that transistor $Q_1$ is in the on-state. Upon the turn-off the energy is transferred in series with $V_{in}$ to the output filter capacitor and load. This configuration allows the output voltage to be set to a greater value than that of the input.

Mathematical theory assumes that:
- the output voltage for dc-dc step-up converter is constant, equal to it’s average value, if it is considered the voltage filter $V_{o}=\infty$;
- the inductor current $I_L$ is linear during the total switching cycle time $T=on+off$;
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- the inductor current $I_L$ is linear during the total switching cycle time $T=on+off$;
- dc-dc step-up converter is operating in the boundary mode, in order to simplify the design.

Choosing the inductor $L$ bigger than it’s value $I_{min}$ obtained in the boundary mode, step-up converter is operating in the correct continuous mode.

The mathematical analysis of circuit in fig.3 follows:

1. The average output voltage for dc-dc step-up converter is known to be [1], [3], [4]:

$$V_{out} = \frac{1}{I-D} \cdot V_{in}$$

2. During $t_{on}$ transistor $Q_1$ inside the MC34063 or µA78S40 is switched on and diode $D_1$ is off being reverse biased by the input voltage $V_{in}$. Kirchhoff’s voltage law applied on circuit in fig.3. during $t_{on}$ gives:

$$V_{in} = L \frac{di}{dt} + V_{sat} \equiv L \left( I_{pk} \right) \frac{d}{dt} + V_{sat}$$
Peak inductor current can be determined from the previous equation:

\[ I_{L(pk)} = \frac{V_{in} - V_{sat}}{L} \cdot t_{on} \]  

(2)

3. During \( t_{off} \) transistor \( Q_1 \) inside the MC34063 or \( \mu A78S40 \) is switched off and diode \( D_1 \) is on because of the magnetic field in the inductor \( L \) that starts to collapse and generates a reverse voltage forward biasing \( D_1 \). Kirchhoff’s voltage law applied in fig.3 gives:

\[ V_{in} = V_F + L \frac{dI_L}{dt} + V_{out} \approx V_F + L \frac{0 - I_{L(pk)}}{t_{off}} - 0 + V_{out} \]

The same peak inductor current can be determined from the previous equation:

\[ I_{L(pk)} = \frac{V_F + V_{out} - V_{in}}{L} \cdot t_{off} \]  

(3)

4. The ration of \( t_{on} \) to \( t_{off} \) is obtained equalizing equations (2) and (3):

\[ \frac{t_{on}}{t_{off}} = \frac{V_F + V_{out} - V_{in}}{V_{in} - V_{sat}} \]  

(4)

5. Assuming the output voltage constant, the net charge per cycle delivered to the output filter capacitor must be zero:

\[ I_{chg\cdot t_{off}} = I_{dischg\cdot t_{on}} \]  

(5)

The peak inductor current can be obtained from equation (5) and dc-dc step-up waveforms:

\[ \frac{I_{L(pk)} \cdot t_{off}}{2} = I_{out\cdot (on + t_{off})} \Rightarrow I_{L(pk)} = 2I_{out\cdot (t_{on\cdot t_{off}} + 1)} \]  

(6)

During the on-time \( t_{on} \) the switch transistor \( Q_1 \) and inductor \( L \) are in series, so the peak inductor current is also equal to the peak switch current:

\[ I_{L(pk)} = I_{pk\cdot (switch)} \]  

(7)

6. From equations (2), (6) and (7) the minimum value of the inductance \( L \) of the dc-dc step-up converter operating in the boundary mode can be determined:

\[ L_{\min} = \frac{V_{in} - V_{sat} - t_{on\cdot max}}{I_{pk\cdot (switch)}} \]  

(8)

7. The ripple output voltage \( V_{ripple(p-p)} \) can be determined knowing \( t_{on\cdot t_{off}} I_{L(pk)} \), \( I_{out} \) and \( C_0 \) and dc-dc step-up switching regulator waveforms:

\[ V_{ripple(p-p)} = \frac{I_{pk\cdot t_{off}} + I_{out\cdot t_{off}}}{2I_{pk\cdot C_0}} \]  

(9)

If an error less than 5% is accepted, it can be accepted a simplified form of relation (9):

\[ V_{ripple(p-p)} = \frac{I_{out}}{C_0} \cdot t_{on} \]  

(10)

Relation (10) allows to approximate the value for the output filter capacitor \( C_0 \), the neglected area between \( t_1 \) and \( t_{on\cdot t_{off}} \) being:

\[ A = (t_{off} - t_1) \cdot I_{out} / 2 \],  

(11)

where \( t_1 \) is defined as the capacitor \( C_0 \) charging interval:

\[ t_f = \frac{I_{pk} - I_{out}}{I_{pk} \cdot I_{off}} \]  

(12)

5. SWITCHING POWER SUPPLIES WITH MC34063 OR \( \mu A78S40 \) AND DC-DC STEP-UP CONVERTER DESIGN EXAMPLE

Given are the following: \( V_{out} = 28V, I_{out} = 175mA, t_{on\min} = 30kHz, V_{in\min} = 12V-25\%, 12V = 9V, V_{ripple(p-p)} = 0.5\% \). Switching power supplies with MC34063 or \( \mu A78S40 \) for dc-dc step-up converters must be designed.

Design example goes as follows:

1. The ratio of switch conduction \( t_{on} \) versus diode conduction \( t_{off} \) time is determined using equation (4):

\[ \frac{t_{on}}{t_{off}} = \frac{\frac{V_{out} + V_F - V_{in\cdot (min)}}{V_{in\cdot (min)}}}{V_{out} - 0.75V} = 2.415 \]  

(13)

2. The cycle time of the LC network can be determined:

\[ T_{(max)} = t_{on\cdot (max)} + t_{off} = \frac{1}{f_{min}} = \frac{1}{30kHz} = 33.3\mu s \]  

(14)

3. From equations (13) and (14) the switching times \( t_{on} \) and \( t_{off} \) are:

\[ t_{on} = \frac{T_{(max)} - t_{off}}{2} = \frac{33.3\mu s - 9.751\mu s}{2} = 9.751\mu s \]  

(15)

4. The ratio \( t_{on\cdot (t_{on} + t_{off})} \) is:

\[ \frac{t_{on}}{T_{(max)}} = \frac{9.751\mu s}{23.58\mu s} = 0.4135 < 6 / 7 = 0.857 \]  

(17)

Note that the ratio \( t_{on\cdot (t_{on} + t_{off})} \) does not exceed the maximum \( 6/7=0.857 \). This maximum is defined by the 6:1 ratio of charge-to-discharge current of timing capacitor \( C_T \) taken from the MC34063 or \( \mu A78S40 \) data sheet electrical characteristics table.

4. The MC34063 or \( \mu A78S40 \) timing capacitor \( C_T \) of the oscillator OSC is charged during \( t_{on} \) at the value \( I_{bg\cdot (min)} = 20\mu A \) and the ripple voltage of \( C_T \) is \( \Delta V_{C_T} = 0.5V \). The value for timing capacitor \( C_T \) is:

\[ C_T = \frac{2.54\mu F}{0.857} \cdot t_{on} = 4.105 \cdot 9.751\mu s = 4.258\mu F \]  

(18)

The standard value \( C_T = 1500PF \) was used.

5. Equation (6) gives the peak switch current:

\[ \frac{I_{pk\cdot (switch)} = 2I_{out\cdot (t_{on} + t_{off})}}{t_{off} + 1} = \frac{2.175mA}{2415s + 1} = 1.195 \]  

(19)

6. Equation (8) gives the minimum value of the inductance \( L \) in the boundary dc-dc step-up converter operation mode:
The value \( L = 170 \mu A > L_{\text{min}} \) was chosen in order to allow dc-dc step-up converter to work in the correct continuous mode.

7. A value for the current limit resistor \( R_{\text{sc}} \) can be determined by using the current level of \( I_{\text{pk(switch)}} \) when \( V_{\text{in}} = 12V \):

\[
I_{\text{pk(switch)}} = \frac{V_{\text{in}} - V_{\text{out}}}{L_{\text{min}} - L_{\text{out(max)}}} = 235 \mu A
\]

The value for the limit resistor \( R_{\text{sc}} \) is:

\[
R_{\text{sc}} = \frac{0.33}{I_{\text{pk(switch)}}} = 0.33 \times \frac{1.632}{160} = 0.2 \Omega
\]

where the voltage drop of 330mV on \( R_{\text{sc}} \) was calculated for \( V_{\text{cc}} = 5V \) and \( I_{\text{dischg}} = 220 \mu A \) using data sheet electrical characteristics table. The standard value \( R = 0.22 \Omega \) was chosen.

8. From equation (10) filter capacitor value is:

\[
C_{0} = \frac{I_{\text{out}}}{V_{\text{ripple(p-p)}}} = \frac{175mA}{140nV_{\text{p-p}}} = 29475 \mu F
\]

Ideally this would satisfy the design goal, however, even a solid state capacitor of this value will have a typical ESR (Equivalent Resistance Series) of 0.3 \( \Omega \) which will contribute 30mV of ripple. In satisfying the example shown, the standard value for the filter capacitor has been settled to \( C_0 = 330 \mu F \).

A tantalum capacitor with ESR of 1.1 \( \Omega \) was chosen, but a supplementary LC output filter with \( L = 1 \mu H \) and \( C = 100 \mu F \) was introduced to keep the output voltage ripple \( V_{\text{ripple(p-p)}} \) to the given value.

9. The given nominal output voltage \( V_{\text{out}} \) is programmed by \( (R_1, R_2) \) resistor divider. The output voltage is:

\[
V_{\text{out}} = V_{\text{ref}} \left( \frac{R_2}{R_1} + 1 \right) = 1.25V \cdot \left( \frac{R_2}{R_1} + 1 \right)
\]

(24)

The divider current can go as low as 100\( \mu A \) without affecting system performance. In selecting a minimum current divider, \( R_1 \) is equal to:

\[
R_1 = 1.25V / 500 \mu A = 2.2k\Omega
\]

(25)

A standard value \( R_1 = 2.2 \Omega \) was chosen. From equations (24) and (25) yields the value for resistor \( R_2 \):

\[
R_2 = R_1 \left( \frac{1.25}{0.5} - 1 \right) = 2.2k\Omega \left( \frac{5}{125} - 1 \right) = 4708 \Omega
\]

(26)

The value \( R_2 = 47k \Omega \) is a standard value, so it was kept.

10. For \( \mu A78S40 \) this step is necessary. In this example with \( V_{\text{in}} = 12V \) the output drive transistor is driven into saturation with a forced gain \( \beta = 20 \).

The required base drive is:

\[
I_B = I_{\text{pk(switch)}} / \beta = 1.195A / 20 = 59.75mA
\]

(27)

Then the driver collector resistor is equal to:

\[
R_{\text{driver}} = \frac{V_{\text{out drive}} - V_{\text{beq}}}{I_B + V_{\text{B E(switch)}} / 170} = \frac{11V - 0.3V - 0.3V}{59.75mA + 0.0017A} = 180 \Omega
\]

(28)

The standard value of \( R_{\text{driver}} = 180 \Omega \) was chosen.

Fig.4. Switching power supply with MC34063 for dc-dc step-up converter

The corresponding circuits for the switching power supplies with MC34063 and \( \mu A78S40 \) used to control dc-dc step-up converter are presented in fig.4 and fig.5. An input capacitor filter of 100\( \mu F \) for MC34063 and of 47\( \mu F \) for \( \mu A78S40 \) was introduced.

Fig.5. Switching power supply with \( \mu A78S40 \) for dc-dc step-up converter

The two circuits are identical as operation mode because \( \mu A78S40 \) is the improved variant for more sophisticated applications of MC34063. It’s internal block diagram has in addition an operational amplifier and a power catch diode (fig.1) and the reference regulator or 1.25V is not internaly connected to the comparator. The conclusion is that for this example it is sufficient to use MC34063 and further analysis focus only on it.

6. PSpICE SIMULATION FOR SWITCHING POWER SUPPLY WITH MC34063

PSpice under ORCAD was used to software verify switching power supply with MC34063 for dc-dc step-
up converter in fig.4. PSpice circuit model [2] for fig.4 is given in fig.6. Subcircuit for MC34063 was included. The most important simulation result is output voltage $V_{\text{out}}$ waveform (fig.7) that proves the stability of witching power supply with MC34063 for dc-dc step-up converter the circuit in fig.4. The average value of $V_{\text{out}}$ is of 28V as it was given in the example and it is reached in 2ms. The output voltage ripple $V_{\text{ripple(p-p)}}$ is around 1V, three times bigger than the given design value 0.5%$V_{\text{out}}=3V$. This bigger value can be explained observing that fig.6 is not totally identical to fig.4 because it doesn’t include the optional suplementary filter that appears in fig.4.

![Fig.6. PSpice circuit model for fig.4](image)

![Fig.7. PSpice simulation waveform of the output voltage $V_{\text{out}}$ on oscilloscope PSC64i](image)

7. PRACTICAL CONSIDERATIONS AND EXPERIMENTAL RESULTS

The design equations for $L_{\text{min}}$ were based upon the assumption that the switching regulator is operating on the onset of continuous conductions with a fixed input voltage, maximum output load current and a minimum charge-current oscillator. Typically the oscillator charge-current will be greater that the specific minimum of 20µA, thus $t_{\text{on}}$ will be somewhat shorter and the actual LC operating frequency will be greater than predicted $f_{\text{min}}$ [6].

The voltage drop developed across the current-limit resistor $R_{\text{sc}}$ was not accounted for in the ratio $t_{\text{on}}/t_{\text{off}}$ and $L_{\text{min}}$ formulas. This voltage drop must be considered when designing high current converters that operate with an input voltage of less than 5V. High frequency circuit layout techniques are imperative with switching regulators. To minimize EMI, all high current loops should be kept as short as possible using heavy copper.
runs. The low current signal and high current switch and output grounds should return on separate paths back to the input filter capacitor. The \( R_1 \) and \( R_3 \) output voltage divider should be located as close to the integrated circuit as possible to eliminate any noise pick-up into the feedback loop [7]. All circuits used permalloy power toroid cores for the magnetics where only the inductance value is given. Input voltage \( V_{\text{in}}=14V \) and output voltage \( V_{\text{out}} \) around 28V waveforms on digital two-channels oscilloscope PSC64i are shown in fig.8. These waveforms are the most important for a switch power supply. Note that \( V_{\text{in}}=14V \) is bigger than the given 12V in the example and the circuit in fig.4 keeps the output voltage \( V_{\text{out}} \) to it’s nominal voltage of 28V still stable. Output power is of 4.9W and conversion efficiency is of 87.7%. Other waveforms are shown in fig.9 and fig.10. Values for \( t_{\text{on}}, t_{\text{off}}, T, \) and \( f \) can be practically verified.

![Fig.8. Input voltage \( V_{\text{in}} \) and output voltage \( V_{\text{out}} \) waveforms on oscilloscope PSC64i](image1)

![Fig.9. Voltage \( V_{CE} \) across switch Q1 waveform](image2)

Fig.10. Voltage \( V_{KA} \) across diode \( D_1 \) waveform

### 8. CONCLUSIONS

The goal of this paper was to obtain simple and complete switching power supplies with MC34063 and \( \mu A78S40 \) monolithic switching regulator subsystems used to control dc-dc step-up converter that can be used in special vehicle applications. The paper included brief introduction, general description and synthetical functional description of switching regulator subsystems and mathematical theory of the dc-dc step-up converter controlled by MC34063 and \( \mu A78S40 \). It also included switching power supplies with MC34063 or \( \mu A78S40 \) and dc-dc step-up converter design example with it’s PSpice under ORCAD modelling and simulation, practical considerations and experimental results.

For MC34063 numerical example, output voltage was of 4.9W and conversion efficiency of 87.7%

Mathematical theory fits with the simulation and experimental results.

### REFERENCES


Interpolation procedure with jitter of Gaussian process at the output of the time varying system

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Abstract: We consider a non stationary Gaussian process formed at the output of a time varying system driven by white noise. The system is the usual RC integrated circuit. The main parameter of this system has a harmonic change. On the basis of the conditional mean rule we analyze Sampling Reconstruction Procedure (SRP) with jitter of the output process. The model of jitter is described by the beta distribution. The reconstruction algorithm is the interpolation. We obtain one of the principal SRP characteristics the error reconstruction function, when the reconstruction function is optimal.

Keywords: jitter, parametric system, reconstruction error, sampling reconstruction

1 Introduction.

There are two waves of the interest to SRP with jitter of random processes. Some first papers have been published in sixty years (see, for instance, [1, 2]). The second wave is characterized by the papers (see, for instance [3-5]). The mentioned papers have some drawbacks, namely: 1) there is no any information about a probability density function (pdf), 2) the quantity of samples is equal to infinity, 3) the jitter effects is the same for all samples, 4) it is impossible to use the applied methods for nonstationary processes.

The Sampling Reconstruction Procedure (SRP) has an special interest in the field of the communications, inside this process the “basic function” plays a fundamental role, however, it is clear that it is not the same thing to reconstruct a deterministic signal than a random signal, and more even, a non stationary signal.

The main objective is to obtain the expressions that define the reconstruction error, the basic function, and the reconstruction function of the process at the output of an RC filter in the interpolation regime when the process is affected by the jitter presence, with the purpose of to evaluate and to compare with the results obtained in [6], where the jitter presence does not exist. Another objective is to demonstrate that the mathematical expectation rule has many advantages and that is a powerful tool to analyze stochastic processes on several scenarios in an easy way.

2 General Expressions

The methodology used for the SRP description is based on the mathematical expectation rule, for what it will be necessary to carry out a brief explanation of the rule in order to understand the used expressions. This rule assures the evaluation of the random variable with the minimum error. Following this rule, it is possible to use the function of the conditional average \( \tilde{m}(t) \) [6] as a reconstruction function. Then the conditional variance \( \tilde{\sigma}^2(t) \) characterizes the error reconstruction function. The main characteristics of the SRP \( \tilde{m}(t) \) and \( \tilde{\sigma}^2(t) \) can be calculated in an easier way for the Gaussian processes. We can consider the general case of a non stationary Gaussian process \( y(t) \) with the mathematical expectation \( m(t) \), the variance \( \sigma^2(t) \) and the covariance function \( K(t_1,t_2) \). This is the complete information about the given process. From here one can write the exact expression of the multidimensional probability density function (pdf) of an arbitrary \( m \) order:

\[
\begin{align*}
    w_m[y(t_1),\ldots,y(t_m)] &= (2\pi)^{m/2} \left| \det K(t_{ij}) \right|^{1/2} \\
    &\times \exp \left\{ -\frac{1}{2} \sum_{i=1}^{m} \sum_{j=1}^{m} [y(t_i) - m(t_i)] a_{ij} [y(t_j) - m(t_j)] \right\}. 
\end{align*}
\]

where \( \det K(t_{ij}) \) is the determinant of the covariance matrix: