# A Novel Design Method of Time-Interleaved Subranging ADC

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*Abstract: - A novel design method of time-interleaved subranging ADC is presented. We use the bisection method to let only half of the comparators in typical subranging ADC to work in every clock cycle. Thus, we are able to reduce the number of comparators by half. It is possible to reduce the die size. An example of a 8-bit time-interleaved subranging ADC operates at 40MHz sampling rate and 1.8V supply voltage is demonstrated. The power consumption of the proposed circuit is only 10mV with SPECTRE simulation. The physizical measurement of the Time-Interleaved Subranging ADC and the ordinary Subranging ADC is compared using layout. It is shown that the bisection method is able to reduce up to 40% in die size.*

*Key-Words: - SHA, Coarse ADC, Fine ADC, Resister String, Control Switch, Timing*

## 1 Introduction

Recently High speed ADC (Analog-to-Digital Converter) keep using and raising it in a plenty of devices such as telecommunications, video and digital communication applications. Therefore, we require more high speed data converters fabricated such as these systems are going to be more high speed and larger than before. The flash ADC was a general way for high speed data conversion in a few years ago. However, Owing to the power consumption and die size are increased exponentially as the resolution, it is preferred an advanced way such as subranging, pipeline, folding-interpolate and time-interleaved ADC.[1-2] In case of the subranging ADC, a setting time of reference voltage in FADC(Fine ADC) is the best consideration for performance of whole system even though it has some advantages which are power consumption and die size of the flash ADC.[1,2,4] In another case of time-interleaved, it has a advantage which is able to materialize high speed system with lower speed though it has some disadvantages such as not an easy to design due to nonlinearity in mismatch between those channels, more increasing the number of channel is more increasing the power consumption and channel size as being made up several channels in parallel architecture.[2-5]

This paper proposes that as adding a way of time-interleaved in subranging system, it is able to reduce the number of comparators by half. Therefore, it is possible to decrease die size. Hence, there is a drawback which is a decreasing data conversion speed by half. [1] For the confirmation of those features, we design by an 8-bit time-interleaved subranging ADC which operates at 40MHz sampling rate in TSMC 0.18-μm, 1P6M CMOS Technology.

## 2 Architecture

### 2.1 A typical subranging ADC architecture

The block diagram of the typical 8-bit subranging ADC architecture is illustrated in Fig.1. First of all, the analog input signal is sampled by SHA (Sample and Hold Amplifier) and then the output signal of SHA is an input signal in CADC (Coarse ADC). Calculating with a 16-bit thermal code of RS(Resister string), the CADC is able to get a 4-bit MSB(Most Significant Bit) which can be an input signal of FADC(Fine ADC) for calculating the rest of another 4-bit which is called a LSB(Least Significant Bit). During the FADC is being calculated the 4-bit LSB, the CADC is holding the 4-bit MSB. After the FADC is done, it is gotten a result of 8-bit output signal at the same time.

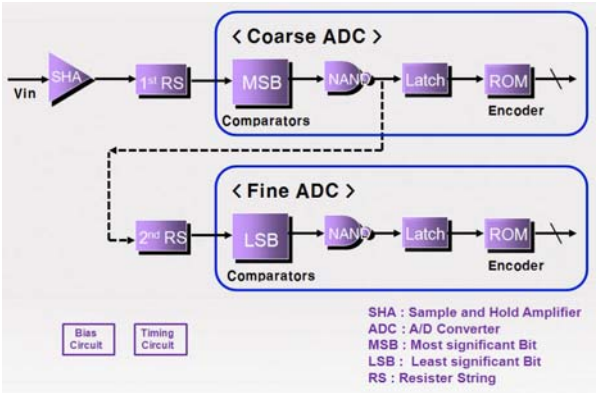


Fig.1 A typical subranging ADC architecture

### 2.2 A proposed subranging ADC architecture

The block diagram of the proposed 8-bit subranging ADC architecture is illustrated in Fig.2 The biggest

specific feature of this architecture is that there are no existing comparators in FADC. Instead of that, there is a Control Switch (CS) which is able to be interleaving time of comparators between CADC and FADC. It means that CS control that interleaving time so it works comparators of both CADC and FADC by using time gap.
The operating system is similar as typical subranging ADC, but there is a huge different thing is that the 4-bit LSB is calculated through same comparators in CADC while being held the 4-bit MSB in latch in CADC so that is possible to be made up half of comparators than before what it is made up.

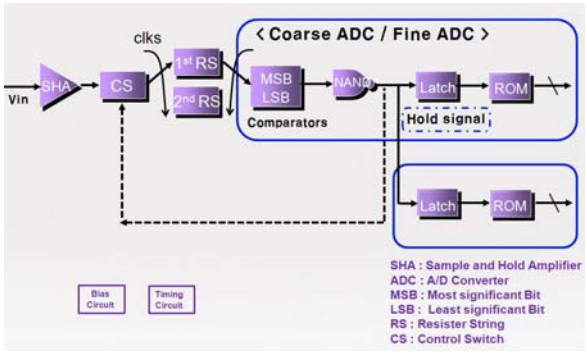


Fig.2 A proposed Subranging ADC architecture

## 3 A way of channel time-interleaved

In case of N-bit, since a typical subranging ADC is made up $2^{1+(n/2)}$ -1 comparators, which results in a big chip die, a large amount of power is consumed. However, a proposed time-interleaved subranging ADC which is made up $2^{n/2}$-1 comparators will decrease the number of comparators by half, compared to the typical one. This brings forth to a positive result, as the chip die is now smaller and hence less power is consumed.

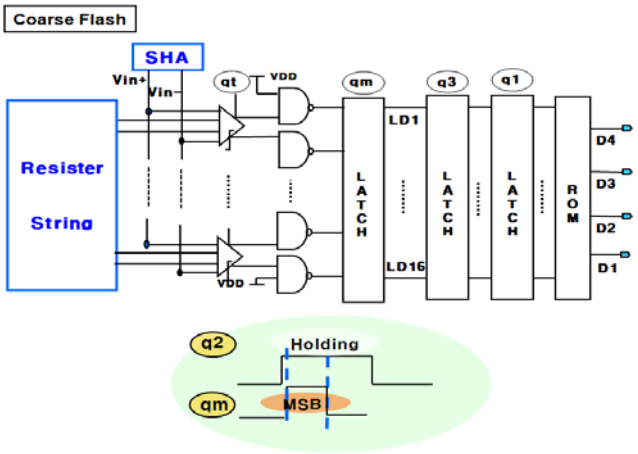


Fig.3 (a) Coarse ADC block diagram

The block diagram of a way of channel time-interleaved is illustrated in Fig.3. Generating half signal, which we called a QM, controls comparators of CADC from holding signal which is a Q2 so that it receives the 4-bit MSB. The other half signal from Q2 is a QMB which controls same comparators in CADC that were used before. It means that although this input signal is calculated through same comparators in CADC, it works for the 4-bit LSB in QMB. And then the 4-bit LSB is held on latch in FADC. After the FADC is calculated, it is possible to receive whole 8-bit output signal at the same clock. Eventually, as channel time-interleaved, we are able to bisect to work same comparators in two times every each clock.

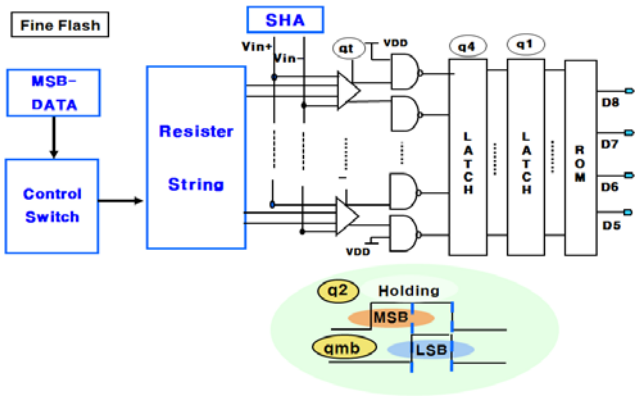


Fig.3 (b) Fine ADC block diagram

## 4 Design of Each Detailed Circuit

### 4.1 Control Switch and Resister String

The Control Switch and Resister String are one of the most important circuits in proposed subranging ADC. The CS and RS are illustrated in Fig.4. It receives the 4-bit MSB after the CADC is calculated in QM, and then this 4-bit MSB, which we called MD1-MD16, is being held on latch in the CADC. This signal is simultaneously an input signal for the second switch group of RS which generates a new reference voltage for the FADC when the latter is calculated in QMB.

The input signal makes switches to the first group of RS, closing it, so that it receives MD1-MD16 in QM in CADC. At the same time, the second group of RS opens, which means that it doesn't work in QM. For instance, if it receives MD1 from CADC, while MD1 is being held on latch in CADC, this signal will make switches to the second group of RS, closing it, simultaneously opening the first group of RS, which means that the latter doesn't work in QMB. If it receives LD1, these signals will work for second group of RS.

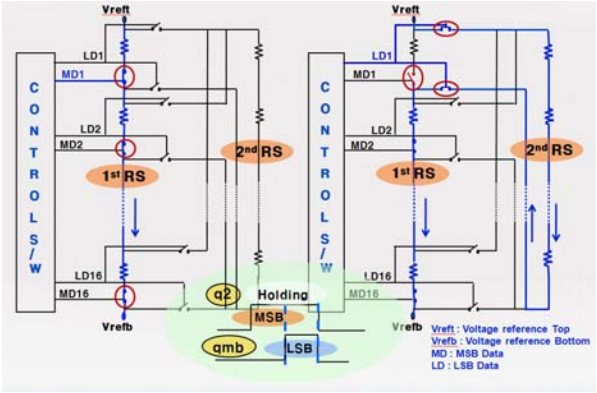


Fig.4 Control Switch and Resister String

### 4.2 Timing

Timing bisected by one signal, which is allowed at the first, controls whole circuit. The timing is illustrated in Fig.5. The QM and QMB are generated through a half-divider by QT, which is allowed at first. Then Q3 is generated by merging Q2 with QM. Likewise, Q4 is generated by merging Q2 with QMB. Moreover, the Q2 and Q1 are generated through a quarter -divider by QT, which controls for comparators. Furthermore, QM and QMB control for RS. Moreover, Q3 and Q4 control for latch. Lastly, Q1and Q2 control for SHA.

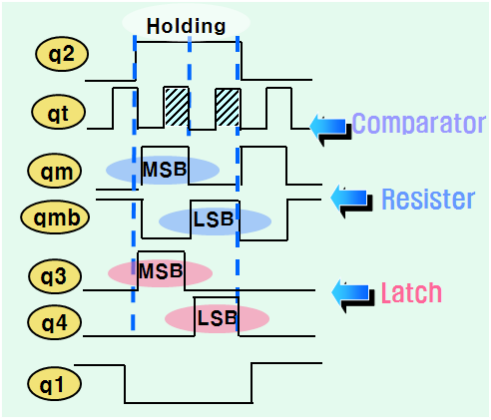


Fig.5 Timing

### 4.3 Latch

Latch is another significant circuit in this proposed subranging ADC. After FADC is done, due to the reception of the whole signal at the same clock, the timing on latch is more significant than other circuits. There are 3 of latch blocks in CADC and there are 2 of latch blocks in FADC. In case of CADC, owing to the holding signal while the FADC is being calculated as I mention it before, so then it is essential that one more latch block needs on CADC than FADC's. First of all, the first latch is holding signal in Q3 in CADC while the FADC is being calculated. Secondly, the first latch in FADC is holding a signal when the calculated FADC is done in Q4. Simultaneously, the signal which is held in first latch is moved into the second latch in Q2 in CADC. After that, both signals in CADC and FADC move at once into next latch block in Q1. After that, both signals move into ROM which means an encoder. At the end, it receives a whole 8-bit output result signal in a same clock.

## 5 Simulations and Layout

The proposed subranging is reliably designed with consideration for variation, supply voltage which is given in process. We want to find some problems which we don't expect about system or etc before. It is simulated by SPECTRE with TSMC 0.18-μm, 1P6M CMOS technology. The result of simulation is illustrated Fig.6. It is the same as we have already expected it before. Thus, it means the whole circuit doesn't have any problems to run in system.

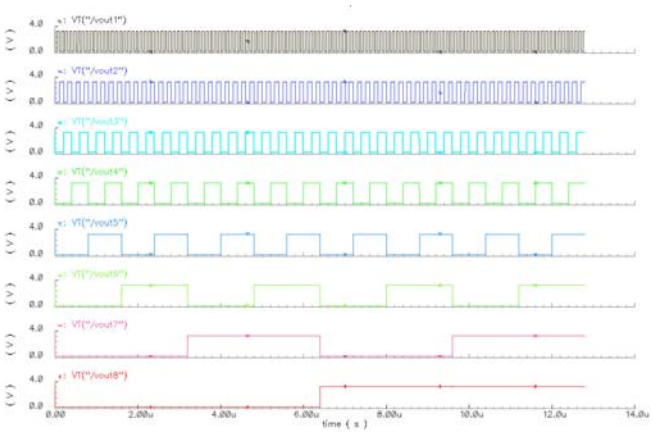

Fig.6 A result of Simulation

Table.1 shows a comparison between typical subranging ADC and proposed subranging ADC.

| | A typical Subranging | A proposed Subranging |
|---|---|---|
| Total comparators | 31 ($2^{N-1}$) | 15 ($2^{N/2-1}$) |
| Clock Cycles / Conversion | 1 | 2 |
| Relative Die Size | 1 | 0.6 |

Table.1 A comparison between typical subranging ADC and proposed subranging ADC

The layout is illustrated Fig.7. The layout which is in TSMC 0.18-μm, 1.8V CMOS technology is illustrated Fig 7. The chip die is 1.7×1.3 $mm^2$.

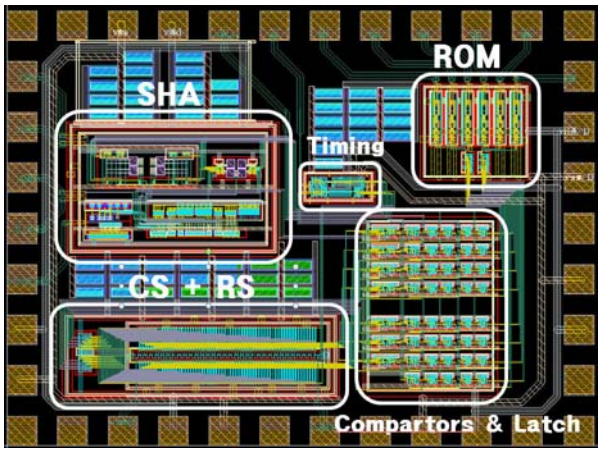


Fig.7 Chip die

## 6 Conclusion

This paper proposes that as adding a way of time-interleaved in subranging system, as reducing the number of comparators by half, it is possible to reduce the die size. For the confirmation of those features, we design by an 8-bit time-interleaved subranging ADC which operates at 40MHz sampling rate in TSMC 0.18-μm, 1P6M CMOS Technology. The power consumption of the proposed circuit is only 10mV with SPECTRE simulation. The physizical measurement of the Time-Interleaved Subranging ADC and the ordinary Subranging ADC is compared using layout. It is shown that the bisection method is able to reduce up to 40% in die size. Indeed, we demonstrate those features by simulation. Therefore, we are going to confirm these features after the chip comes out.

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