A Clock generator using Voltage Regulated VCO

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Abstract: - A clock generator using PLL with ring VCO is described in this paper. The circuit consists of voltage regulated VCO as a clock-distributor for quard phase and uses in receiver state. Total circuit was designed for fabrication using 0.18um 1P6M CMOS proces and tested for 850MHz quard-phase PLL output results.

Key-Words: - PLL(Phase looked loop), PFD(Phase freguency detector), Charge Pump, Loop filter, Regulated VCO(voltage control oscillator)

1 Introduction

In high speed communication system for transmission of data, PLL is supposed to use for restoration of data and system-clock.
If Jitter increases in the clock generator, it can be the cause which falls the capacity of high speed communication system. Especially, Jitter which is caused by power-noise can be the cause which can make some loss during the transmission of data, and it can make the speed slower because of the clock-skew in the high-speed system. Of blocks which compose PLL, the circuit which has the most important influence is VCO. In VCO which use system-power as its power source, the influence of the its power source's noise affects the out-put Jitter quite much and then it makes the quality of the clock lower.[1][2][3]
This report indicates that VCO has to be seperated from the system power to reduce the out-put Jitter because of its power source's noise, to supply VCO's stable power by designing the constant voltage generator and PLL Jitter will decrease as improving the power-noise's quality. [4][5] In this report, it's based on the result of the experimentation through our project we processed.

2 Problem Formulation

2.1 Clock generator's whole block

In fig1, it shows the Clock generator's role approximately which we express in this report. The Clock generator of the reception part can offer 850MHz which has 4 phases which is based on 340MHz to each channel of the reception part.

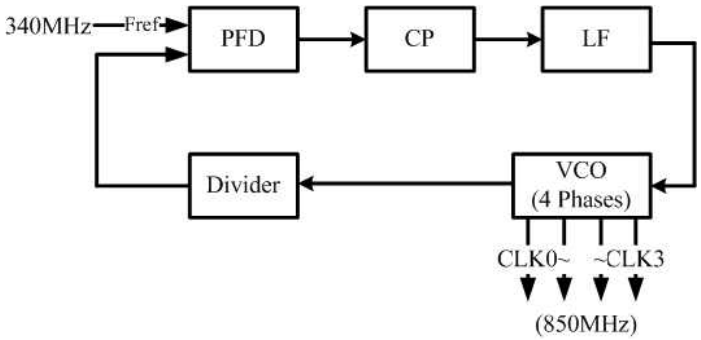

fig 1. Clock generator's Top block

2.2 Phase Frequency Detector

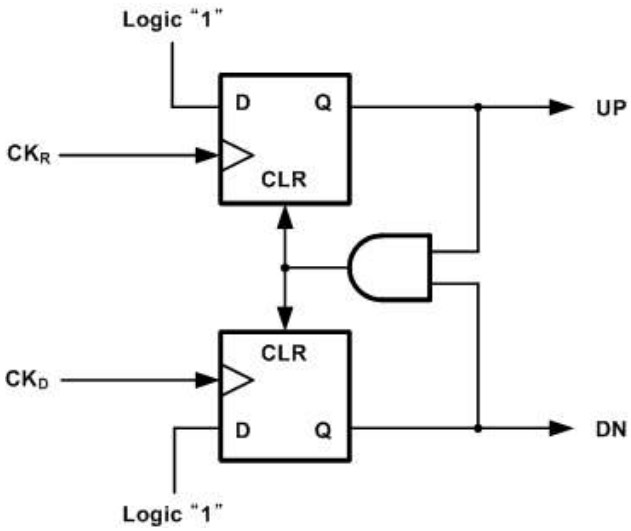

fig 2. Frequency Phase Detector

The phase frequency detector which we used in this report is combined with TSPC type's D Flip-Flop and one AND Gate.
When CLR is 'low', Flip-Flop's output has stable value which had once before if CKR and CKD which is from divider are 'low'. At this moment, the standard Clock signal is 'high', UP signal will output 'high' and there is no change in DN signal. Otherwise, if the Clock signal is 'high' which is from the division part, DN signal will be 'high' and there is no change in UP signal. AND if UP and DN signals are 'high', we make UP and DN signal 'low' by making CLR signal 'high' as the gate's delay.

2.3 Charge Pump

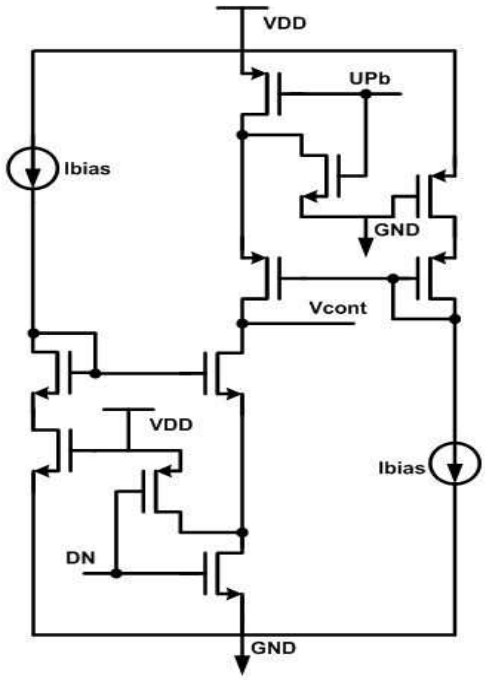

fig 3. Charge Pump

In fig 3, its electric-charge pump is a system of source-switch. The source-switch electric-charge pump means that the switch is located in the electric current-mirror's source. Because of this location, the parasitism capacitance is low, and because it is located in the low impedance node, switching movement can be fast. Thanks to the fast switching movement, high frequency movement can be easy.
Furthermore, if we can make bias electric current low, power consumption will be low. And because the switch is not located in the electric-charge pump's output node directly, it is not interrupting too much by putting into the electric-charge or even the Clock feed through. And the switch is closed, any peak electric current which is due to turn-on resistance doesn't occur because the electric current-mirror's transistor will go into from interception part to saturation part.

2.4 Loop Filter

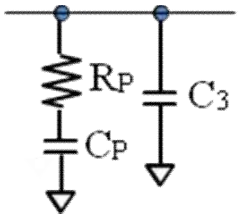

fig 4. Loop Filter

In fig 5 shows Loop Filter. The loop filter changes an electric current which is from the electric-charge pump to a voltage after receiving it as an input. Its voltage will be VCO's control voltage. To ensure phase margin, we used the loop filter which has 2 organization and we realized it from the outside chip.

2.5 Voltage Control Oscillator

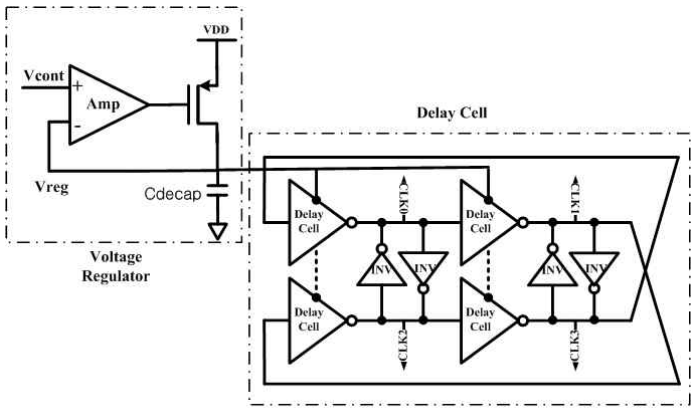

fig 5. Voltage Control Oscillator

In fig 5, it's a construction of the constant voltage and Delay Cell of Vcont is not connected to Vreg directly but it operates through the Op-Amp.
Therefore, we can reduce the effect which is related with the oscillator from outside noise because we can offer more stable power-source by offering outside power-source to the oscillator independently. Cdecap offers dominant pole as far as it doesn't affect PLL's zone(bandwidth of PLL) and we can reduce the power-resource noise's effect because the power-supply sensitivity will be low as the size is getting bigger. And then we proceeded Delay Cell which is formed by inverter as a voltage-control type which is related with the output of Vcont.

3 Chip Test

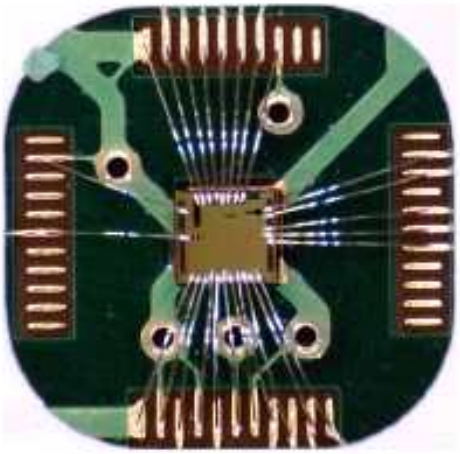

fig 6. Test Chip

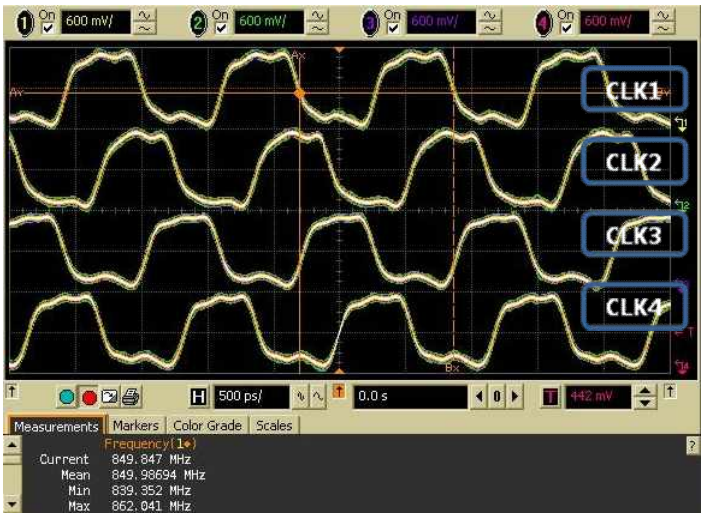

fig 7. Test Result

fig 8. Clock Jitter

In fig 6 shows Test Chip. fig 7 shows our final result and we can check output signal of 850MHz. fig 8 shows Clock's Jitter which is from the final output. As this result, we could affirm that Clock's p-p Jitter was about 16ps and rms Jitter was about 2ps.

4 Conclusion

In this report, we offered independent power-source to VCO by using a regulator in order to lose the effect of power-source's noise.
In view of the result from the experimentation of the chip, it showed that each of the Clock generator's phase difference was established and the maximum Clock's p-p Jitter was about 16ps, rms was about 2ps. We didn't consider each output's matching too much because it depends on the whole system. From now on, we consider that we may be able to apply the original Clock generator which we proceeded first to the whole system of the reception part.

References:

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