Clock and Date Recovery Circuit Using 1/4-rate Phase Picking Detector

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Abstract—This work is designed of clock and data recovery circuit using system clock generator. This circuit is composed by PLL(Phase Locked Loop) to make system clock and data recovery circuit. The data recovery circuit using 1/4-rate phase picking Detector helps to reduce clock frequency. It is advantageous for high speed PLL. It can achieve p-p 88ps jitter operation. The designed CDR(Clock and data recovery) has been fabricated in a standard 0.18um 1P6M CMOS technology and an active area 1x1mm.

Key-Words: - CDR, 1/4-ratePD, Phase Picking, Low jitter

1. Introduction

High speed interface is required by present systems because data transmission speed and semiconductor technology are developed. Not only transmission between systems, but transmission between chips is demanding high speed bandwidth of data. General system use parallel transmission for overcoming low bandwidth. But that method is generated distortion and skew of data. And system cost is increased due to adding channels. To solve trouble of parallel transmission, serial link that changes parallel to serial in transmitter send to receiver using channel. And then receiver recovers serial data sent through channel. In the serial link system, CDR circuit of receiver recover clock and data from distorted random NRZ(Non Return to Zero) data.

PD(Phase Detector) in CDR circuit of receiver is the block that detect and recover data change. It is different to 3-state PFD(Phase Frequency Detector) in PLL. So PD in CDR circuit apply to PDs as Hogge and Alexander and FD(Frequency Detector).[1] General use oversampling type PD due to that PDs is difficult applying to high speed system. PDs using oversample method are phase picking type that select fitting phase from multi phase sampling and phase tracking that select fitting phase from tracking phase of data.[2] And jitter characteristic of CDR using phase picking type PD is better than CDR using phase tracking type PD. But CDR circuit applied by input data rate as full-rate and half-rate has limitation of speed and high power consumption of system including VCO.[3]

This work is designed of CDR circuit using 1/4-rate oversampling type PD. So VCO output frequency in CDR circuit is reduced. And jitter characteristic of CDR is reduced due to using phase picking type PD.

2. Architecture of CDR

Fig. 1 is architecture of clock and data recovery circuit. CDR is divided into two main blocks : PLL and DR(Data recovery). Reference clock is required on main system. PLL generates reference clock of main system. Based on DLL(Delay Locked Loop), DR receives clock need to 1/4-rate PD from PLL. VCDL(Voltage controlled Delay Line) of DR is controlled by 1/4-rate output signal. If phase difference between data and clock from PLL is occurred, signal of 1/4-rate PD output is sent to CP(Charge Pump) to control delay of VCDL. 1/4-rate PD not only detect phase, but also recovers data and divides data to parallel.

PLL is composed by PFD(Phase Frequency Detector), CP(Charge Pump), LPF(Loop Filter), VCO(Voltage controlled Oscillator) and Divider. VCO is ring type to make 8 phase multi clock.
Data Recovery Circuit is composed 1/4-rate PD, CP, LPF and VCDL.

1/4-rate PD is oversampling type. 1/4-rate PD samples input data to use 8 phase multi clock and then detects toggle of data. Phase information is analyzed by detected data. 1/4-rate PD prints UP and DN signals by analyzed phase information. Printed 2 signals are changed to value to control delay of VCDL in CP. So, data is matched with clocks of PLL. When data is matched with clocks of PLL, data is recovered by data picking type.

### 3. Design of detail circuit

#### 3.1 1/4-rate Phase Detector

8 phase multi clocks of PLL are used to reference clocks on 1/4-rate PD. 8 phase multi clocks are needed in 1/4-rate PD because PD is oversample type.

**Fig. 2** Detecting conditions of 1/4-rate PD.

Fig. 2 is detecting conditions of 1/4 rate PD. Data processes oversampling by clocks of PLL like Fig. 2. Locked case, each data are printed on clk45, clk135, clk225 and clk315. If transition section of data is between clk0 and clk45, 1/4-rate PD is printed Pup signal. So delay of VCDL is reduced. And If transition section of data is between clk45 and clk90, 1/4-rate PD is printed Pdn signal. So delay of VCDL is induced.

**Fig. 3** Outputs of 1/4-rate PD.

On Fig. 3, inputs and outputs of 1/4-rate PD in the locked case is shown.

**Fig. 4** Architecture of 1/4-rate PD.

Fig. 4 is architecture of 1/4-rate PD. Architecture of 1/4-rate PD is implemented in based Fig. 3.
3.2 Voltage Controlled Delay Line.

![Fig. 5 Voltage controlled delay line](image)

Fig. 5 is architecture of VCDL. Power voltage of VCDL is controlled by voltage which is received from LPF. If controlled voltage is increasingly high, delay of VCDL is increased. If controlled voltage is increasingly low, delay of VCDL is decreased. And it is input of PD that data is passed through delay line based inverter.

### 3.3 Voltage Controlled Oscillator

In the PLL, to make 8 phase multi clocks, VCO type of ring is used. VCO is composed of 3 main parts: bias, delay cells and buffer. Bias supplies current to delay cells. Frequency of VCO is controlled by delay cells. To be made to full swing, buffers are needed in VCO.

![Fig. 6. Architecture of Voltage controlled oscillator](image)

Bias circuit is designed by rail-to-rail type that is oscillated from gnd to vdd. [4] Delay cells is designed by ratch type. In this CDR circuit, full swing is needed more than duty-cycle. So full swing generator is added in buffer of VCO.

### 4. Layout and Test

![Fig. 7 Total clock and data recovery circuit layout](image)

Fig. 7 is Total clock and data recovery circuit layout that is used by CMOS 0.18um 1P-6M technology. Chip size is 1mm x 1mm. And LPF is designed out of chip.

![Fig. 8 Test of recovered clock jitter](image)
Fig. 9 Eye diagram of recovered data

Fig. 8 is test of Recovered clock jitter. Measured jitter of clock is p-p 88ps. Recovered clock frequency is 640MHz. Fig. 9 is eye diagram of recovered data. It is important that clock jitter of PLL in this CDR circuit. If PLL clock jitter is high, recovered clock jitter also is high.

4. Conclusion

In this paper, CDR circuit that receive clock from PLL and recover data is designed by CMOS 0.18um 1P-6M technology. By using 1/4-rate PD, it is faster operation and lower power consumption than 1-rate and 2-rate CDR.

In this CDR, input data at 2.56Gbps is recovered to output at 640Mbps. Recovered data jitter is p-p 88ps and chip size is 1mm x 1mm.

References: