A practical modelling for the design of a sigma delta class D power switching amplifier and its pedagogical application

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Abstract: The class D amplifier is now well known in audio applications. Its excellent power ratio (greater than 90%) is the most important advantage. The MOS transistors switching power stage is able to drive a useful power up to 100W to the loud speaker. However, designing such an amplifier is more difficult than designing a classical class A or AB power amplifier. As a global and simple analysis is rarely found in the scientific literature, a simple method is presented here based on a simplified modelling, to design a sigma delta class D power switching amplifier as easily as possible. The experimental results are given to illustrate the design method. Finally, we explain how we exported this work towards pedagogical application and practical lessons for our engineer students.

Keywords: Power electronic, circuit modelling and design, class D, sigma delta modulation, pedagogical approach

1. Introduction

1.1 Generalities

1.1.1 Class D basics

The Class D amplification [1] uses MOS power transistors in switching mode [2]. It is able to obtain a power ratio close to 95%. It is then possible to reduce the size and thereby to miniaturize the audio amplifier. The principle is given in figure 1 [3], [4]. The audio signal is converted in a Pulse Width Modulated intermediate signal or Sigma delta modulated signal. This two level signal drives a full bridge MOS power transistor which works in switching mode. Free running diodes are not shown in figure 1. The power supply over 30V enables it to carry a high current in the load. A low pass output filter between the MOS stage and the speaker restores the audio signal. And the feed back active network set the voltage gain of the circuit.

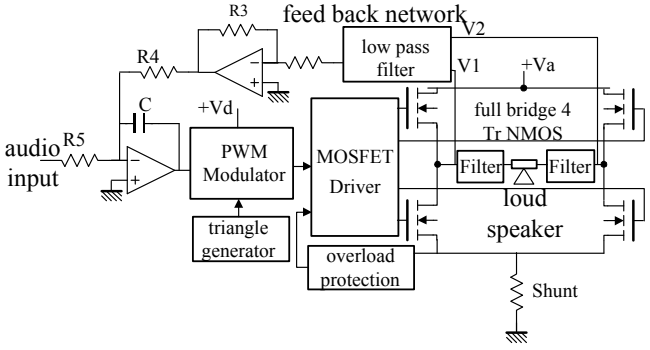

Fig.1: Class D PWM amplifier block diagram

1.1.2 Principle of Pulse width modulation (PWM)

The analogue signal is compared to a high frequency triangular waveform. The output is a two level pulsed signal as shown in figure 2.

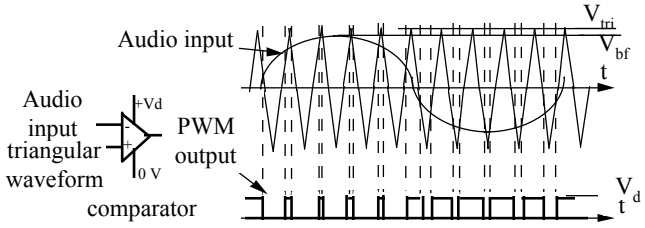

Fig 2: PWM modulation

1.1.3 Principle of the Sigma delta modulator

The sigma delta modulator generates at its output, a digital serial pulse signal, similar to the analogical PWM, but the width of the impulses, by the principle, is sampled and multiple of the period of the clock ($1/F_e$). (Cf. figure 3b)

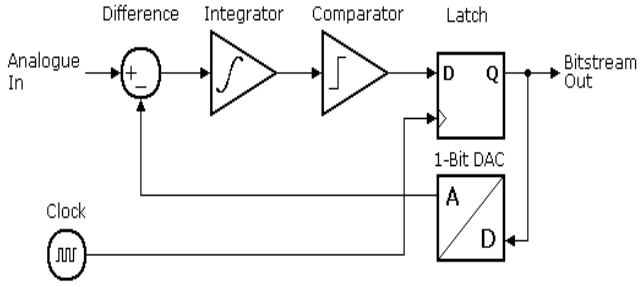

Fig 3a: First order Sigma delta analogue modulation

The figure 3b shows the modulated signal spectrum. This one contains the useful LF frequency of the input signal (which interests us for the later reconstitution of the signal). It contains also a series of lobes (looks like the spectrum of a "pseudo random" bits stream clocked by a clock at F_e) with cancellations all the $n.1/T_e$ (related to sampling by the D latch) and a null DC value.

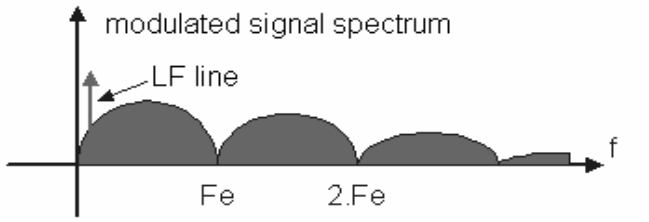

Fig 3b: Sigma delta spectrum waveform

At the maximum modulation rate, the maximum value of the LF frequency line V_{max} will be:
$V_{max} = 0.5.V_d$, like for PWM modulation, where V_d is supply voltage of the D latch [4].

1.1.4 Sigma delta modulator versus PWM

In the sigma delta version, the PWM stage is replaced by a sigma delta modulator as indicated in figure 4.

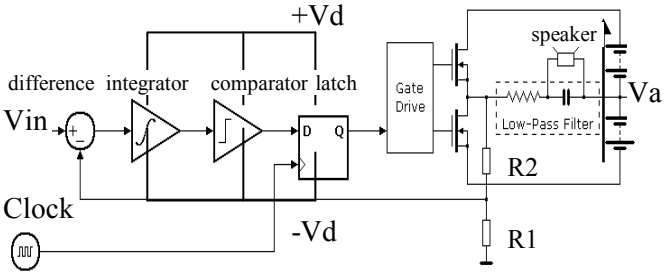

Fig 4: Half bridge first order sigma delta Class D amplifier

Each of the two versions has its own advantages and inconvenient: Sigma delta modulation can be built with analogue circuits or fully synthesised in digital circuit such as FPGA but there is inherent quantification noise due to the sampling. In the two cases the clock frequency must be at least 10 times the maximum frequency of the input signal.

1.1.5 Commercial circuits state of art

Many Integrated class D amplifiers are now available for commercial uses [6], [7] such as automobile radio receivers. Philips, National semiconductor, Texas Instrument, Analog Devices have designed some dedicated sigma deltas class D amplifiers for audio application with power up to 50 W. (For example: Philips 2 × 50 W class-D amplifier TDA 8920, Texas instrument 2W class-D power amplifier TPA00514, TPA2000D2, AD1996)

2. Interest of our work

2.1 Theory missing

In one hand, the mathematical theory of Class D amplification is quite complex due to a mix of analogue digital and power circuits. The mix between continuous time circuit and discontinuous time circuit make a complete modelling difficult. Software such as MATLAB allows obviously simulation and modelling using the "Z" transform [11]. In a other hand, these amplifiers circuits often look like a "black box" in technical data books. But finally, a simple, intuitive and concrete description of such amplifier is thus rarely found in the literature.

So, what we suggest here is a pedagogical and simplified approach to understand the design of such class D amplifier.

2.2 Pedagogical interest

Whatever the taught electronic field, the link between the theory and practice is often the most important difficulty that appears for the students. Our approach helps them to make this link. Moreover a such practical design allow to sweep, in one project, analogue, digital, power and signal processing aspects of electronic. So, it might be seen a synthesis's project for our engineer students.

3. Design simplified approach

3.1 Sigma delta modulation equivalent modelling

The spectrum of the feed back V_4 signal (cf. figure 5a) after sampling was given in figure 3b in the case of a sinusoidal input signal V_{in}: One sees the spectral line LF (Low Frequency) of the input signal and the periodic lobes related to the sampling. In the case of an unspecified input LF signal V_{in}, one understands, by extension, that the spectrum of the V_4 signal will contain the LF contribution of Vin and - instead of the lobes- an almost "white" spectrum (flat) extending until the infinite.
Consequently, it is possible to establish a first equivalent model [8], in which one replaces the D

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latch by a equivalent switch, switched at the sampling frequency F_e as indicated in figure 5a.

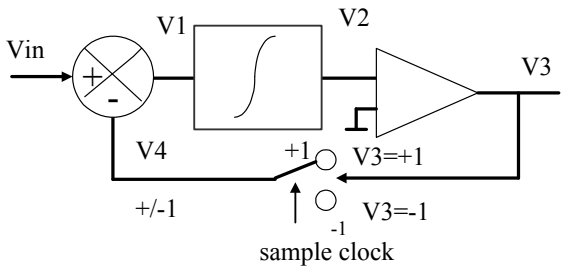

Fig 5a: Simplified modelling

In the second time, the comparator (nonlinear component by nature) and sampling are replaced by an equivalent noise source "B", which is superimposed on the V_2 signal. The "linear" diagram thus obtained makes it possible to compute an equivalent linear transfer function. (cf. figure 5b)

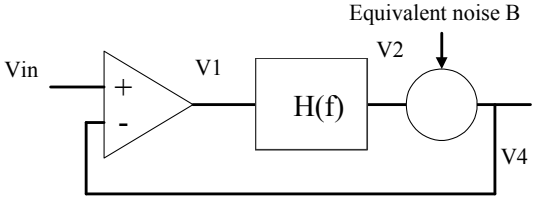

Fig 5b: Simplified noise equivalent modelling

Indeed, we can write:

$$V_1(p)=Vin(p)-V_4(p)$$
$$V_2(p)=H(p)\ V_1(p) \text{ and } V_4(p)=V_2(p)+B \quad (1)$$

With $H(p) = 1/T_c.p$ (with T_c time constant of the integrator)

It yields:

$$V_4(p) =(T_c.p/(1+T_c.p))\ B(p)+(1/(1+T_c.p))V_{in}(p) \quad (2)$$

Thus, the noise B is high pass filtered while the input signal V_{in} is low pass filtered with the same time-constant T_c of the integrator (cf. figure 6). One must thus choose T_c to let pass the maximum frequency F_{max}, of the input signal V_{in}.

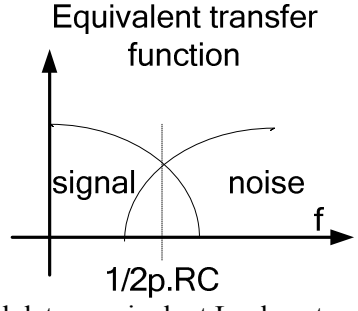

Fig 6: Modulator equivalent Laplace transfer function

3.2 Class D amplifier modelling

Referring to the previous paragraph and from a LF small signal point of view, the class D amplifier (including sigma delta modulator, H bridge and feed back as indicated in figure 4) can be modelled as shown in figure 7.

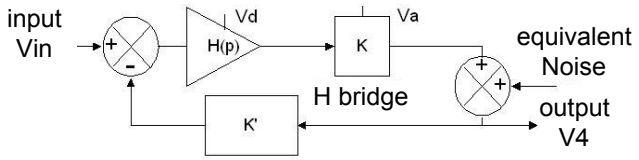

Fig 7: Equivalent class D amplifier LF modelling

Where H(p) is the transfer function on the integrator, K factor, the ratio between the power supply voltage V_a of the power H bridge and the supply voltage V_d of the rest of the circuit ($K= V_a/V_d$). K' the feed back factor can be seen as the ratio of the resistor value R_2/R_1 (cf. figure 4)

After a similar calculus than in § 3.1, it yields (3):

$$V_4(p) = \left(\frac{\frac{T_c}{K.K'}.p}{\left(1+\frac{T_c}{K.K'}.p\right)}\right).B(p) + \frac{1/K'}{1+\frac{T_c}{K.K'}}.V_{in}(p)$$

The equivalent LF gain is 1/K' and do not depends on power supply voltage. At the opposite, V_a supply affects the LF bandwidth.

3.3 Stability aspects

The modulator being a feed back system, it is necessary to wonder about its stability. According to whether one uses an integrator inverter or not, that one will connect on the entry + or – of the comparator, one will need to loop the output Q or /Q of the D latch to ensure stability. In the contrary case, the system is divergent and the output will be locked in a high or low state.

As increasing the order of modulator can cause instability, a simple first order modulator will be used.

4. Design strategy

4.1 Generalities

For the students, a kind of linear « cooking guide » has been written in order to facilitate the design of such amplifier. It includes the mains steps to size the amplifier.

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4.2 Design "cooking guide"

The first step of the design is to size the circuits and components.

Let the supply voltage for all low voltage circuits to be +/-V_d and the power supply voltage for the bridge +V_a.

One can first calculate the minimum required supply voltage of the full or half bridge as follow: Starting from the specified maximum electrical power Pm to be delivered to the load R_L, "to be supposed resistive in the audio bandwidth" (Speaker 8 or 4 Ω),

- One determines first the RMS voltage value V_{bfs} of the useful LF line in the modulated signal by:
$$P_m = (V_{bfs})^2/R_L.$$
- Knowing the Fourier composition of the output signal at its maximum modulation rate, the output LF line can reaches $\sqrt{2}*V_{bfs} = V_a$ for a full H bridge and $0.5*V_a$ for an half bridge.
- The minimum value of the supply voltage V_a is thus :
$$V_a = \sqrt{(P_m.R_L)}.\sqrt{2}$$
for a full bridge, and the double full an half bridge.

Closed LF loop gain determination

- For a correct operation, all voltages through the circuit must be compatible with low voltage power supply +/-V_d. However, the modulation rate is maximum when the peak value of the input signal V_{in} is equal to the peak voltage of the feed back square signal V_4. The consequence is that the maximum value of input voltage V_{in} is :
$$V_{inmax} = V_d/2.$$
As the maximum output peak voltage LF line is equal to V_a, there is a minimum possible LF closed loop gain $G_{min}= 2.V_a/V_d$ for a full bridge.
- While the LF closed loop gain is greater than G_{min} and the LF output voltage do not exceed V_a, the gain value will be set by the resistance ratio $(R_1+R_2)/R_1$ and do not depends on power supply V_a.

5. Detailed design guide

5.1 Generalities

For pedagogical, perennially and cost reasons, the design is done only using discrete and reliable components. The main specifications are:

- Output audio power 10W
- Supply voltage +/-5V and power bridge supply +15V,
- Sampling clock frequency adjustable from:
F_e = 200 kHz to 800 kHz
- Input audio signal: V_{in}, 20Hz-15kHz, 0-2,5V max.
- Amplifier voltage gain: G_v=10.

5.2 Sigma delta modulator

It consists of a classical low cost, fast op amp LF355, a fast comparator AD 790 (switching time must be smaller than (1/10). T_e) and a simple CD4013D latch.

-Choosing the integrator constant R.C:

When removing the integrator capacitor, the sigma delta modulator obviously does not operate correctly: The D latch works as a divider by 2 (/Q looped on the D input through a "delay cell" due to the delay time into the comparator and OP amps).

Under theses conditions, the minimum value of R.C is evaluated as follow:

The output voltage of the integrated stage must not reach the saturation limits during a half period of the $F_e/2$ signal. Thus, R.C value must be greater than T_e to avoid saturation.

Reminding the first condition we found in § 3.1, we can finally summarize the choice of R.C time constant integrator as indicated in figure 8:

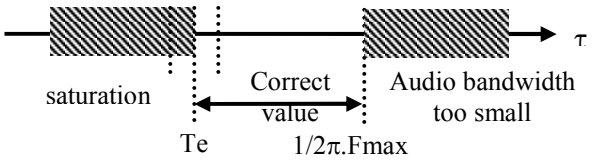

Fig 8: value of RC time constant for sigma delta modulator

- When assembling the sigma delta modulator and the H bridge to build the D class amplifier, we must take care of the K and K' factors: from equation (3) in § 3.2, we can thus determine the RC time constant.

- Choosing the sample frequency:

The sample frequency F_e must be at least greater than 10 times the maximum audio frequency F_{max}. Increasing the sample frequency allows to reject noise in higher frequency, but it also increases the switching losses into the bridge. A good compromise is to choose $F_e = 60.F_{max}$.

5.3 Driver stage

The driver circuit (in our example IRF2113 [3]), located between the PWM modulator and the full bridge, allows the MOS transistors to switch under the best conditions by:

-delivering a 10V voltage pulse and a peak current of 3A to improve the switching times.

-generating a dead time to avoid the cross conduction of two transistors at the switching times.

-inhibiting the gates command signal in case of current overload

5.4 Power MOS stage [12]

- Choosing the power MOS transistor:

If the maximum current or voltage can not be supported by classical bridge integrated circuits such as LM 18200 (NS), L298 (SGS) for example, the students choose a discrete NMOS transistor reference, by looking at the breakdown voltage $V_{(BR)DSS}$ of the transistor and maximum current with the lower R_{on} to minimize the conduction losses. In our example, we uses four discrete matched low "R_{on}" NMOS IRFZ44 (or equivalent) with a bootstrap circuit connected to the driver stage.

5.5 Feed back network

Why and where placing the feed back network is most frequent question. The feed back can be the "natural" sigma delta modulator return (before the full bridge). In this case the LF equivalent closed loop gain will directly depend on H bridge supply voltage value. Thus, it is better to take feed back as close as possible from the load to reduce the defaults and the sensitivity to the supply voltage, noise etc. So, the feed back can take place after the H Bridge on one arm with a simple resistor ratio or on the two arms with a more differential sophisticated network.

In our case, it consists of two resistor's bridge (gain set up and signals scaling), two fast follower op amps and an adder/ subtraction circuit LF 355.

6. Experimental results

The following figures show examples of what the students can measure and check on our electronic demo board. The figure 9 shows the true waveform observed on sigma delta modulator.

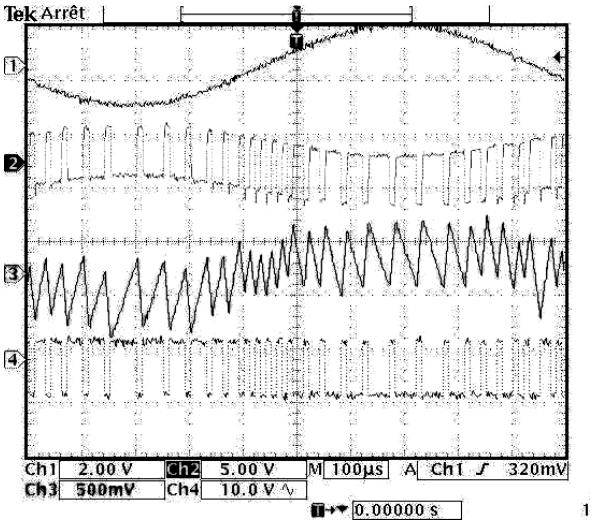

Fig 9: Signal waveform in sigma delta modulator (four traces oscilloscope Tektronix TDS 3114)

Trace 1: input sinus signal 1 kHz,
Trace 2: output of input comparison stage,
Trace 3: output of integrator stage,
Trace 4: Modulated signal (D latch),
(Horizontal scale: 0.1µs/div)

The figure 10 shows the spectrum of modulated signal (has to be compared with figure 3b)

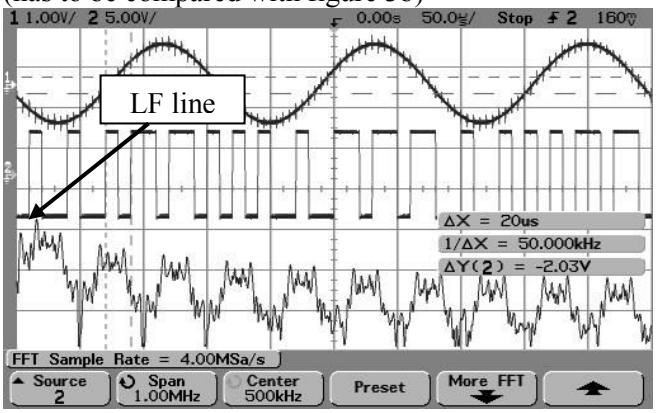

Fig 10: Modulated signal and spectrum waveform (oscilloscope Agilent 54602A)

Trace 1: input sinus signal 1 kHz,
Trace 2: Modulated signal (D latch),
Trace 3: Spectrum (100 kHz/div) (F_e =100 kHz)

The effect of increasing the sample frequency is shown on figure 11. The noise is rejected in higher frequency (as to be compared to figure 10).

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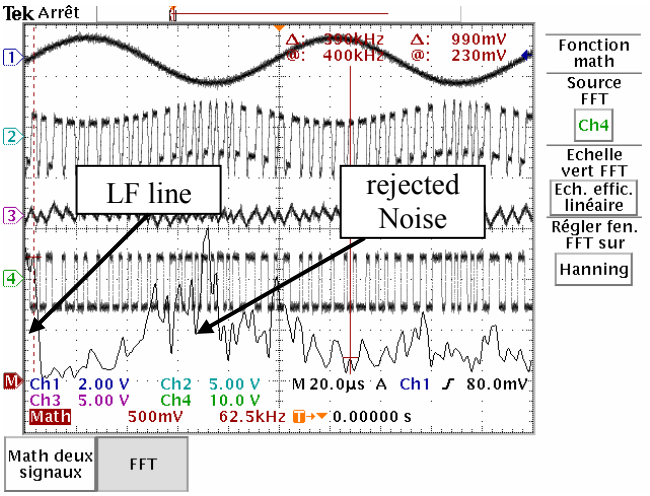

Fig 11: impact of sample frequency value

Trace 1: input sinus signal 1 kHz,
Trace 2: output of input comparison stage,
Trace 3: output of integrator stage,
Trace M: Spectrum of modulated signal, F_e =800 kHz)

From other measurements, we deduce the maximum power ratio (table 1) at 10 kHz input frequency and with a true audio load (three way speakers 8 ohms) at 3 different output useful power levels.

H bridge supply voltage	10V	12V	20V
Output power level	6,25 W	9W	25W
Power ratio	88%	91%	90%

Table 1

Finally, a picture of the test bench is given in figure 12 for full audio tests.

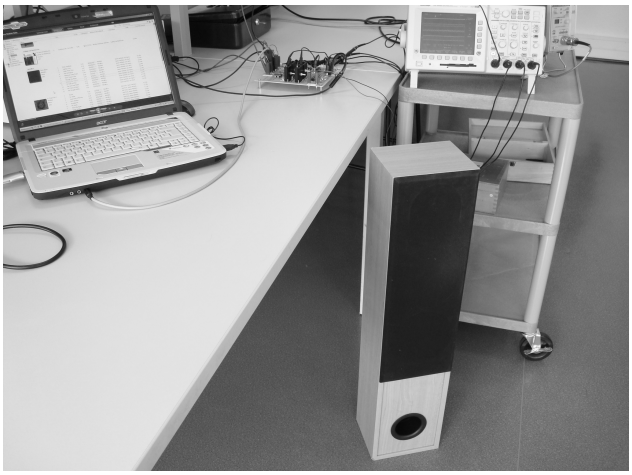

Fig 12: test bench with a 100 W, 8 Ω, 3 ways speaker

7. Pedagogical aspects

7.1 Exporting the design method in a practical lesson for students

Once the class D amplifier design tested and validated, a kind of linear « cooking guide » (based on § 4.2) has been written in order to facilitate the design of class D amplifier by the students. Then, we organized a new practical lesson as indicated in the next paragraph. This new practical 4 hours lesson takes place in the optional practical lesson cycle in second years of study.

7.2 Practical lesson organisation

The teachers present first the class D subject and give some general explanations. Then, our students compute the main components using the design strategy given in § 4.2. Then, they plug the calculated elements (integration capacitor, feed back resistors) on our electronic pre-wired circuit. And they start the measurements in order to observe the signals in all "strategic" points of the class D amplifier. They can check some differences between the basic theory and the practical measurements (signal distortion, true switching times, parasitic oscillations and so on. They try to point out and identify the impact of each important component on global performances (power losses in particular). Finally, they understand how to improve the performances level (noise reduction for example).
Teachers ask for a written report with explanations, measurements and practical curves at the end of the lesson.

8. Conclusion

In this study, we presented a pedagogical method to design a power switching class D amplifier as simply as possible. Modelling the closed loop circuit at the audio frequency for small signals is the most difficult step in this method. The experimental results show a good matching with our pedagogical simplified approach.
However, this method only enables us to find easily the most important parameters of the amplifier; Fine and subtle electronic details must be taught separately. But the most important is that, thanks to this simplified approach, the students are quickly able to make a design of a complex circuit with an excellent efficiency.

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