Symmetric Autozeroing Floating-Gate Transconductance Amplifier for Ultra Low-Voltage Applications

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Abstract: In this paper we discuss the symmetric autozeroing ultra low-voltage transconductance amplifier and present some applications. The autozeroing performed by all ULV circuits is important to reduce the impact of noise and especially avoid power supply noise in mixed signal low-voltage CMOS circuits. The simulated data presented is relevant for a 90nm TSMC CMOS process.

Key–Words: CMOS, Low-Voltage, Amplifier, Autozero, Differential, Floating-Gate

1 Introduction

In this paper we look at the noise properties of ultra-low voltage CMOS transconductance amplifiers. It has always been a challenge to implement analog circuits in a modern digital CMOS process, especially if the analog circuitry is included in a system with clocked digital logic. Traditional amplifiers have been limited by a lower limit for supply voltage given by $2V_t + 2V_{sat}$ which in practice limits the supply voltage close to 1V. Another challenge in mixed signal design is the impact of noise in the supply voltage given by the switching of digital gates. Autozeroing has been proposed as a method to reduce the effect of noise in analog circuits.

While the supply voltage applicable in deep submicron will continue to decrease and eventually fall below 1V the threshold voltage will remain relative stable. The gate oxide thickness becomes only a few nanometers and the supply voltage has to be reduced in order to ensure device reliability. In order to maintain maximum dynamic range, a low voltage analog circuit must be able to deal with signal voltages that extend from rail-to-rail. This requires traditional circuit solutions to be replaced by new circuit design strategies.

Floating-Gate (FG) gates have been proposed for Ultra-Low-Voltage (ULV) [1]. However, in modern CMOS technologies there are significant gate leakage which undermine non-volatile FG circuits. FG gates implemented in a modern CMOS process require frequent initialization to avoid significant leakage. There are several approaches to FG CMOS logic [2, 3, 4].

In section 2 the basic autozeroing ULV circuit is presented, followed by the symmetric ULV transconductance amplifier in section 3 followed by the conclusion in section 4.

2 Ultra Low-Voltage Circuits

![Floating-Gate (FG) transistors](image)

Figure 1: MOS and pMOS clocked semi-floating-gate (CSFG) transistors.

The clocked-semi-floating-gate (CSFG) transistors are shown in Figure 1. The recharge transistors are controlled by clock signals which will force the nMOS evaluate transistor gate terminal (FG) to $V_{DD}$ in the recharge mode, i.e. $\phi = 1$, and the pMOS transistor gate terminal to gnd when recharging. Any input transition will affect the evaluate transistors gate voltage either by a positive or a negative charge. By powering up the gate to source voltages in an initial-
ization phase we are able to reduce the power supply without decreasing the ON current provided by the enhanced transistors. The aim is to maintain a high current level combined with a very low supply voltage. The enhancement can be viewed as an active threshold level combined with a very low supply voltage.

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Figure 2: a) ULV inverter, b) symmetric ULV differential pair and c) symmetric ULV current mirror.

Both digital and analog ULV circuits can be designed using autozeroing ULV inverters. The clock frequency applied must be high enough to avoid significant charge leakage during the evaluation phase. The upper limit for the clock frequency depends on the application and input signal frequency. When the gates, i.e. all gates simultaneously, are recharged, hence output precharged to $V_{DD}/2$, the precise output precharge voltage of each gate is adapted to noise relevant for the gate. The precharge voltage is defined by the offset voltages $V_{pre} = (V_{offset+} + V_{offset-})/2$ due to a reverse biasing gate and simple voltage division. If the evaluate transistor are matched, i.e. $V_{offset-} = V_{DD} - V_{offset+}$, the precharge voltage can be expressed as $V_{pre} \approx V_{DD}/2$.

Note that the evaluate transistors are not required to be matched accurately, we may adjust the precharge level by using the offset voltages. Assuming that $V_{offset+} = V_{DD}$ and $V_{offset-} = V_{ss} = 0V$ we can estimate the effect of power supply noise on the precharge voltage and accuracy of the autozeroing gate. By modelling the power supply noise as $V'_{DD} = V_{DD} + \Delta V_1$ and $V'_{ss} = 0V + \Delta V_2$ we can express the precharge voltage as $V_{pre} = (V'_{DD} + V'_{ss})/2 = (V_{DD} + \Delta V_1 - \Delta V_2)/2$. In addition the nMOS and pMOS evaluate transistors are biased or recharged with the power supply noise $\Delta V_1$ and $\Delta V_2$ respectively. When the gate enters the evaluation phase the gate are biased as an inverter and the power supply noise is evident for the evaluate transistors and the ef-
fective gate source voltage of the evaluate transistors, assuming that the precharge voltage is stable, can be expressed as

\[
V_{DD} + \Delta V_1 - \Delta V_2 \quad nMOS
\]
\[
-(\Delta V_2 + V_{DD} + \Delta V_1) \quad pMOS
\]
\[
= -(V_{DD} + \Delta V_1 - \Delta V_2) ,
\]

and the evaluate transistors remain matched after the autozeroing is performed. All ULV gates respond only to AC signals and blocks the DC level of input signals. This means that the precharge level of inputs and outputs are not important for the circuit’s functionality and accuracy. This feature makes it easier to use ULV circuits together with other subsystems with different supply voltages and you can use external input signals with any DC level.

The switching of power supply when entering the evaluate mode may affect the accuracy of the ULV gate if there is an inherent mismatch associated with the evaluate transistors. This mismatch is not affected by power supply noise or other forms of circuit noise. Transistor mismatches, however may affect the operation of the ULV gates. Ideally the precharge voltage should \( V_{DD}/2 \), or \( (V_{DD} + \Delta V_1 - \Delta V_2)/2 \) in the presence of power supply noise. Evaluate transistor mismatch will affect the output precharge directly through the voltage division in recharge mode. By modelling the mismatch as a transistor threshold voltage shift of the nMOS evaluate transistor, i.e. \( V_{pre} = V_{tn} = V_{tn, nominal} + \Delta V_3 \), the precharge voltage will be \( V_{pre} = (V_{DD} + \Delta V_1 - \Delta V_2 + \Delta V_3)/2 \). When the circuit enters the evaluate mode the output voltage of the gate will be pulled towards one of the rails depending on the sign of \( \Delta V_3 \). If \( \Delta V_3 < 0 \) the nMOS is weak and the output will be pulled towards \( V_{ss} \) and the AC effect of parasitic capacitance seen from the output and to the semi floating-gates \( C_{sg} \) (and eventually \( C_{ds} \)) will increase the effective threshold voltage of the nMOS evaluate transistor and reduce the effective threshold voltage of the pMOS evaluate transistors associated with the gate. Hence, the autozeroing will reduce the effect of transistor mismatches locally. The preceding gate may, however also be affected by the transistor mismatches of a gate. If the precharge level of a specific gate is lower than \( V_{DD}/2 \) due to a strong nMOS evaluate transistor the precharge level of a following circuit will be higher than \( V_{DD}/2 \) and so on. A chain of gates will perform a global common autozero, i.e. with all inherent transistor mismatches, with local autozero and slightly different precharge voltages.

### 3 Symmetric ULV Transconductance Amplifier

![Figure 3: ULV transconductance amplifier.](image)

The ULV transconductance amplifier is shown in Figure 3. Transistor level shown in Figure 3 a) consists of a bidirectional pseudo differential pair and a bidirectional current mirror. We may use simplified ULV inverter symbols for the amplifier as shown in Figure 3 b) where the clock drivers provide the tail current for the pseudo differential pairs as labeled 1 and 2 and the inverters labeled 3 and 4 are the differential input stage of the bidirectional differential pair. The inverters labeled 5 and 6 provide for the current mirror function. The amplifier level symbol is shown in Figure 3 c). Inverter 5 and the local feedback capacitor \( C_f1 \) converts the output current \( I_+ \) of inverter
3 to a voltage $V_a = V_{DD} - V_+$ which yields an output current of the current mirror, i.e. inverter 6, equal to $-I_+$. A significant feature of the symmetrical circuits results in increased transconductance. Basically, after recharge the currents $i_{n+}$ and $i_{p+}$ and $i_n$ and $i_p$, will be the same. Any change in the differential input $\Delta V_{in} = \Delta V_+ - \Delta V_-$ will produce a change in all currents so that

$$
\Delta I_{n+} = -\Delta I_{n-} = -\Delta I_{p-} = \Delta I_{p+} = \Delta I_{p+} - \Delta I_{n+} = \Delta I_{p-} - \Delta I_{n-} = -I_-
$$

and the transconductance of the symmetric pseudo-differential pair is thus the sum of the transconductance of each of the differential pair.

The autozeroing of the ULV gates is performed on the inverter level shown in Figure 3 c) where inverters 5 and 6 are directly connected to virtual power supply provided by clock drivers. Inverters 3 and 4 however perform autozeroing when connected to virtual power $V_p = V'_pDD$ and $V_n = V'_s$. The floating gates are recharged to $V_{DD}$, and $V'_s$ in the recharge phase and when entering the evaluate phase the effective gate to source voltages of the bias transistors are equal to $V_{DD} - V_{ss}$ and $-V'_sDD$ for the nMOS and pMOS pseudo differential pair respectively. Furthermore the evaluate transistors of inverters 3 and 4 which form the symmetric differential pair will be recharged to $V'_pDD - V'_s$ and $-V'_sDD$. The condition $I_{n+} = I_{n-}$ and $I_{p+} = I_{p-}$ still holds, $I_{n+} = I_{p+}$ and $I_{n-} = I_{p-}$ must be satisfied. Assume a positive $\Delta V_1$, i.e. $V'_DD = V_{DD} + \Delta V_1$, the nMOS evaluate transistor will be recharged to provide more current than the pMOS counterparts. In the evaluate mode the increased power supply will increase the current level of the pMOS evaluate transistor and the increased current of the nMOS evaluate transistors will be matched. Furthermore, the current level will match the current level of the symmetric current mirrors as well. In fact, all symmetric ULV gates will be adjusted to the specific power supply available when the circuits enters the recharge state. The autozeroing or recharge frequency may be chosen in a wide range to avoid supply noise and noise imposed by leakage. Note, that the autozeroing is performed at all nodes driven including the internal node $V_a$ in the amplifier shown in Figure 3.

The ULV gates are noise tolerant due to two major aspects

1. **Symmetry.** All ULV gates, both analog and digital, are symmetric. The symmetry allows any circuit to be connected to any other circuit without considering the dc level.

2. **Autozeroing.** All ULV gates, both analog and digital, perform autozeroing at a high rate to reduce impact of noise.

![Figure 4: The output currents of the symmetric ULV transconductance amplifier. $V_{DD} = 300mV$. The output current is not determined by the dc level of the inputs.](image-url)
level is not significant when the inputs are applied to capacitors.

3.1 ULV Voltage Differentiator

By using the ULV amplifier in Figure 3 as a voltage follower we obtain the transfer function $\Delta V_{out} = \Delta V_+$. The circuit follows any change in the input signal when operated in the evaluation mode. By adding another amplifier with opposite clock signals and connect the inputs and outputs we obtain a continuous time voltage follower. The current running in the recharge mode is not significant to the overall performance of the circuit. In Figure 6 a ULV differentiator is shown.

4 Conclusion

The amplifier allows rail to rail signals and no need for dc-dc conversion is required. The ULV amplifier is not directly connected to the power supply and the response of the amplifier is not significantly affected by varying supply voltage. The transconductance amplifier may operate at a supply voltage equal to the threshold voltage of the nMOS transistor in a 90nm CMOS process.

References:


