# Design of Wide-Range Transceiver

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*Abstract:* - This paper describes a wide-range transceiver with a range from 200Mb/s to 4Gb/s. A clock generator applied with Adaptive Frequency Calibrator (AFC) and a Clock Data Recovery Circuit (CDR) is proposed to ensure wide-range operation. The clock generator is designed to operate by compartmentalizing high speed and low speed modes at 2Gb/s as a basis. The AFC is applied to the high speed mode to generate low jitter clock, the Voltage Controlled Oscillator (VCO) is adjusted manually in low speed mode to satisfy wide-range operation. The Proposed CDR circuit uses coarse delay stage based on Delay Locked Loop (DLL) to which has an unlimited capture range, and fine delay stage based on phase interpolator (PI) which adjusts the delayed clock finely. It can guarantee a finer phase step in the wide operation. The designed wide-range transceiver uses 0.18um CMOS process, and is simulated with the modeled channel and equalizer (EQ). The proposed transceiver achieves a BER of less than 10-10 with 27-1 PRBS. The worst phase delay step in the proposed transceiver is 13ps at 200Mb/s to 4Gb/s, and the average phase step is under approximately 10ps.

*Key-Words:* - Wide-range Transceiver, TX, Equalizer, CDR(Clock and Data Recovery), AFC

## 1 Introduction

In digital data transmission, the serial link integration is used widely. Particularly, in multimedia transmission systems to send comprehensive amounts of data at high speeds as well as sending various formats of data, to meet these demands wide-range transmission is necessary. As the CMOS process advances, to achieve higher speed and more compact integration, the serial link systems physical layer design is experiencing the bottleneck condition[1]. In addition wide-range transmission has supplementary design issues to transmit various formats of multimedia data that includes low speed data. Typically, a wide-range clock generator that supports several variables with low jitter at high data rate is indispensable. The receiver requires a wide-range clock data recovery circuit (CDR) that corresponds with the wide-range clock generator. An equalizer (EQ) that can secure a reliable eye-opening from the input data is also necessary. Commonly, when transmitting at high speed the EQ regulates its loop frequency response to recover the Inter Symbol Interference (ISI) input data stream that has been distorted by a limited bandwidth of channel[2][3].

This transceiver is designed to operate from 200Mb/s to 4Gb/s and is based on the Mesochronous clocking system which shares clocks. The Phase Locked Loop (PLL) as a clock generator is designed to operate by compartmentalizing high speed and low speed modes at 2Gb/s as a basis. Due to the effect of the clock jitter on the entire transceiver at higher data rates, to acquire low jitter at high speed mode an Adaptive Frequency Calibration (AFC) is applied. The proposed AFC is designed to generate optimized code by subtraction of counter values and initial values.

The proposed CDR has a dual-loop architecture which uses coarse and fine delay stage to adjust the phase step of the multi-phase clock. The coarse delay stage is based on Delay Locked Loop (DLL) architecture whereas the fine delay stage is based on

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Phase Interpolator (PI). Conventionally, the PI is limited in operational frequency by quantization phase step caused by its nonlinear characteristic[4]. This paper proposes a CDR with the capacity to acquire larger capture range and maintain a finer phase step when wide-range input clock and data rate alters, using the previous PI and DLL. An EQ was designed on the frontal part of the CDR. The entire transceiver system is verified through simulation.

In Chapter II, this paper goes onto elaborate details and results of the simulation of each individual blocks in the proposed design. Chapter III illustrates the simulation of the entire transceiver including the channel. The final conclusion is described in Chapter IV.

# 2 WIDE-RANGE TRANSCEIVER ARCHITECTURE

Fig. 1. is a block diagram of the designed transceiver. The transmitter receives parallel data and multi-phase clock (M_CLK) from the wide-range clock generator, then converts it to serial data to be transferred to the channel through the CML output buffer. Distorted by the channel, the data is compensated via EQ. The compensated data is then inputted to the CDR, and by the regenerated clock it is finally recovered as parallel data. The clock generator of both transmitter and receiver is configured in the same architecture. Description for each individual block is illustrated below.

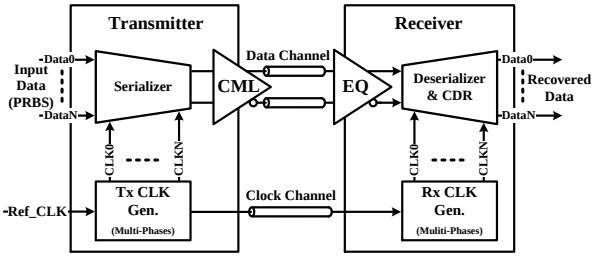


Fig. 1 Block diagram of transceiver

## 2.1 Clock generator

The block diagram of AFC applied wide-range clock generator is shown in Fig. 2. This architecture is configured with a typical integer-N PLL and AFC, the proposed design includes two 6-bit counters, 5-bit subtracter, 5-bit adder, 5-bit register, digital filter and mode selector. The mode selector is programmed to set the initial value of the register and Voltage Controlled Oscillator (VCO) code of low speed mode under 2Gb/s externally. The AFC operation principles are: First, reference frequency (Ref_CLK) and feedback frequency (Div_CLK) values are saved in the counter, second, once the MSB of reference frequency reaches 1, the previously saved values in the counter is sent to the subtracter, third, the subtracter subtracts the two values then sends it to the adder, lastly, the adder adds output value from the subtracter with the initial value of register and sends the result back to the register to renew the value of the register.

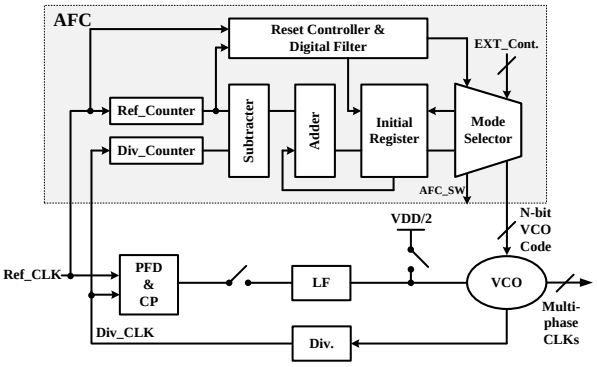


Fig. 2 Block diagram of clock generator

The previous AFC consists of two counters, a magnitude comparator, state control circuit and has fast search time because the use of the binary search algorithm[5]. However, if the reference frequency changes, the bit-depth of the counter must be increased. By using the proposed method, the output of subtracter is more specific down to the difference of frequencies and can send out value ranging from -15 to +15, compared to the previous method using a magnitude comparator to send ‘fast’, ‘slow’ and ‘equal.’ If the output value becomes a negative value, the Div_CLK is faster than the Ref_CLK, if the output value is 0, Ref_CLK and Div_CLK are the same, if the output value is of the positive, the Ref_CLK is faster than the Div_CLK. The activation of AFC mode is determined by the digital filter which receives the subtracted value. If the received values are -1, 0, 1 in sequence, AFC mode is terminated. If any other value is received, AFC mode is activated. Fig. 3. is a waveform of VCO control voltage and AFC Code based on input reference frequency. In Fig. 3. it is apparent that in each input frequency the VCO control voltage is converged to half VDD.

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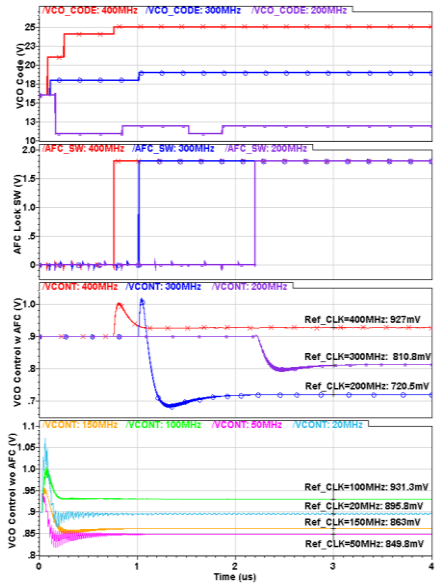


Fig.3 Waveform of VCO control voltage according to Ref_CLK

## 2.1 Transmitter and Equalizer

Transmitter consists of the four components as Shown in Fig 4.: the 10-phase clock generator which distributes to data generator and serializer, the 10:1 MUX stage as a data serializer, the output CML driver stage and the PRBS generator which creates a random Non-Return to Zero (NRZ) data pattern. The data generator is separated into two parts: the PRBS generator makes a random NRZ data stream from 20Mb/s to 400Mb/s and D-FF stages make 10 data stream copies as a forged parallel host data. Each 10 parallel data that passes through the 10:1 multiplexer is serialized into one differential data stream. In the Serializer stage, a binary tree type method with multiplexing technique is used for high-speed operation.

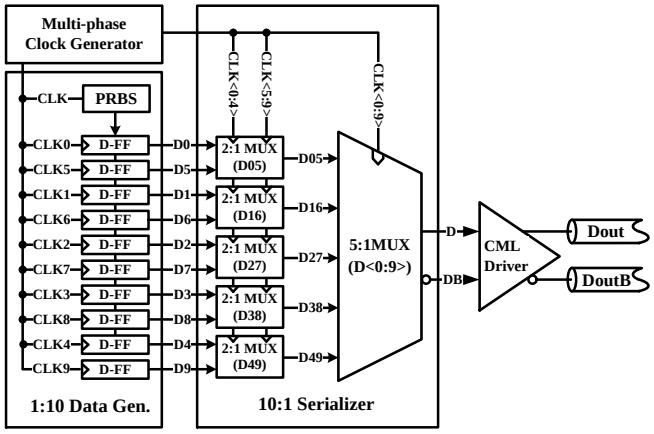


Fig.4 Block diagram of transmitter

Fig. 5. is a block diagram of the applied Continuous Time Linear Equalizer (CTLE), it consists of 3-stage EQ cell to compensate for attenuation of -30dB at a maximum 4Gb/s. The Cheery-Hooper Limiting Amplifier (LA) topology is applied to the EQ cell. Each EQ cell obtains frequency peaking from Nyquist frequency by RC degeneration. The tuning of AC gain in each EQ cell is done by adjusting the array of capacitor bank[6]. Fig. 6 is the result of a simulation of modeled channel attenuation characteristic. Fig. 7. shows EQ gain using a 4-bit capacitor bank, and frequency response when -25dB is compensated.

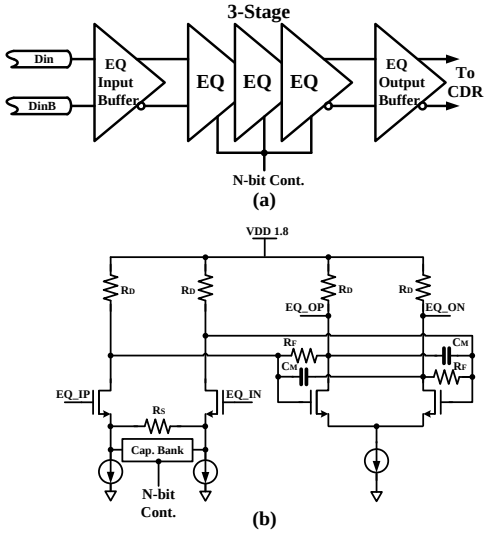


Fig. 5 Block diagram of EQ and circuit of EQ cell

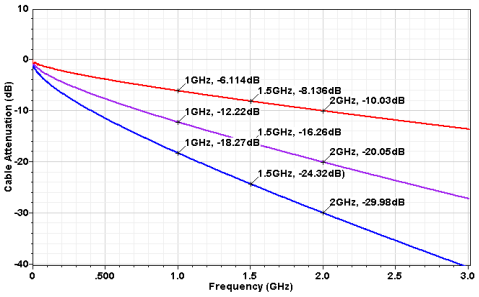


Fig. 6 Channel frequency response

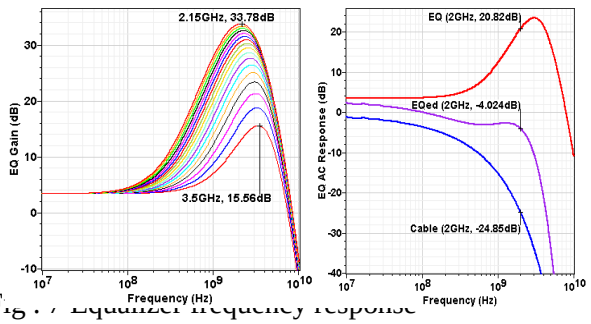


Fig. 7 Equalizer frequency response

## 2.1 Clock and Data Recovery circuit

Fig. 8. is a block diagram of the proposed CDR. Wide-range CDR recovers data by receiving multi-phase clock from the clock generator then adjusting the phase to regenerate clock. PI is unsuitable for wide-range operation, on the grounds that, it reduces a linearity of phase step at low input frequency. The CDR is proposed by using DLL to ensure the coarse resolution that maintains phase step linearity in the PI.

The proposed CDR uses coarse delay stage to insert delay time to the multi-phase clock (M_CLK) then selects delayed clock (D_CLK) to provide to the fine delay stage based on PI. The fine delay stage uses adjacent D_CLK to perform precise PI operation and creates a regenerated clock (R_CLK) with constant phase step. The R_CLK is generated between D_CLK_E and D_CLK_O by receiving control from the control logic then uses the DAC which transforms it into weighted current. If a data rising edge strays from the range between D_CLK_E and D_CLK_O, D_CLKs are changed into the next range to lock. At this step control current uses seamless switching to suppress jitter induction during conversion time.

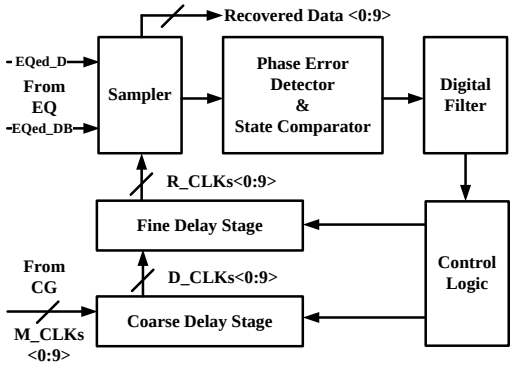


Fig. 8 Block diagram of wide-range CDR

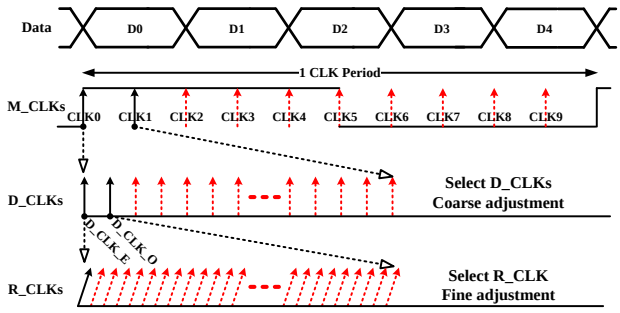


Fig. 9 Timing diagram of coarse and fine delay stage

# 3 SIMULATION RESULTS

Fig. 9. shows the timing diagram of coarse and fine delay stage. Fig. 10. is the result of the simulation on fine delay stage output by DAC code in each process corner (SS, TT, FF). The total coverage phase steps are about 250ps. The average resolution is 9.3ps and the worst resolution is 13ps. Fig. 11. Shows respectively the following: the output of transmitter, the input of receiver and the compensated data from EQ, post-simulated eye-diagrams of data stream with a -25dB attenuation channel at 4Gb/s. Fig. 12. represents the result of Jitter Tolerance (JTOL) using the proposed CDR and results in Fig. 11. The simulation test-bench for Bit Error Rate(BER) test is configured with Verilog-A.

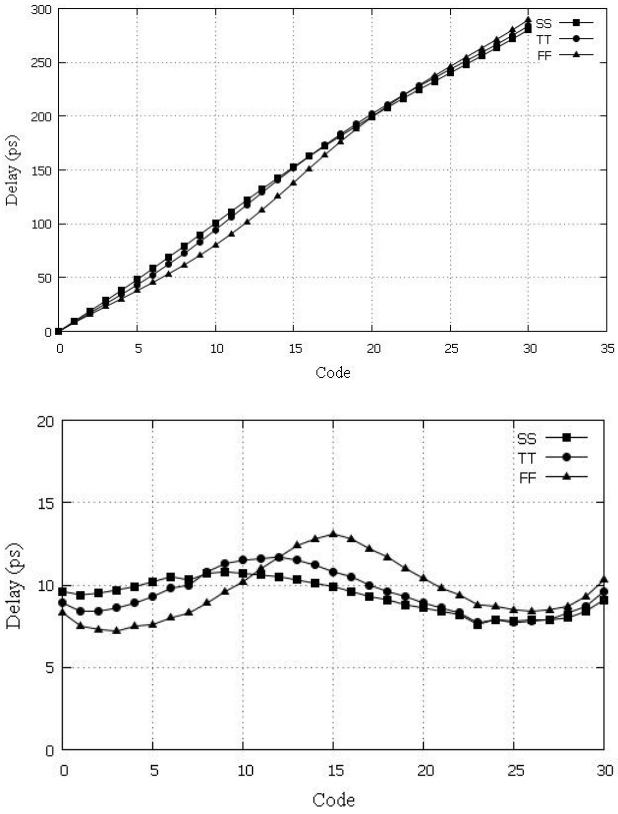


Fig. 10 Fine delay stage resloution

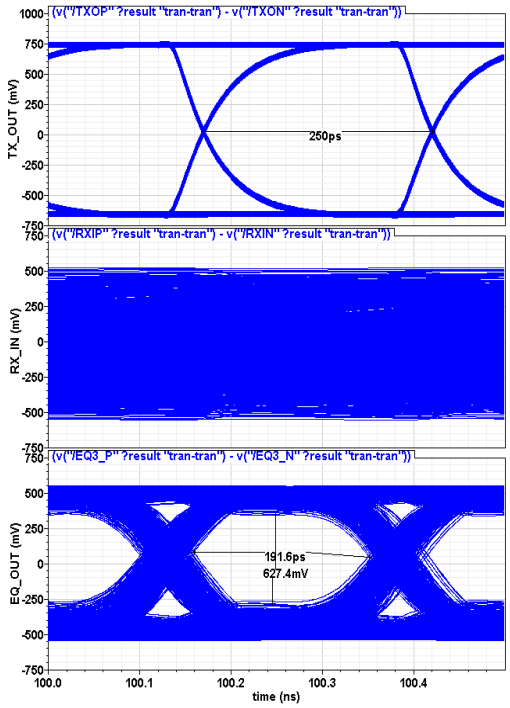


Fig. 11 Eye-diagram of data stream

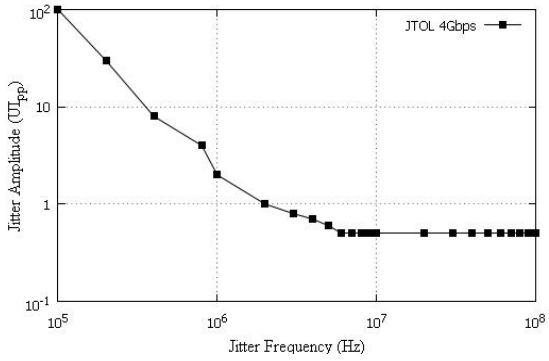


Fig. 12 Jitter tolerence

## 4 Conclusion

A wide-range transceiver was designed with the proposed CDR. The clock generator which generates multi-phase clock according to the reference clock is presented to perform wide-range operation by implementing AFC and high/low speed mode. The proposed CDR is designed with DLL and PI to maintain a constant phase step using multi-phase clock at various data rates. The entire transceiver system including the channel and EQ performance is verified with simulation and the BER of final recovered data from transmitter to receiver is confirmed. The designed transceiver achieved a BER of less than 10-10 with 27-1 PRBS at 4Gb/s. The phase step at 200Mb/s to 4Gb/s is founded to be 7ps to 13ps. In this paper, the performance of transceiver applied with the proposed CDR and wide-range clock generator can be estimated by the simulation.

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