The Probabilistic Model of Random Variation in Nanoscale MOSFET's High Frequency Performance

RAWID BANCHUIN
Department of Computer Engineering
Siam University
235 Petchakasem Rd., Phasi-charoen, Bangkok 10163
THAILAND
rawid_b@yahoo.com

Abstract: - In this research, the probabilistic model of the random variations in nanoscale MOSFET's high frequency performance defined in term of variation in gate capacitance, has been proposed. Both random dopant fluctuation and process variation effects which are the major causes of the MOSFET's high frequency characteristic variations have been taken into account. The nanoscale MOSFET equation has been used as the mathematical basis instead of the conventional square law. The proposed model has been verified based on the 65nm CMOS technology by using the Monte Carlo SPICE simulations of the benchmark circuits and the Kolmogorov-Smirnof goodness of fit tests. They are very accurate since they can fit the Monte Carlo SPICE based data and distributions with 99% confidence. Hence, the proposed models have been found to be the potential mathematical tool for the statistical/variability aware analysis /design of various nanoscale MOSFET based high frequency applications.

Key-Words: - gate capacitance, high frequency, nanoscale MOSFET, statistical design, random variation, variability aware design.

1 Introduction

MOSFET has been adopted in many high frequency circuits, system and applications such as active inductor, active transformer, high frequency filter, optical front ends, clock/data recovery circuits and Bluetooth devices. Of course, the performances of these high frequency equipments are mainly determined by the high frequency performance of their intrinsic MOSFET which can be conveniently measured in term of gate capacitance, C_g.

Obviously, imperfection in MOSFET's properties for example random dopant fluctuation, line edge roughness and gate length random fluctuation cause the random variations in MOSFET's parameters which are crucial in the statistical/variability aware design of MOSFET based applications. This is because these MOSFET's parameters such as drain current, I_d and transconductance, g_m are randomly fluctuated due to the cited imperfection. By this motivation, there are many previous researches on the modeling of such variations in the parameters for example, [1-4] which the state of the art nanoscale CMOS technology has been focused in [2] and [3]. These models take the form of the comprehensive analytical expressions which have been found to be the convenient mathematical tools for the statistical/variability aware analysis/design of various MOSFET based applications. However, these researches did not mention anything about the variation in C_g even though it also exists and significantly impacts the high frequency performances of various MOSFET based circuits, systems and applications. So, it can be seen that these previous models lack of important information for high frequency applications. The impact of C_g's random variation to the cited high frequency performances of MOSFET based applications can be viewed as follows. Since such high frequency performance parameters are functions of C_g, they are randomly varied due to the aforementioned C_g's random variation. For example, the resulting active inductance value of the MOSFET based active inductor is randomly varied due to this C_g's random variation as it is a function of the gate-source capacitance, C_{gs} which in turn is a function of C_g. This is a catastrophic situation for the designing of these high frequency circuits, systems and applications which preciseness is necessary.

Fortunately, there are previous studies in the characteristics of random variation in C_g for example [5-7] etc. The results of these previous studies are the graphical plots and numerical measurement of such variations. Unfortunately,

such results are not generic since they are obtained from a certain technological basis. Furthermore, none of any related comprehensive analytical expressions that display the variation characteristics of C_g has been derived. However, it has been pointed out in [7] that random dopant fluctuation and process variation effects such as line edge roughness and gate length random fluctuation are the major causes of random variations in high ftrequency characteristics of MOSFET including C_g. According to the importance of both C_g along with its possibility to be randomly fluctuated as mentioned above, the comprehensive analytical modeling of its variation similarly to the modeling of the other parameters proposed in the previous researches such as [1-4], must be urgently performed. Furthermore, as the nanometer level technology reigns the CMOS universe nowadays, the nanoscale MOSFET oriented models are more preferable.

Hence, due to the above motivation, the probabilistic model of random variation in nanoscale MOSFET high frequency performance defined in term of variation in C_g, has been proposed in this research. Both random dopant fluctuation and process variation effects which are the major causes of the random viriations in the MOSFET's high frequency characteristics as stated in [7], have been taken into account. The nanoscale MOSFET equation [8] has been used as the mathematical basis similarly to [2] and [3] instead of the classical square law which become inaccurate for the deeply scaled and nanoscale MOSFET. The proposed model has been verified based on the 65nm CMOS process technology by using the Monte Carlo SPICE simulations of the benchmark circuits and the Kolmogorov-Smirnof goodness of fit tests. The verifications have been performed based on both NMOS and PMOS technologies. These models are very accurate since they can fit the Monte Carlo SPICE based data and distributions with 99% confidence. Hence, the proposed model has been found to be the potential mathematical tool for the statistical/variability aware analysis/design of various MOSFET based high frequency applications in the nanometer regime.

2 The Proposed Model

In this section, the proposed model will be discussed. Before proceeds further, it is worthy to give some foundation on the nanoscale MOSFET's equation. According to [8], the drain current, I_d of the nanoscale MOSFET can be given by

$$I_d = WC_{ox}(V_{gs} - V_t)v_{sat} \tag{1}$$

where C_{ox}, W, V_t, and v_{sat} denote the gate oxide capacitance of the transistor, channel width, threshold voltage and saturation velocity [8] respectively.

At this point, the derivation of the proposed model can be started. Firstly, the analytical expression of C_g must be derived. According to [10], C_g can be given by

$$C_g = \frac{dQ_g}{dV_{gs}} \tag{2}$$

where Q_g denotes the gate charge [11]. By using (1) and the methodology adopted from [11], Q_g of the nanoscale MOSFET can be given by

$$Q_g = \frac{WL(V_{gs} - V_t)^2}{3\alpha_d v_{sat} V_t} - Q_{B,\max} \tag{3}$$

where α_d, L and $Q_{B,max}$ denote the coulomb scattering coefficient, channel length and the maximum bulk charge respectively. So, C_g of the nanoscale MOSFET can be given by using (2) and (3) as follows

$$C_g = \frac{2}{3}\frac{WL}{\alpha_d v_{sat}}\frac{V_{gs} - V_t}{V_t} \tag{4}$$

By taking both random dopant fluctuation and process variation effects into account, random variation in C_g existed [7]. Of course, such variation which is denoted by ΔC_g can be defined as the different between the actual value of C_g which is affected by the random dopant fluctuation along with the process variation effects and the nominal one. With such definition of ΔC_g, (4) and Pelgrom's model of variation at the physical level [9], the distribution functions of ΔC_g can be given by

$$pdf_{\Delta Cg}(\delta C_g) = \frac{3\alpha_d v_{sat} V_{TH}}{2\sqrt{2\pi}\, A_{VT}\sqrt{WL}} \exp\left[-\frac{9\alpha_d^2 v_{sat}^2 V_{TH}^2 \delta C_g^2}{8A_{VT}^2 WL}\right] \tag{5}$$

where A_{VT}, δC_g and V_{TH} denotes the Pelgrom's proportional constant [9], any sampled value of ΔC_g and the nominal threshold voltage respectively.

Hence, it can be stated that the proposed model which probabilistically describes the random dopant fluctuation and process variation effects induced random variation in C_g can be given as shown above. At this point, the probabilistic model of the random variation in nanoscale MOSFET's high

frequency performance has been analytically and comprehensively derived. By the analyticity of this model, the probabilistic behavior of such random variation can be thoroughly explained. Since many physical level parameters have been included, this model is highly comprehensive and the physical causes of such random variation in C_g can be thoroughly explored. Compared to the previous studies such as those in [5-7] which presents the study results of variation in C_g in terms of graphical plots and numerical measurements obtained from a certain technological basis, the proposed model is a more analytic, comprehensive and generic result as it is an analytical expression in term of many physical variables without any reference to a certain technology node but to the general nanoscale CMOS technology. An interesting model of the fluctuation in MOSFET's high frequency performances has been proposed in [12]. However, there is none of any physical level variables based analytical expressions of such fluctuations have been proposed. To the knowledge of the author, the proposed model is the first physical level variables based analytical one for the aforementioned high frequency fluctuation.

As formerly mentioned, many meaningful statistical parameters of ΔC_g can be obtained by using this model. For examples, mean and variance of ΔC_g are given by

$$\overline{\Delta C_g} = \int_{-\infty}^{\infty} \delta C_g \, pdf_{\Delta C_g}(\delta C_g) d\delta C_g = 0 \qquad (6)$$

$$\sigma^2_{\Delta Cg} = \int_{-\infty}^{\infty} \left(\delta C_g - \overline{\Delta C_g}\right)^2 pdf_{\Delta C_g}(\delta C_g) d\delta C_g = \frac{4}{9} \frac{A^2_{VT} WL}{\alpha_d^2 v_{sat}^2 V_{TH}^2} \qquad (7)$$

where $\overline{\Delta C_g}$ and $\sigma^2_{\Delta Cg}$ denote mean and variance of ΔC_g respectively. Furthermore, the analytical expressions of many other meaningful statistical parameters such as moments of various orders, skewness and kurtosis can also be obtained by simply apply the conventional mathematical statistic to the proposed model with the required mathematics can be performed even by hand calculation. This is also a merit of the model. At this point, it can be seen that the optimization of the high frequency performances of the nanoscale MOSFET based circuits, systems and applications can be simply achieved by attempting to minimize $\sigma^2_{\Delta Cg}$ which can be obtained from the proposed model as shown above. A possible alternative optimization methodology is to maximize the probability of obtaining zero ΔC_g which can also be analytically derived by using the proposed model. So, it can be seen that such optimization can be performed with the aid of the proposed model.

Furthermore, this model can serves as the mathematical basis for the desired simulations when performing the design by using the electronic CAD tools. The required computational effort is potentially smaller than that of the brute force Monti-Carlo analysis based on the random variations of the parameters at the physical level which is time expensive as mentioned in [13]. According to all aforementioned, the proposed models have been found to be the potential mathematical tool for the statistical/variability aware analysis/design of various MOSFET based high frequency applications at the nanometer level which promisingly gives a significant advancement to the MOSFET's high frequency circuits and systems designing community. In the subsequent section, the verification of the proposed model will be discussed.

3 The Verification

Similarly to [2, 3], the verification of the proposed model has been performed in both qualitative and quantitative aspects. In the qualitative sense, the estimated distributions of random variations in C_g and f_T obtained from the model have been graphically compared to their counterparts obtained from the Monte Carlo SPICE simulations of the benchmark circuits designed with BSIM4 65 nm model. On the other hand, for the quantitative point of view, numbers of Kolmogorov-Smirnof goodness of fit test (KS-test) have been performed by using the cumulative distributions of such random variations obtained from the same set of Monte Carlo SPICE simulations for the qualitative verifications. It should be mentioned here that both NMOS and PMOS technologies have been considered.

As the confidence level of the tests is 99% and the number of runs for the Monte-Carlo SPICE analysis is chosen to be 3000, the critical value of the tests, c has been found to be 0.0297596 [14,15]. In the upcoming subsections, the verifications of the model based on NMOS technology and the PMOS counterpart will be respectively discussed.

3.1 NMOS based model verification

In order to verify the model's accuracy in the prediction of random variation in C_g, the chosen benchmark circuit is a single MOSFET with both

drain and source have been grounded where as the gate terminal has been fed by the input voltage. The input admittance which takes C_g into account can be seen by looking into the input terminal. This methodology of finding the MOSFET's input admittance by using SPICE analysis has also been used in [16]. For NMOS technological basis, this circuit can be depicted in Fig.1. As the input conductance is extremely small, C_g can be approximately given as follows

$$C_g = \frac{Y_{in}}{j\omega} = \frac{1}{j\omega}\frac{I_{in}}{V_{in}} \tag{8}$$

where Y_{in}, I_{in} and V_{in} denote the input admittance, input current and input voltage respectively. Of course, the variation in the formerly defined C_g above obtained from the Monte-Carlo SPICE simulation of this circuit has been adopted as the circuit based ΔC_g for NMOS technology. It should be mentioned here that this benchmark circuit use the nominal channel length of 60nm which is closed to the minimum allowable one along with the nominal aspect ratio of 20.

By proceed in the similar manner to the model verifications in [2, 3], the graphical comparisons for the distributions of per-unit change in C_g which is denoted by $\Delta C_g/C_g$ is depicted in Fig. 3 for the qualitative NMOS based verification. Obviously, it can be seen that a strong agreement between the predicted distribution obtained from the proposed model and the counterpart obtained from the Monte-Carlo SPICE analysis of the benchmark circuit can be observed. Hence, proposed model has been qualitatively verified as highly accurate for NMOS technology.

For the quantitative verification, it can be seen that the resulting goodness of fit test statistic can be found as KS = 0.028462 which is smaller than c = 0.0297596. This means that the proposed model can fit the variation in C_g obtained from the NMOS based benchmark circuit with 99% confidence. At this point, the proposed model verified as highly accurate for NMOS technological basis.

3.2 PMOS based model verification

For the model verification based on PMOS technology, the benchmark circuit similarly to that depicted in Fig.1 can be used with the core PMOS transistor is used instead of the NMOS one. Also similarly to the NMOS based case, the graphical comparison for the distributions of $\Delta C_g/C_g$ is depicted in Fig.3 as the qualitative PMOS based verification. A strong agreement between the distribution obtained from the proposed model and that obtained from the Monte-Carlo SPICE analysis of the PMOS based benchmark circuit has also been observed. Hence, proposed model has been qualitatively verified as highly accurate for PMOS technology.

For the quantitative verification, it can be seen that the corresponding test statistic can be found as KS = 0.018036 which is also smaller than c = 0.0297596. This means that the proposed model can also fit the variation in C_g obtained from the PMOS based benchmark circuits with 99% confidence. At this point, the proposed model is verified as also highly accurate for PMOS technology.

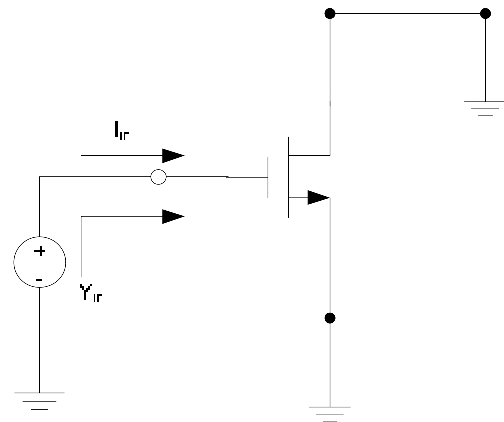

Fig.1: NMOS benchmark circuit for verifying the model of ΔC_g

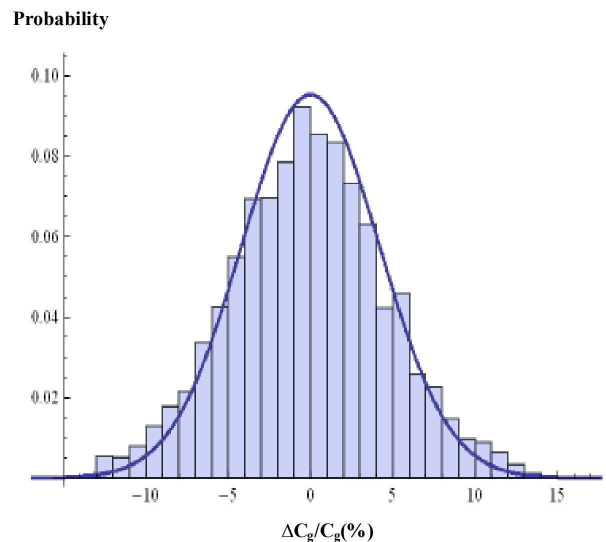

Fig.2. NMOS based comparative distribution plots for $\Delta C_g/C_g$: The model based (line) v.s. The benchmark circuit based (histogram)

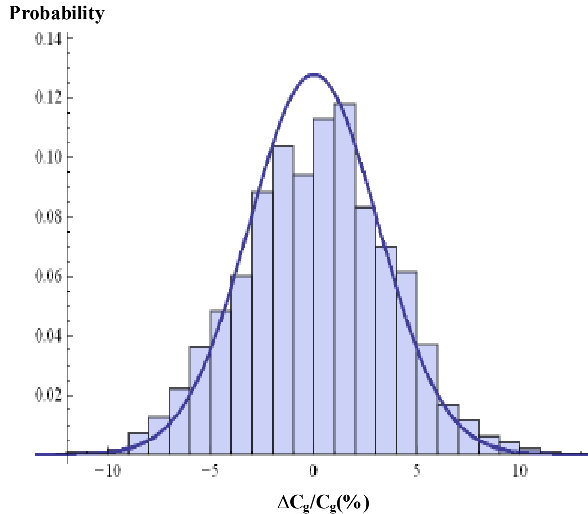

Fig.3. PMOS based comparative distribution plots for $\Delta C_g/C_g$: The model based (line) v.s. The benchmark circuit based (histogram)

4 Discussion

Beside its usual application, the proposed model is applicable as the mathematical foundation for the modeling of the high frequency performance mismatch of the globally spaced nanoscale transistors for example, the mismatch in C_g of such spaced devices which is denoted by DC_g. Since these transistors have similar local variations and low correlation as they are globally spaced, the variance of DC_g is simply twice of its local counterpart given by (7). By this result and the proposed model, the distribution function of DC_g can be simply given by

$$pdf_{DCg}(dC_g) = \frac{3\alpha_d v_{sat} V_{TH}}{4\sqrt{\pi} A_{VT}\sqrt{WL}} \exp\left[-\frac{9\alpha_d^2 v_{sat}^2 V_{TH}^2 dC_g^2}{16 A_{VT}^2 WL}\right] \quad (9)$$

where dC_g denotes any sample value of DC_g.

Now, the discussion regarding to the results obtained from the model verifications will be given. It can be seen from the formerly shown Monte Carlo SPICE analysis results that the maximum percentages of variations in C_g obtained from the NMOS based benchmark circuit which is given by 14.037, has been found to be higher than its counterparts obtained from the PMOS ones which is 10.61%. This means that nanoscale PMOS technology is more robust to the random dopant fluctuation and process variation effects than its NMOS counterpart due to its lower percentage of variation.

Furthermore, it has been observed that the test statistic for the PMOS based verification which is 0.018036, has been found to be smaller than the NMOS based counterpart which is given by 0.028462. This means that the proposed model is better fit to the PMOS based data than the NMOS based one due to its smaller statistic. So, it can be seen that this model can predict the variation for the nanoscale PMOS transistor with higher accuracy than the similar prediction for the NMOS one.

5 Further Studies

There are many potential further studies for this research. One of these is to perform the similar probabilistic modeling for the MOSFET's cut off frequency, f_T and the maximum oscillation frequency, f_{max} since they are also crucial high frequency characteristics. The other tentative further study is to perform the similar modelling based on the up to dated physical level variation models for example, those proposed in [17] and [18] etc.

6 Conclusion

The probabilistic models of random variarions in nanoscale MOSFET's high frequency performance defined in terms of variation in C_g, has been proposed. Both random dopant fluctuation and process variation effects which are the crucial causes of the MOSFET's high frequency characteristic variations [7] have been taken into account. The nanoscale MOSFET equation proposed in [9] has been used as the mathematical basis instead of the conventional square law. The proposed probabilistic model have been verified based on both NMOS and PMOS technologies at 65nm level by using the Monte Carlo SPICE simulations of the BSIM4 65 nm model based benchmark circuits along with the KS tests. The model has been found to be very accurate since it can fit the Monte Carlo SPICE based data and distributions with 99% confidence. Hence, the proposed model has been found to be the convenient mathematical tool for the statistical/variability aware analysis/design of various nanoscale MOSFET based high frequency applications such as active inductor, active transformer, high frequency filter, optical front ends, clock/data recovery circuits and many Bluetooth devices.

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