Controllers for Power Factor Correction of PMBLDCM Drive

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Abstract—The power quality (PQ) disturbances at utility AC mains of a permanent magnet brushless DC motor (PMBLDCM) drive are of prime concern in their applications. This paper discusses modeling and simulation of control strategies for operation of various DC-DC converters as power factor correction (PFC) converters for a PMBLDCM drive. The performance simulation of a non-isolated buck-boost converters fed PMBLDCM drive is carried out in MATLAB-SIMULINK environment to demonstrate the effectiveness of the modeling concepts.

Keywords—power factor correction, harmonic mitigation, DC-DC converters, control schemes, PMBLDCM drive, power quality.

1 Introduction
Permanent magnet brushless DC motors (PMBLDCMs) are considered as better option in various low power (less than 5 kW) applications due to their energy efficiency and ease of control [1-3]. The PMBLDCM is a three-phase synchronous motor with permanent magnets (PMs) on the rotor. The commutation in a PMBLDCM is accomplished by solid state switches of a three-phase voltage source inverter (VSI). The combination of VSI and PMBLDCM is referred as PMBLDCM drive [4-10]. The efforts of researchers towards improvement in the performance of traditionally used motors such as induction motors, DC motors and synchronous motors has opened up new application areas of the PMBLDCM. Moreover, the advancements in power electronics and digital signal processors (DSPs) have added many features to the PMBLDCM drives to make them preferred choice for various industrial installations [1-10].

The most commonly used topology for PMBLDCMD fed from single-phase AC mains uses a diode bridge rectifier (DBR) followed by a smoothing DC capacitor as shown in Fig. 1. It draws an uncontrolled charging current for the DC capacitor resulting in a pulsed current from the AC mains as shown in Fig 2, resulting in various power quality (PQ) disturbances at AC mains such as poor power factor (PF), increased total harmonic distortion (THD) of AC mains current and its high crest factor (CF). The power quality (PQ) disturbances at AC mains of a PMBLDCMD are represented in terms of various power quality indices such as PF, CF, total harmonic distortion (THDi) of AC mains current, displacement power factor (DPF) and ripples in DC link voltage ($\Delta V_{dc}$) [11-20].

Fig. 1 Basic DBR based topology for PMBLDCMD

Fig. 2. Current waveform at AC mains and its harmonic spectra for the PMBLDCMD topology shown in Fig. 1

These PQ disturbances result in transformer and neutral conductor heating, heating of motors and cables, EMI, power supply failure (brownout or blackout) and component failure. Reduction of harmonic currents and voltage distortion at AC mains with near unity PF are referred as power factor correction (PFC) and mitigation of PQ disturbances. Various DC–DC converters are operated as PFC converters for variety of applications. The performance of a PFC converter is evaluated on the basis of these PQ indices. For the monitoring and mitigation of these PQ problems in the low power...
applications, there are international standards such as IEC 61000-3-2 [21] and IEEE 1159 [22] under enforcement. These standards emphasize on low harmonic contents and near unity power factor current to be drawn from AC mains by various loads. As reported in the literature [11—20], the PFC converter topologies in various commercial applications possess two-stages of DC-DC converters. A boost DC-DC converter is used as a power factor pre-regulator (PFP) at the front-end followed by second stage DC-DC converter for voltage regulation. The second converter is usually a flyback or a forward converter for low power application (less than 1 kW) and a full-bridge converter for higher power applications (1-5kW). However, the high cost and complexity in operation of two DC-DC converters are the constraints of the two stage PFC converters resulting in the use of a single stage PFC converter in many applications. Moreover, the additional cost and complexity of two-stage PFC is not justified for low power applications, therefore, the converter topologies with features of PFC as well as voltage regulation in single stage are preferred in the PMBLDCM drives.

There are many DC-DC converter topologies e.g. buck, boost, buck-boost, Ćuk, SEPIC, zeta, push-pull, half bridge and full bridge, reported in the literature [9, 11-20] for general purpose loads, which can be modeled and designed for PMBLDCM drives. There are various control strategies reported in the literature [4-9] for PFC. This paper primarily focuses on the two control strategies which are based on current multiplier control and voltage follower control due to their inherent advantages of PFC with other added features. The current multiplier control is further investigated in terms of peak current control and average current control for PFC at AC mains. The voltage follower control has been reported in the literature with a variety of applications such as switched mode power supplies (SMPS) and electronic ballasts, due to inherent advantages of PFC with reduced sensors and single control loop, however, it has a disadvantage of increased peak current rating of the solid state switches.

The current multiplier control requires additional sensors for input current (i_d) and supply voltage (v_s). High-frequency PWM and hysteresis current control techniques are usually employed for the current control loop and wide-bandwidth controllers in voltage loop to provide fast response and desired PQ at input AC mains. The current multiplier control results in current control at input AC mains and DC link voltage control of the PMBLDCM drives along with improved power quality at AC mains.

The voltage follower control has been reported in the literature with a variety of applications such as switched mode power supplies (SMPS) and electronic ballasts, due to inherent advantages of PFC with

![Fig. 3 PFC controller topology based on current multiplier control (average current control)](image)

![Fig. 4 PFC controller topology based on voltage follower control](image)

**2 Modelling of current multiplier control for PFC**

The current multiplier control is modeled for PFC as shown in Fig. 3 consisting of a voltage controller, a reference current generator and a current controller.

**2.1 Voltage Controller**

The voltage controller is a proportional-integral (PI) controller which processes voltage error V_e and outputs a control signal (I_c). The output of the PI controller I_c(k) at k^{th} instant is given as

\[ I_c(k) = I_c(k-1) + K_{pv} (V_e(k) - V_{dc}(k-1)) + K_{iv} V_e(k) \]  

(1)

where K_{pv} and K_{iv} are proportional and integral gains and V_e is voltage error input to PI controller given as,

\[ V_e(k) = V^*_e(k) - V_{dc}(k) \]  

(2)
where $V_{dc}^*(k)$ is the reference DC voltage and $V_{dc}(k)$ is the actual DC link voltage at $k^{th}$ instant.

### 2.2 Reference Current Generator

The reference current for the PFC controller ($i_{d}^*$) is given as,

$$i_{d}^* = I_{c}(k)u_{vs}(3)$$

where $u_{vs}$ is the unit template of the voltage at input AC mains, calculated as,

$$u_{vs} = \frac{v_d}{V_{sm}}; v_d = |v_s|; v_s = V_{sm}\sin \omega t \quad (4)$$

where $\omega$ is frequency in rad/sec at input AC mains.

### 2.3 Current Controller

Fig. 3 shows the PFC control topology with current multiplier control. The strategies for current controller include average current control, peak current control and hysteresis current control.

#### 2.3.1 Average current control

The average current control uses average value of sensed current ($i_d$) which is compared with reference input current of the PFC converter ($i_{d}^*$) to generate the current error $\Delta i_d = (i_{d}^* - i_d)$. This current error is amplified by gain $k_d$ and compared with fixed frequency ($f_s$) saw-tooth carrier waveform $m_d(t)$ to get the switching signals for the power switch (i.e. MOSFET/IGBT) of the PFC converter as shown in Fig. 5 and given as,

If $k_d \Delta i_d > m_d(t)$ then $S = 1$  \quad (5)

If $k_d \Delta i_d <= m_d(t)$ then $S = 0$  \quad (6)

where $S$ is the switching function representing ‘on’ position of the switch of the PFC converter with $S=1$ and its ‘off’ position with $S=0$.

#### 2.3.2 Peak current control

Fig. 6 shows the PFC controller with peak current control. The reference input current of the PFC converter ($i_{d}^*$) is compared with its sensed peak current ($i_{sw}$) to generate the current error $\Delta i_d = (i_{d}^* - i_{sw})$. The amplified current error is used to generate the switching signals for the solid state switch (i.e. MOSFET/IGBT) of the PFC converter as given by equations (5-6). The current control envelop is depicted in Figs. 7-8 for average current control and peak current control respectively.

#### 2.3.3 Hysteresis Current Controller

The hysteresis current controller restricts the current within the specified limits as depicted in Fig. 9. However the control of switching frequency is lost and there can be abnormal increase of the switching frequency for the desired current limit which may damage the solid state switch i.e. IGBT/MOSFET.

### 3 Modeling voltage follower control for PFC

The modeling of voltage follower control for PFC consists of the modeling of a voltage controller and a PWM controller.

#### 3.1 Voltage Controller

The voltage controller for voltage follower control is also modeled in same way as discussed in subsection 2.1 as given by equations (1-2).

#### 3.2 PWM Controller

The control signal ($I_c$) from voltage PI controller is compared with fixed frequency ($f_s$) saw-tooth carrier waveform $m_d(t)$ to get the switching signals for the solid state switch (i.e. MOSFET/IGBT) of the PFC converter as shown in Fig. 5 and given as,

If $I_c > m_d(t)$ then $S = 1$ (MOSFET ‘on’) \quad (7)

If $I_c <= m_d(t)$ then $S = 0$ (MOSFET ‘off’) \quad (8)

where $S$ is the switching function representing ‘on’ position of the switch of the PFC converter with $S=1$ and its ‘off’ position with $S=0$. 

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Fig. 5 PWM pulse generation for PFC converter operated with current multiplier control

Fig. 6 PFC controller topology based on current multiplier control (peak current control)
The envelop of current in voltage follower control is depicted in Fig. 10 which uses the DCM operation of the converter i.e. the current becomes zero in each switching cycle. Therefore for the same average current requirement in the PMBLDCM drive the peak current value of the drive shall be higher as compared to current multiplier control.

![Fig. 9 The envelop of hysteresis current control](image9)

![Fig. 10 The envelop of voltage follower control](image10)

Fig. 11 Simulated performance of non-isolated buck-boost PFC converter fed PMBLDCMD with current multiplier control

Fig. 12 Simulated performance of non-isolated buck-boost PFC converter fed PMBLDCMD with voltage follower control

a THD, at 1500 rpm  
b THD, at 1000 rpm  

Fig. 13 I_s and its harmonic spectra under steady state condition for non-isolated buck-boost PFC converter fed PMBLDCMD with current multiplier control

Fig. 14 I_s and its harmonic spectra under steady state condition for non-isolated buck-boost PFC converter fed PMBLDCMD with voltage follower control
4 Results and Discussion

The performance simulation of a non-isolated buck-boost DC-DC converter for current multiplier control and voltage follower control has been carried out for power factor correction of a 2 hp, 1500 rpm permanent magnet brushless DC motor (PMBLDCM) drive. The simulated performance of the PMBLDCM drive is shown in Figs. 11-12 in terms of AC mains voltage ($V_a$), source current ($I_a$), DC link voltage ($V_{dc}$), speed, torque and phase current of the PMBLDC motor ($N$, $T_e$ & $I_a$). It is observed that the current multiplier control effectively maintains the DC link voltage at the reference value under speed control along with sinusoidal source current. However, the voltage follower controller has demonstrated larger settling time of DC link voltage with overshoots and dips.

The power quality performance is also demonstrated in Figs. 13-14 for current multiplier control as well as voltage follower control strategies. The results of PFC converter fed PMBLDCM drive demonstrate THD of AC mains current within the limits of IEC 61000-3-2 with sinusoidal current drawn from AC mains. The PF is maintained near unity with an efficient control of speed at rated torque conditions.

5 Conclusion

The modeling and simulation of various controllers for PFC of a PMBLDCM drive has been carried out in this paper to demonstrate the effectiveness of these control strategies in power factor correction. These control strategies can be applied to various DC-DC converters for PFC of utility fed PMBLDCM drive in a variety of applications. These controllers are more suitable for low power applications where low cost controllers are required. It is hoped that this paper shall be a helpful reference for the professionals working in the area of power factor correction.

References