IMPLEMENTATION OF MULTILEVEL INVERTER WITH MINIMUM NUMBER OF SWITCHES FOR DIFFERENT PWM TECHNIQUES

1P.Rajan * R.Vijayakumar, **Dr.Alamelu Nachiappan,
**Professor of Electrical and Electronics Engineering
Pondicherry Engineering College, Pondicherry
*Research Scholar, Pondicherry Engineering College, Pondicherry
1Research Scholar, Christ College of Engineering and Technology, Pondicherry

Abstract-Titled research work has been dealt with different types of PWM technique for Multilevel Inverter with reduce number of switches. In the past decades, the researchers have dealt with the conventional topology, which possesses twelve switches of Multilevel Inverter is applied to PWM method. The present research work has been introduced a new method of multilevel inverter using 5 switches is applied with different PWM technique. In introduction part the conventional cascaded multilevel inverter & switching pattern are explained. In second part PWM technique of proposed work and circuits is explained. The comparative analysis for different PWM techniques and with and without filter using different modulation index is demonstrated using MATLAB/SIMULINK.

Keywords: Multilevel Inverter; Total Harmonics Distortion; Pulse Width Modulation; Switching Frequency Optimal.

1. INTRODUCTION

Nowadays, multilevel inverters have received more attention for their ability on high power and medium voltage operation and for other advantages such as high power quality, low order harmonics, lower switching losses and better electromagnetic interferences.[1] These cascaded multilevel inverter generate a stepped voltage waveform, and more number of dc voltage waveform and switches will be used and they explain only the inverter operation and do not explain in different type of PWM technique is apply in proposed multilevel inverter.[2] These multilevel inverter is using a single phase seven level inverter for grid connected system. They are not explaining in different type of PWM technique is applied in proposed multilevel inverter.[3] These symmetric multilevel inverter introduce the least number of switches, and gate trigger circuitry, switching loss are reduced, cost and size, but it is implemented in basic sinusoidal pulse with modulation (SPWM) technique.[4] These cascaded multilevel inverter are using a nine and seven switches and sinusoidal pulse with modulation (SPWM) technique is also implemented using multicarrier wave signals, but they are not used in different type of PWM technique is apply in proposed multilevel inverter.[5-11] In recent years, different symmetric cascaded multilevel inverters have been presented, the main disadvantage of these circuits is some of them use a high number of bidirectional switches. More number of insulated gate bipolar transistors are required and they are not implemented in different type of PWM technique. Generally, voltage source inverter (VSI) and current sources inverter (CSI) are widely used for grid integration of renewable
energy; recent trend goes towards the use of multilevel inverter. Because of these several benefits, MLI generates output having less distortion, produces lesser common mode voltage, produces less stress, reduces electromagnetic interference and generates better quality output. MLI also pertains to lesser and smaller filter size [12&13]. Several commercial MLI topologies are existing such as neutral point clamped inverter, flying capacitor, cascaded H bridge [12&13]. Among these, cascaded multilevel inverter is suited for induction motor drives application.

In this paper, a new topology of multilevel inverter is proposed in order to increase the number of output voltage levels and reduce the number of switches, drives circuit, total cost of the inverter, and implementation of different type of PWM technique. Moreover, the proposed topology is compared with other topologies from the different point of view. Such as number of IGBT, number dc sources and performances of different type of PWM technique. Finally, the performances of the proposed topology in generating are voltage levels through a seven levels inverter is confirmed by simulation using a (MATLAB/SIMULINK).

2.0 CONVENTIONAL METHOD

2.1 A 12 Switches Cascaded H-Bridge topology.

A single-phase structure of an m-level cascaded inverter is illustrated in Fig.1. Each separate dc source (SDCS) is connected to a single-phase full-bridge, or H-bridge, inverter. Each inverter level can generate three different voltage outputs, +Vdc, 0, and −Vdc by connecting the dc source to the ac output by different combinations of the four switches, S1, S2, S3, and S4. To obtain +Vdc, switches S2 and S3. By turning on switches S1 and S2 or S3 and S4, the output voltage is 0. The ac outputs of each of the different full-bridge inverter levels are connected in series such that the synthesized voltage waveform is the sum of the inverter outputs. The number of output phase voltage levels m in a cascade inverter is defined by

\[ m = 2s + 1 \]

where s is the number of separate dc sources. A stepped output voltage and current can be obtained in a cascaded MLI by cascading several H-bridge inverters. Adding another H-bridge to the existing H-bridge, number of levels increases by two. Hence for a 7-level output, three H-bridge inverters are to be cascaded as shown in Fig. 2. The switching states of the cascaded 7-level multilevel inverter are shown in Table1.
Table 1: Switching sequence of cascaded multilevel inverter using 12 switches

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>$S_1$</th>
<th>$S_2$</th>
<th>$S_3$</th>
<th>$S_4$</th>
<th>$S_5$</th>
<th>$S_6$</th>
<th>$S_7$</th>
<th>$S_8$</th>
<th>$S_9$</th>
<th>$S_{10}$</th>
<th>$S_{11}$</th>
<th>$S_{12}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{L1}$</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$V_{L2}$</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$V_{L3}$</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>$V_{L4}$</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>$V_{L5}$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>$V_{L6}$</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

3.0 PULSE WIDTH MODULATION (PWM) TECHNIQUE

3.1 Constant Switching Frequency Multicarrier Pulse Width Modulation (CSFMC-SH PWM).

A Constant switching frequency multicarrier sub harmonic pulse width modulation (CSFMC-SH PWM) Fig. 3 shows an m-level inverter, m-1 carriers with the same frequency $f_c$ and the same amplitude $A_c$ are disposed such that the bands they occupy are contiguous. The reference waveform has peak to peak amplitude $A_m$, the frequency $f_m$, and its zero centered in the middle of the carrier set. The reference is continuously compared with each of the carrier signals. If the reference is greater than $s$ carrier signal, then the active device corresponding to that carrier is switched off. In multilevel inverters, the amplitude modulation index $M_a$ and the frequency ratio $M_f$ are defined as

$$M_a = \frac{A_m}{(m-1)A_c} \quad (1)$$

$$M_f = \frac{f_c}{f_m} \quad (2)$$

3.2 Constant switching frequency multicarrier switching frequency optimal pulse width modulation (CSMC-SFO PWM).

Fig. 4 shows the (CSFMC-SFO PWM) in which triplen harmonic voltage is added to each of the carrier waveforms. The method takes the instantaneous average of the maximum and minimum of the three reference voltages ($V_a$, $V_b$, $V_c$) and subtracts the value from each of the individual reference voltages to obtain the modulation waveforms.

$$V_{offset} = \frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2} \quad (3)$$

$$V_a^{SFO} = V_a - V_{offset} \quad (4)$$

$$V_b^{SFO} = V_b - V_{offset} \quad (5)$$

$$V_c^{SFO} = V_c - V_{offset} \quad (6)$$

The zero sequence modification made by the SFO PWM technique restricts its use to three phase three wire system, however it enables the modulation index to be increased by 15% before over modulation or pulse dropping occurs. In this paper to increase output voltage, MC-SFO PWM technique is used and by Third harmonic injection, the...
output voltage $V_{ac}$ can be achieved to 30V with THD value 19.97%.

**Fig.4** Constant switching frequency multicarrier switching frequency optimal pulse width modulation (CSMC-SFO PWM).

### 3.3. Variable Switching Frequency Multicarrier Sub harmonic Pulse Width Modulation (VSFMC-SH PWM)

A Variable switching frequency multicarrier sub harmonic pulse width Modulation (VSFMC-SH PWM) For a multilevel inverter, if the level are $m$ there will be $m-1$ carrier set with variable switching frequency multi carrier Pulse width modulation when compared with sinusoidal reference. The carriers are in phase across for all the bands. In this technique, significant harmonic energy is concentrated at the carrier frequency. But since it is a co-phase component, it doesn’t appear line to line voltage. In this paper, we proposed a seven level inverter whose levels are $\{0,V_{dc},2V_{dc},3V_{dc}\}$ its carrier set are assigned to have variable switching frequency of 1000 Hz and 3000Hz as shown in the **Fig.5**.

### 3.4. Variable Switching Frequency Multicarrier Switching Frequency Optimal Pulse Width Modulation (VSFMC-SFO PWM)

For a multilevel inverter, if the level is $m$ there will be $m-1$ carrier set with variable switching frequency multi carrier Pulse width modulation when compared with third harmonic injection reference. For third harmonic injection given as

$$Y = 1.15sint + 1.15sint/6sint (7).$$

The resulting flat topped waveform allows over modulation while maintaining excellent AC term and DC term spectra. This is an alternative to improve the output voltage without entering the over modulation range. So any carriers employed for this reference will enhance the output voltage by 15% without increasing the harmonics. In this paper, there are seven level inverter is proposed whose levels are $\{0,V_{dc},2V_{dc},3V_{dc}\}$, its carrier set are assigned to have variable switching frequency of 1000 Hz and 3000Hz as shown in the **Fig.6**.
3.5 Phase Shifted Carrier Switching Frequency Optimal Pulse Width Modulation (PSC SFO PWM).

Fig. 7 shows the phase shifted carrier switching frequency optimal pulse width modulation (PSC SFO PWM). Fig. 8 shows the phase shifted carrier SFO PWM modulating signal generation. The method takes the instantaneous average of the maximum and minimum of the three reference voltages \( V_a, V_b, V_c \) and subtracts the value from each of the individual reference voltages to obtain the modulation waveforms. Using equation (3,4,5,6 )The carrier voltage is the average of maximum and minimum value of \( V_a, V_b, V_c \). The phase voltage using SFO is the difference between reference voltages to carrier voltage. The zero sequence modification made by the SFO PWM technique restricts its use to three phase three wire system, however it enables the modulation index to be increased by 15% before over modulation or pulse dropping occurs.

5.0 PROPOSED 5 SWITCHES CASCADED H-BRIDGE TOPOLOGY

5.1 Circuit Description

The proposed five switched topology has been introduced in Fig. 9. It is about modifying or reducing single switch from 10 switches topology obtaining the tag of 5 switches configuration. The proposed 5 switches topology is simpler design compared to all conventional topologies.
This proposed topology method using generalized expression for the output voltage level is

\[ V_0 = (2 \times S_n - 3) \]

Where \( V_o \) = Number of output voltage level

\[ S_n = \text{Number of switches} \]

\[ V_0 = (2 \times V - 1) \]

Where \( V \) = Number of DC sources

To obtain the unique pulse pattern and trigger the switches at the proper instant, switches \( S_1, S_2 \) and \( S_3 \) get compulsorily unidirectional, otherwise the output waveform will get distorted. The system is more compact and user friendly by using reduced number of switches. The seven levels MLI result in less utilization of sources through the usage of the four separate dc sources for the generation. Number of H-Bridge is used and it plays 2 switches producing reversal polarity. Table 2 represents the switching scheme for the proposed topology.

<table>
<thead>
<tr>
<th>Output Voltage</th>
<th>( S_1 )</th>
<th>( S_2 )</th>
<th>( S_3 )</th>
<th>( S_4 )</th>
<th>( S_5 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_0 )</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>( 2V_0 )</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>( 3V_0 )</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>( 4V_0 )</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>( -V_0 )</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>( -2V_0 )</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>( -3V_0 )</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 2 switching scheme for the proposed topology.

5.2. Power Stage Operation

The switching sequences for the generation of positive levels \((0, V_{dc}, 2V_{dc}, V_{dc})\) named as level 0, level 1, level 2, level 3 are as shown in Table 2. According to the table, there are four possible switching states to control the inverter. The required output positive voltage levels produced by the level generator are generated as follows:

1) Zero output level: \( S_1, S_2, S_3, S_4, S_5 \) are OFF in the generation of zero voltage(0 level) is shown in Table 2.

2) \( V_{dc} \) output voltage level: \( S_3, S_5 \) are ON. All the other switches are OFF resulting in the generation of 1 \( V_{dc} \). Fig.10 shows the current paths that are active at this stage.

3) \( 2V_{dc} \) output voltage level: \( S_2, S_5 \) are ON. All the other switches are OFF resulting in the generation of 2 \( V_{dc} \). Fig.11 shows the current paths that are active at this stage.

4) \( 3V_{dc} \) output voltage level: \( S_1, S_5 \) are ON. All the other switches are OFF resulting in the generation of 3 \( V_{dc} \). Fig.12 shows the current paths that are active at this stage.
6.0 SIMULATION RESULTS FOR WITHOUT FILTER

To verify the proposed schemes, a simulation model for a single phase seven level Multilevel Inverter is implemented. Fig.13 and Fig.14 shows the output voltage of CSFMC-SH PWM with modulation index 1, fundamental frequency 50Hz and THD value is 26.97% with output voltage of 30V. Fig.15 and Fig.16 shows the output voltage of CSMC-SFO PWM and harmonic spectrum with modulation index 1. The THD value is 19.97% with output voltage of 30V. Fig.17 and Fig.18 shows the output voltage of VSFMC-SH PWM and harmonic spectrum with modulation index 0.8. The THD value is 17.15% with output voltage of 30V. Fig.19 and Fig.20 shows the output voltage of VSFMC-SFO PWM and harmonic spectrum with modulation index 0.8. The THD value is 16.33% with output voltage of 30V. Fig.21 and Fig.22 shows the output voltage of PSC-SFO PWM and harmonic spectrum with modulation index 1. The THD value is 15.26% with output voltage of 30V.
Fig. 14. THD of Constant switching frequency multicarrier sub harmonic pulse width modulation.

Fig. 15. Output voltage of seven level proposed multilevel inverter Constant switching frequency multicarrier switching frequency optimal pulse width modulation (CSMC-SFO PWM).

Fig. 16. THD Constant switching frequency multicarrier switching frequency optimal pulse width modulation (CSMC-SFO PWM).

Fig. 17. Output voltage of seven level proposed multilevel inverter Variable Switching Frequency Multicarrier Sub harmonic Pulse Width Modulation.

Fig. 18. THD of Variable Switching Frequency Multicarrier Sub harmonic Pulse Width Modulation.

Fig. 19. Output voltage of seven level proposed multilevel inverter Variable switching frequency multicarrier switching frequency optimal pulse width modulation (VSFMC-SFO PWM).
7.0 SIMULATION RESULTS FOR WITH FILTER

To verify the proposed schemes, a simulation model for a single phase seven level Multilevel Inverter is implemented. Fig.23 and Fig.24 shows only the output current of PSC-SFO PWM with modulation index 1, fundamental frequency 50Hz and THD value is 1.53% with output voltage of 30V. Simulation parameters of filters are Filter inductor L:5mH, Filter capacitor C:2µF.
6.0 COMPARATIVE RESULTS

In order to clarify the advantages and disadvantages of the proposed topology, it should be compared with the different kinds of topologies presented in this paper. In the comparison the number of switches, capacitor, Voltage sources are taken and tabulated in Table 3. The Table 4 shows the THD value using for without filter CSMC-SH PWM, CSMC-SFO PWM, VSMC-SH PWM, VSMC-SFO PWM and PSC-SFO PWM the THD values are reduced respectively. With different modulation index. The Table 5 shows the THD value using for without filter CSMC-SH PWM, CSMC-SFO PWM, VSMC-SH PWM, VSMC-SFO PWM and PSC-SFO PWM the THD values are reduced respectively. With modulation index is 1.

<table>
<thead>
<tr>
<th>Modulation index</th>
<th>CSMC-SH PWM THD</th>
<th>CSMC-SFO PWM THD</th>
<th>VSMC-SH PWM THD</th>
<th>VSMC-SFO PWM THD</th>
<th>PSC-SFO PWM THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>20.97</td>
<td>19.47</td>
<td>16.22</td>
<td>15.97</td>
<td>15.26</td>
</tr>
<tr>
<td>0.8</td>
<td>27.62</td>
<td>20.22</td>
<td>17.35</td>
<td>16.33</td>
<td>16.01</td>
</tr>
<tr>
<td>0.6</td>
<td>20.65</td>
<td>20.98</td>
<td>14.08</td>
<td>17.45</td>
<td>17.42</td>
</tr>
<tr>
<td>0.4</td>
<td>20.17</td>
<td>21.38</td>
<td>19.99</td>
<td>19.06</td>
<td>19.23</td>
</tr>
<tr>
<td>0.2</td>
<td>20.01</td>
<td>22.54</td>
<td>20.22</td>
<td>20.19</td>
<td>20.11</td>
</tr>
</tbody>
</table>

Table 4 Comparative Analysis of THD for proposed multilevel inverter using without filter.

<table>
<thead>
<tr>
<th>Multilevel inverter type</th>
<th>Proposed multilevel inverter using 5 switches</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage source</td>
<td>3</td>
</tr>
<tr>
<td>capacitor</td>
<td>-</td>
</tr>
<tr>
<td>switches</td>
<td>12</td>
</tr>
</tbody>
</table>

Table 3 Comparative of switching components.

<table>
<thead>
<tr>
<th>Modulation index</th>
<th>CSMC-SH PWM THD</th>
<th>CSMC-SFO PWM THD</th>
<th>VSMC-SH PWM THD</th>
<th>VSMC-SFO PWM THD</th>
<th>PSC-SFO PWM THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3.56</td>
<td>3.01</td>
<td>2.66</td>
<td>2.36</td>
<td>1.53</td>
</tr>
</tbody>
</table>

Table 5 Comparative Analysis of THD for proposed multilevel inverter using with filter.
8.0 CONCLUSION

In this paper, new topology 5 switches are introduced and the same 7-level output is observed in either of the cases and different types of PWM outputs are obtained. Circuits are simulated using MATLAB/SIMULINK software and Total Harmonic Distortions are obtained. It can be seen that the 5-switch topology is better than other presented topology because it requires a lesser number of switches and also THD content is lower in comparison with other mentioned method.

References


