Receiver Architecture and Implementation for Differential Offset QPSK

EMMANUEL FRANTZESKAKIS[*], ARIS POSONIDIS[*],CHRISTOS PAPATHANASIOY[**], and KONSTANTINOS ARETOS[***]
Transmission and Access Systems Department
[*]DSP Laboratory, [**]RF Laboratory, [***]IC Design Centre
Intracom S.A.
19.5 Km Markopoulou Ave., 190 02 Peania Attika
GREECE

Abstract: The Offset QPSK modulation has been adopted by a multitude of wireless digital transmission applications, with satellite communications being the most prominent one. Nevertheless, OQPSK is exclusively deployed with coherent reception because non-coherent or differentially coherent OQPSK reception techniques either exhibit unacceptable performance or require very high complexity receivers.

This paper is concerned with a novel differentially coherent receiver for Differentially encoded Offset QPSK modulation. This receiver consists of a bandpass demodulation structure followed by an eight-state Viterbi soft decision algorithm. The bandpass demodulator estimates a two-component I-Q output involving both inter-symbol interference and cross correlation leakage. The Viterbi algorithm is responsible for combining the available information in an optimal manner in order to estimate the received data. The VLSI architecture of this receiver is also discussed.

Utilizing 40000 gates in an FPGA, it is the first reported DOQPSK receiver hardware implementation. The prototype has been tested in a point-to-multipoint TDMA transmission system. It can accommodate transmission rates up to 4Mbit/sec. Its performance is comparable or supersedes the one of previously proposed non-coherent or differentially coherent OQPSK receiver structures, while keeping the implementation complexity considerably lower than the most efficient of these ones. Furthermore, the DOQPSK receiver under consideration performs marginally better than non-coherently detected p/4-DQPSK implying important consequences on the trade-off between power consumption and spectrum utilization.

Key-Words: Differential Offset QPSK, DOQPSK, differential demodulation, GMSK, Low BT , quadrature phase shift keying, differential phase shift keying, Viterbi algorithm, soft decision, mobile radio *CSCC'99* Proc.pp..4281-4285

1 Introduction

Two of the major factors characterizing the efficiency of modern wireless digital communication systems are the required bandwidth allocation and power consumption. Approximating a constant envelop characteristic, Offset Quaternary Phase Shift Keying (OQPSK) modulation allows the operation of power efficient low output back-off (OBO) or 1dB compression point power amplifier (PA) with the penalty of only a small spectral regrowth. Furthermore, an amplitude limiter can be used at the receiver side with negligible performance degradation. For these reasons, OQPSK modulation has been adopted by a multitude of wireless digital transmission applications, such as satellite communications. The use of a non-coherent or differentially coherent receiver structure eliminates the need of complex carrier recovery circuitry. At the same time, it implies an advantage on the speed of transmission link restoration, especially in communication over fading channels, and/or burst mode transmission systems such as the Time Division Multiple Access (TDMA) systems. This desired reliability feature can be achieved at the cost of some performance degradation in the signal-to-noise ratio (SNR) versus bit-error-rate (BER) curve, since the demodulation process is not aided by a stable carrier reference signal [1].

Specifically for the case of OQPSK though, inter-symbol interference (ISI) intervenes between the in-phase (I) and quadrature (Q) data streams if a non-coherent or a differentially coherent receiver scheme is used. Kaleh addresses this problem in [2]. Both baseband and bandpass implementations are considered. In the former, the receiver consists of a receiver filter incorporating a zero forcing equalizer followed by a complex correlator circuit. The later consists of the corresponding bandpass receiver filter followed by a

structure employing Hilbert transform, lowpass filtering and down-conversion. This can be simplified to a cascade of receiver filtering, real correlation and lowpass filtering, provided that the correlation lag *D* and the bandpass frequency f_0 satisfy the relation

$$exp(j2pf_0D) = j \; . \qquad (1)$$

Kaleh's receiver structure has been supplemented in [3] with a 2-state Viterbi algorithm appropriate for differential decoding and decision making. Simulation of these two structures has shown a 1.5dB SNR-BER performance improvement of [3] over the receiver in [2]. A different approach is adopted by Gunther et al.[4]. A square root raised cosine receiver filter is used, followed by a complex correlator and a 16-state Viterbi algorithm (VA) appropriate for differential encoding, ISI compensation and decision making. The 16-state VA undertakes the equalization procedure, thus it eliminates the need of the zero-forcing equalizer, while at the same time a 1.5dB SNR-BER performance improvement over the receiver in [3] is obtained. No training is needed for the VA, since perfect Nyquist filtering is considered and therefore the expected receiver values can be computed algebraically. Nevertheless, the required computational complexity is considerably higher than the one of [3].

The DOQPSK receiver introduced in this presentation achieves a performance as good as the one of [4], while it requires less than half its computational complexity. The rest of the paper is organized as follows. In Section 2, the demodulation structure and the Viterbi algorithm are described. In Section 3, implementation issues and performance evaluation results are given. Our work is concluded in Section 4.

2 Differentially Coherent OQPSK Demodulation and Decision Making

Consider the bandpass demodulation structure presented in Figure 1, that consists of a pair of real correlators differing by a lag equal to half the bit period *T*, followed by a pair of low-pass filters. We assume that the relation (1) between the correlator lag *D* and the intermediate frequency (IF) f_0 is satisfied. The lowpass filters are raised cosine filters. A bandpass receiver filter should precede this structure that simply serves the purpose of channel separation and harmonic suppression. Unlike the one in [2] it does not need to be a matched filter or incorporate a zero forcing equalizer. The resulted observation statistic is a two element X-Y vector with eye diagrams depicted in Figures 2 and 3.

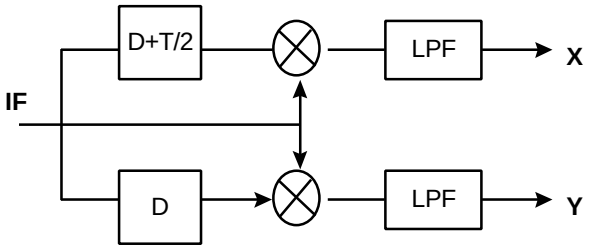

Fig. 1. Bandpass DOQPSK demodulator

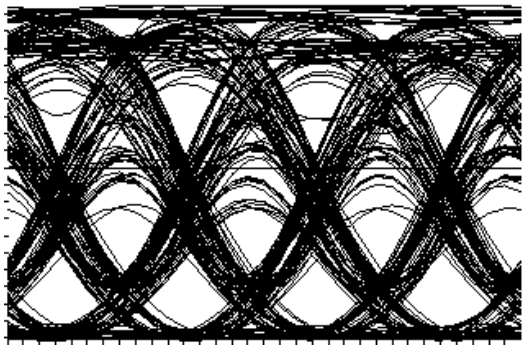
Fig. 2. X-eye diagram

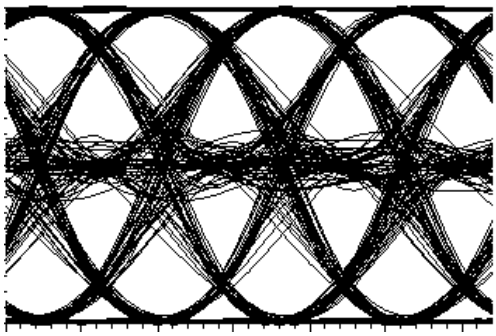
Fig. 3. Y-eye diagram

These diagrams clearly show an inter-symbol interference (ISI) spanning at least across three consecutive receiver samples. Since differential encoding is used in the transmitter, we conclude that a quadruple of transmitted bits is necessary to determine the value of the associated receiver statistic. Therefore, if a Viterbi algorithm (VA) is used for equalization and decision making there will be 16 different metrics to be calculated at each step, and consequently an 8-state Viterbi algorithm will be needed. Theodoridis et al.[5] provide the necessary background for characterizing the appropriate Viterbi algorithm.

Training can take place off-line or in real time and amounts to the computation of the 16 points of gravity $(g_{i,X}\ ,\ g_{i,Y})$, $i=0,1,\ldots,15$, in the 2-dimensional observation space associated to the 16 possible binary quadruples. During run-time the trellis diagram in Figure 4 is realized. The Euclidean distances between the receiver statistic and the 16 centres of gravity are used as the VA metrics:

$$metric_i(X,Y)=(X-g_{i,X})^2+(Y-g_{i,Y})^2, \quad i=0,1,\ldots,15. \qquad (2)$$

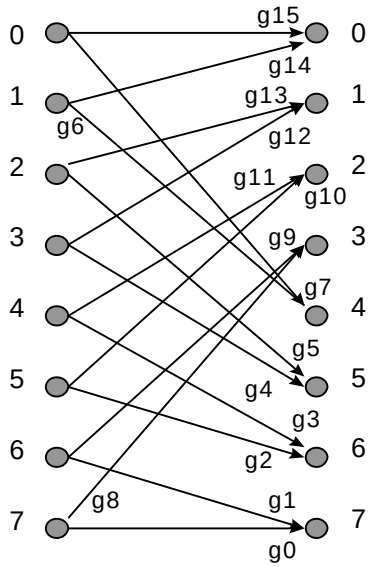

Fig. 4. Trellis diagram

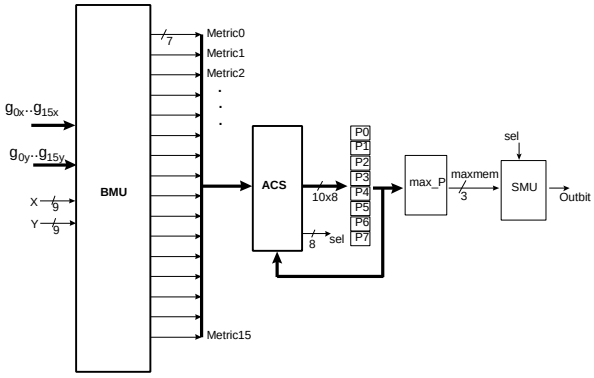

Fig. 5. Viterbi architecture

The block diagram of the Viterbi architecture is shown in Figure 5. Three main units are involved [6]. First, the Branch Metric Unit (BMU), which based on the received noisy symbols, evaluates the quantities in equation (2). Second, the Add-Compare-Select units (ACS), which recursively compute the path metrics P by adding the appropriate branch metrics to the old path metrics of the competing paths, comparing and consequently selecting the survivor paths. Third, the Survivor Memory Unit (SMU) that maintains the surviving sequences dictated by ACS and is responsible for extracting the decoded symbol. The surviving paths merge with high probability when traced backward, so SMU uses this property in order to find the decoded symbol by using finite memory depth. Controlling the trade-off of area efficiency versus throughput can be achieved with numerous techniques (cf. [7] for ACS and [8] for SMU).

3 Implementation Issues, Performance Evaluation and Scope

The DOQPSK receiver structure described in the previous section has been applied for the physical layer implementation of a point-to-multipoint time division multiple access (TDMA) system, able to accommodate transmission rates up to 4Mbit/sec. The flow diagram of the radio is depicted in Fig. 6.

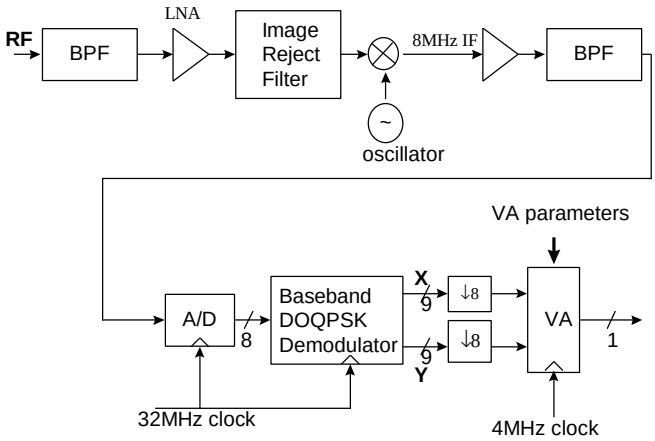

Fig. 6. DOQPSK receiver flow diagram

The input signal is a radio frequency (RF) modulated carrier. This RF signal passes through a channel separation filter, it is amplified by a low noise amplifier (LNA) and then filtered again in order to have the amplified image rejected. Using a free running oscillator the signal is down-converted to an intermediate frequency (IF) equal to 8MHz, that is twice the transmission bit rate. A second stage of amplification as well as another bandpass filter used for harmonics suppression and antialiasing purposes follow. The later has cut-off frequencies at 6MHz and 10MHz. A high speed analogue-to-digital converter (A/D) capable of providing 32Msamples/sec is required for the digitization of the IF signal. The bandpass demodulator operates at 32 MHz. Consequently, the bit period in terms of the circuit clock period takes the value $T=8$. The parameter D shown in Figure 1 is assigned the value $D=9$. One can easily verify that relation (1) is then satisfied. The lowpass filters are implemented as root raised cosine filters with rolloff factor equal to 1. The choice of these filters is appropriate if the same filters are used for pulse shaping at the transmitter side. Downsampling of the demodulated signal by a factor of 8 allows the VA to operate at bit rate. The VA is characterised by the trellis diagram specified in Figure 4, while the mapping of the VA on VLSI architecture is shown in Figure 5. When implemented on ASIC or

FPGA, the computational complexity of the Viterbi decoder alone is approximately 15000 gates.

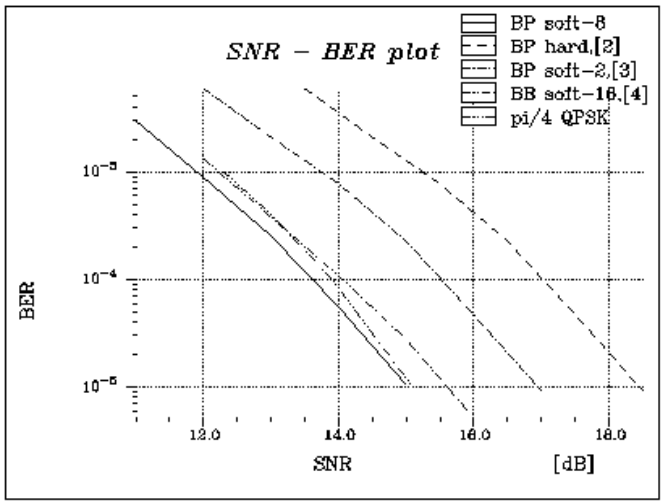

Fig.7. SNR-BER plots

The resulted SNR-BER curve is shown in Figure 7. This is compared to simulated single-branch demodulators using either hard decoding [2] or 2-state soft decoding [3]. We observe a 3.5dB improvement with respect to the first one and a 2dB improvement with respect to the second one. The SNR-BER curve of the baseband receiver proposed by Gunther et al. [4] exhibits a degradation of approximately 0.5 dB compared to ours. Furthermore, [4] requires a complex multiplication instead of two real multiplications and a 16-state Viterbi algorithm instead of an 8-state one. This implies more than twice the computational complexity required by the DOQPSK receiver presented in this work. In Figure 7, the SNR-BER curve for non-coherently detected p/4-DQPSK [1] signaling is also shown. We observe that the proposed DOQPSK receiver has a marginally better performance than the one of p/4-DQPSK.

The DOQPSK receiver structure discussed so far can also be applied for differential coherent reception of all OQPSK compatible modulation schemes. These are modulation schemes which can be coherently demodulated by an ordinary OQPSK coherent demodulator. Examples of such schemes are the IJF-OQPSK [9] and FQPSK [10].

Flexibility is an important advantage of the proposed receiver structure. Since the training of the adopted Viterbi algorithm, does not require any assumptions on transmitter or receiver filters, unlike the one in [4], the overall structure is very flexible and its performance can be optimized for the choice of specific receiver filters, channel bandwidth constraints and/or the use of non linear reception, such as amplitude hard limiting, resulting a negligible performance degradation. Finally, the VA offers the possibility of real-time adaptation, thus increasing robustness in data transmission over time variable channels, such as the fading channels.

4 Summary and Comments

This paper presents a differentially coherent receiver architecture for Differentially encoded Offset QPSK consisting of a two branch bandpass demodulator followed by an eight-state Viterbi soft decision algorithm. Its performance supersedes previously proposed non-coherent or differentially coherent OQPSK receiver structures [2],[3],[4], while it keeps complexity requirements low. This architecture has been implemented on ALTERA10K70 FPGA, it requires approximately 40Kgates and can accommodate transmission rates up to 4Mbit/sec. Its performance has been tested and verified by integration in the physical layer of a TDMA point-to-multipoint transmission system.

The SNR-BER performance curve of our DOQPSK receiver is marginally better than the one of non-coherently demodulated p/4 DQPSK. Therefore, this DOQPSK receiver shares a combination of advantages enjoyed by OQPSK systems, such as using power efficient low output back-off or class C power amplifiers with band-limited transmission and the advantage of efficient non-coherent reception offered by p/4 DQPSK systems.

Experiments that are not reported in this brief presentation show improved robustness against co-channel and adjacent channel interferences compared to other DOQPSK receivers and p/4 DQPSK. Another issue not addressed here is the ability of the presented receiver to function as a very efficient demodulator for low BT GMSK modulated signal.

References:

[1] L.E.Larson, *RF and Microwave Circuit Design for Wireless Communications*, Artech House, 1996.

[2] G.K.Kaleh, "A Differentially Coherent Receiver for Minimum Shift Keying Signal", *IEEE Journal on Selected Areas in Communications*, Vol. 7, No 1, pp.99-106, Jan. 1989.

[3] G.K.Kaleh, "Differential Detection via the Viterbi Algorithm for Offset Modulation and MSK-Type Signals", *IEEE Trans. On Vehicular Technology*, Vol. 41, No 4, pp. 401-406, Nov. 1992

[4] C.G. Gunther and J. Haberman, "DOQPSK-differential demodulation of filtered offset QPSK",

IEEE 44th Vehicular Technology Conference Proceedings, vol. 3, pp.1542-1546, 1994.

[5] S.Theodoridis, C.F.N.Cowan, C.P.Callender, C.M.S.See, "Schemes for equalization of communication channels with nonlinear impairements", *IEE Proceedings on Communications*, Vol.142, No 3, pp.165-171, 1995.

[6] S.B.Wicker, *Error Control Systems for Digital Communications Storage, Prentice Hall*, 1995.

[7] Fetweis G. and Meyr H. "Parallel Viterbi algorithm implementation: Breaking the ACS-bottleneck". *IEEE Trans. Commun.*, Vol.37, No.8, pp.785-789, 1989.

[8] Black P.J. and T.H. Meng T.H. "A 140-Mb/s, 32-state, radix-4 Viterbi decoder". *IEEE J. Solid-State Circuits*, Vol.27, No.12, pp.1877-1885, 1992.

[9] H.Mehdi and K.Feher, "FQPSK, Power and Spectral Efficient Family of Modulations for Wireless Communication Systems", *Proceedings of the 44th IEEE Vehicular Technology Conference*, vol.3, pp.1562-1566, 1994.

[10] T.Le-Ngoc, K.Feher and H.Pham-Van, "New Modulation Techniques for Low-Cost Power and Bandwidth Efficient Satellite Earth Station", *IEEE Trans. On Communications*, vol.30, pp.275-283, Jan.1982.