Building block specifications for multi-mode receiver

K. GALANIS[1], A. PNEUMATIKAKIS[1], L. DERMENTZOGLOU[1],
A. ARAPOYANNI[2] and I. MOISIADIS[1]

[1]Integrated Systems Development
22, K. Varnali str., 15233 Xalandri, Athens
GREECE

[2]University of Athens, Dept. of Informatics
Panepistimiopolis, 157 84 Athens
GREECE

Abstract: - This paper describes the simulation procedure of a heterodyne receiver capable of multimode operation. The receiver consists of a head filter, an LNA, an image rejection mixer, two IF filters and an IF amplifier. The overall receiver performance was evaluated in terms of Noise Figure, Intermodulation, blocking requirements, SNR, and BER. The accomplishment of the most demanding system specifications is the key parameter for succeeding tri-band operation (GSM/DCS1800/PCS1900). The receiver achieves an overall noise figure of 8.8 dB, input intercept point of –4 dBm and image rejection greater than 61 dB. The main objective is the extraction of feasible building block specification in order to operate for all the GSM-like standards.

Key Words: - RF Receivers, wireless communications, Intermodulation, SNR, C/I, Image rejection, BER

1 Introduction

Cellular phones designers face increasing pressure to design smaller, lighter and less expensive phones. In the same time the globalization of telecommunications leads to more advanced structures, capable of operating almost everywhere in the world [1, 2]. Today's leader in the telecommunication market, GSM and its variants, cover almost 90% of cellular communication demands. Hence multi-mode phones are of increasing importance.

Since cost constitutes one of the most critical aspects, heterodyne receivers become more and more popular [8, 9]. Such a topology, when compared to the superheterodyne architecture, reduces the number of local oscillators, mixers, amplifiers and filters needed, thereby minimizing current consumption and spurious signals. The combination of simplicity, reliability and decreased hardware make this type of receivers an attractive choice, especially since direct down conversion presents problems like the local oscillator leakage to the antenna, the instantaneous dynamic range requirements at the input and the dc offset [2].

The proposed architecture is the single down conversion low IF. The goal is to translate the system specifications [3, 5] into feasible building block specifications and to optimize the overall RF architecture according to this. The results can be utilized to drive the building block design and to evaluate the silicon implemented designs.

This paper analyses receiver architecture for GSM-like standards. The main objective is to determine the performance required for the different receiver building blocks, keeping in mind the state-of-the-art in components. Optimization is carried out in order to ensure realistic designs. The receiver performance is evaluated by simulation and is compared to the GSM specifications.

This paper is organized as follows: In section 2 the overall RF specifications are determined according to international standardization organizations. In section 3 the proposed architecture is presented and analyzed. Then, in section 4 the simulation methodology and results are presented, leading to the optimized receiver chain. Finally, in section 5 the conclusions are drawn and feasibility results are presented.

2 System Requirements

Complying with the GSM/DCS/PCS specifications, basic radio performance requirements such as noise figure (NF), third order input intercept-point (IIP3), local oscillator (LO) phase noise, carrier to interferer ratio (C/I) and bit error rate (BER) requirements must be met [3]. Since the receiver is optimized for multimode operation, it is enough to meet the most demanding standard's specifications.

These are derived using the co-channel and adjacent channel rejection and the blocking requirements [5].

Table 1: Multi-mode receiver performance goals.

NF	<9dB
IIP3	-9dB
LO phase noise	-141dBc/Hz
C/I	>12dB
BER	$<10^{-3}$
Image Rejection	68dB

The receiver should handle large blocking signals while receiving a wanted signal at -99 dBm. The maximum in-band and out-of-band interferers are -23 dBm and 0 dBm respectively. The image rejection requirement is defined considering the image as an out-of-band spurious signal at the power level of –43dBm [3].

3 Single down conversion receiver

The proposed receiver architecture is the single down conversion low IF and its block diagram is depicted in Fig. 1.

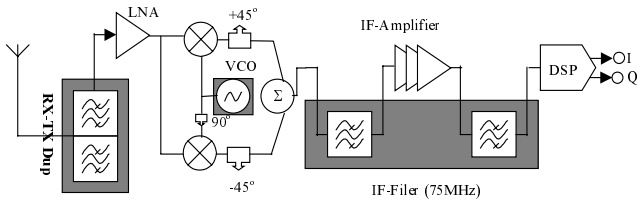

Fig. 1: Block diagram of the receiver.

The RF section comprises a RF filter, a LNA and a doubly-balanced image rejection mixer. The RF filter and the LNA provide the RF selectivity, and together with the IR mixer, the image rejection. This joint provision of the image rejection allows the relaxing of the phase and gain matching requirements of the mixer. The LNA and the active mixer provide the necessary gain at the RF, to ensure the wanted noise performance. The mixer down-converts to the relatively low IF of 75MHz. At this frequency the filtering requirements are relaxed and the final down conversion to base-band does not require prohibitory increased power dissipation from the A/D converter. The IF stage comprises two IF filters and an AGC amplifier. The two filters provide the IF selectivity, as determined by the adjacent channel rejection requirements, i.e. they perform channel selection and anti-aliasing (since sub-sampling is used). They are positioned one before the AGC to reduce its linearity requirements and the other after the AGC to account for the harmonics it generates. The AGC provides the necessary IF amplification and power adjustment.

The main advantage of the single down conversion-low IF architecture is the use of only one down-conversion stage. This makes the receiver blocking and noise performance easier to meet, especially for aggressive specifications like those of GSM, and reduces power consumption. IF sampling allows the final conversion to base-band to be carried out digitally, adding flexibility. The combination of the front end and IR mixer for image rejection reduces the matching requirements of the latter. Finally, the strict IF filtering reduces the linearity requirements of the AGC and the dynamic range requirements of the ADC.

On the other hand, the three required filters and the strict IF filtering are the inconveniences of the single down conversion receiver, since the choice of non-integrated filtering devices seems unavoidable. Finally this kind of structure is highly demanding for linearity in the IF stage.

Table 2: Multi-mode filtering requirements

Filter	Parameter	Value
E-GSM RF	Passband	925-960 MHz
	Insertion loss	4.3 dB
	PB ripple	2.6 dB
	Attenuation	28dB @ f<905 MHz 20dB @ f<915 MHz 23dB @ f>980 MHz
DCS1800 RF	Passband	1805-1880 MHz
	Insertion loss	2.7 dB
	PB ripple	1.7 dB
	Attenuation	20dB @ f>1785 MHz 10dB @ 1920<f<1980 MHz 21dB @ 1980<f<3500 MHz
PCS1900 RF	Passband	1930-1990 MHz
	Insertion loss	3.2 dB
	PB ripple	1.8 dB
	Attenuation	30dB @ f<1800 MHz 25dB @ 1850<f<1910 MHz 16dB @ 2010<f<2090 MHz 33dB @ 2160<f<2230 MHz 28dB @ 2100<f<2150 MHz 30dB @ f>2240 MHz
IF Filter (common)	Passband	75 MHz±100kHz
	Insertion loss	6.8 dB
	PB ripple	1.5 dB
	Attenuation	4dB @ ±200kHz 26.1dB @ ±400 kHz 36.9dB @ ±600 kHz 40.3dB @ 1.8<f<3.0 MHz

The filters for the multi-mode operation of the chain (see Fig. 1) are summarized in Table 2. These are state-of-the-art non-integrated filters [7]. No optimization of their behaviour is attempted, as this would increase the cost, volume and power consumption of the handset. Only the rest of the receiver chain is optimized in the next section to allow for the wanted performance given the filters.

4 Optimization of the Receiver Chain

Simulation has been used for the optimization of the receiver chain. For this, MATLAB has been employed. The various building blocks have been described using non-ideal models that include non-linearity, noise figure, bandwidth of operation and insertion loss. Additionally, the model of the IR mixer includes phase and gain mismatches as well as LO phase noise. Furthermore, for BER measurements, the complete GMSK modem has been setup.

The goal of the simulation process is the optimization of the receiver chain that is oriented to multi-mode operation, i.e. the transition from the strict specifications dictated by the driver standards [3, 5], to more feasible specifications that actually comply with these standards. The result of this process is a set of building block specifications to be used by the silicon designer. These building block specifications, although they impair the performance of the receiver, they are feasible and allow the correct operation of the receiver, as it is evaluated by C/I and BER measurements. An example of this is the allowance of non-linearity that leads to gain compression, as long as the C/I remains above 12dB.

The receiver has been subjected to tests that include out- of-band and in-band (adjacent channel) interferers and imager. The resulting performance is summarized in Table 3. Also the optimized building block specifications are shown in Table 4.

Table 3: Summary of measured results of receiver.

C/I	12.5	dB
Overall receiver Gain	18-38	dB
NF	8.8	dB
BER	10^{-3}	
Image Rejection	≈61	dB

In Fig. 2 the capability of the receiver to reject gradually an adjacent channel interferer of –33 dBm at 600 kHz offset from the –82 dBm GMSK modulated useful signal is presented, keeping the C/I criterion well above the 12 dB.

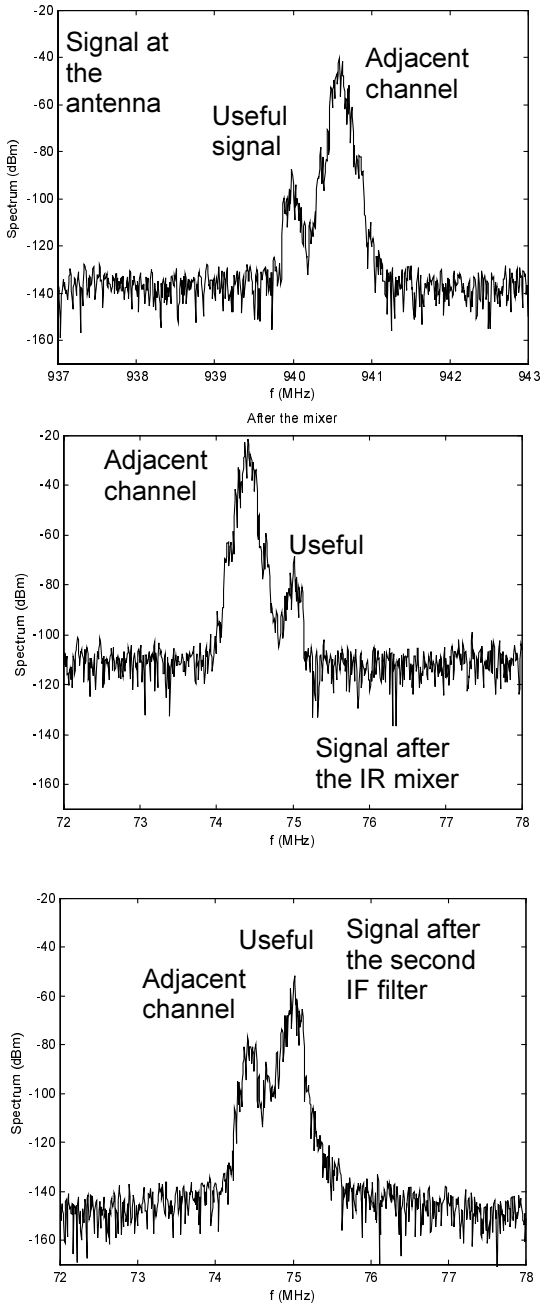

Fig. 2: Adjacent channel test results

According to the specifications tables 2 and 4, it is obvious that the use of multiple dedicated head filters and LNAs is unavoidable. Alternatively, tunable bandpass filters and wide-band amplifiers can be used, but their performance is limitted regarding tunability, rejection factors and dynamic range.

The IIP3 of –4 dBm guarantees that the C/I remains above 12 dB, although this figure imposes approximately 0.2 dB of compression in the LNA. Consequently further reduction of the mixer's IIP3 (5 dBm) by using non matched figures ($IIP3_{mixer} \langle IIP3_{lna} + Gain_{lna}$) produce further gain compression of 0.1

dB. This guarantee a feasible linearity requirement for the active mixer while simultaneously does not have a bad impact on the overall receiver performance.

Table 4: Optimized building block specifications.

BB	Parameter	Value	Unit
LNA	Input freq.	925-960 1805-1880 1930-1990	MHz
	Power gain	15	dB
	NF	2	dB
	CP 1dB	-14	dBm
	IIP3	-4	dBm
IR mixer	IF	75	MHz
	Power gain	8	dB
	NF	10	dB
	CP 1dB	-20	dBm
	IIP3	5	dBm
	Image rejection	31	dB
	Gain mismatch	0.5	dB
	Phase mismatch	2	deg
LO	Freq. Range	1000-2065	MHz
	Freq. step	1	kHz
	Phase noise	-71 @ ±200kHz -103 @ ± 400kHz -111 @ ± 600kHz -121 @ 0.6<f-f_o<0.8MHz -121 @ 0.8<f-f_o<1.6MHz -131 @ 1.6<f-f_o<3MHz -141 @ 3MHz<f-f_o	dBc/ Hz
IF amplifier	Input freq.	75	MHz
	Power gain	12 to 32	dB
	NF	16	dB
	CP 1dB	-4	dBm
	IIP3	6	dBm

The resulting NF is 8.8 dB. Further reduction of the NF is not pursued due to the NF - gain tradeoff of the LNA.

Finally, the achieved image rejection is around 76 dB for EGSM, 66 dB for DCS1800 and 61 dB for PCS1900 respectively. These figures are the sum of the image rejection provided by the head filter and mixer (31 dB constantly [6]), as well as the rejection provided by the RF amplifier. Due to image positioning (lies in any case 2IF MHz beyond carrier frequency) the RF amplifier reduces its gain around 6dB/octave. In conclusion, its contribution to the overall image rejection performance of the front end is approximately 10 dB.

5 Conclusions

In this paper, receiver architecture suitable for multi-mode operation is presented, and the specifications that are dictated using the GSM-like standards as drivers are considered. Then, using simulation, the optimal building block specifications are derived. These specifications allow the operation of the receiver according to the standards and are feasible both in terms of cost and integration.

The receiver under study was found to operate apropriately for the tri-mode, allthough a trade off between linearity and reliability has been accounted. The extracted building block specifications were optimized in terms of feasibility results for CMOS or BiCMOS realization.

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