A Current-Path Based Placement Methodology for Analog IC Layout Design

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Abstract: - In this paper, we present a transistor placement methodology for CMOS analog integrated circuit that leads the subsequent phase to conform to analog layout constraints, such as: matching, symmetry, signal coupling and geometric constraints such as: cell aspect ratio (or cell height), and user-defined cell input/output pin locations. This placement methodology bases on the characteristics of current paths and the layout constraints can help us to obtain better performance, that is guaranteed by experimental results.

Key-Words: -Analog layout, placement, slicing, current-path, design automation

1 Introduction

Signals in the real world are analog in nature and all interface circuitry require analog parts. Many CAD tools and algorithms can synthesize and generate layouts for the digital parts of such chips. The complexity and variability of analog layout are more difficult than the digital layout problem. Those layout constraints include matching, symmetry, limited parasitic and signal couplings [1-3], and also the geometric restrictions on cell aspect ratio (or cell height) and I/O pin locations.

Some ideas from digital design methodologies, such as standard cell library [4] and cell generators, have recently been applied to analog design. However, in the analog world it is difficult to build a rich enough set of library cells to support the wide spectrum of possible applications. Furthermore, analog cell libraries become obsolete quickly as technology or design rules change.

In ILAC [8], cell generation is emphasized; analog routing is considered a secondary issue. It is infeasible to complete a symmetry routing for a bad symmetric placement. OPASYN [6] uses accumulated design experience to partition an analog circuit into a slicing tree. Even the use of shape function achieving better matching on cell aspect ratio, the limitations of the design experiences on special circuits make it difficult for the cell generator to be applied to a general circuit. The usage of a general slicing tree structure [5-6] and [7] usually bring a bad symmetric placement that makes it infeasible to complete a fully symmetry routing.

In this paper, we propose an analog CMOS placement methodology that leads the subsequent phase to conform to analog layout constraints. Slots of current path are extracted from the circuit, so that it will not bring coupling easily, and the routing will be produced symmetric. The top-down partition and bottom-up placement make every device has its own space to place. The layout of a chip won't be out of shape, because we can adjust every device slightly instead of modifying the whole chip by a wide margin. Since the locations of devices on the layout floor are similar to arrangement in associated schematic, we can recognize and detect mistakes efficiently. It will be subservient to construct an analog CMOS automatic layout generator.

2 The proposed methodology

In this section we give a detailed description of our placement methodology for analog CMOS layout design. It consists of seven steps such as estimating the total chip area, choosing aspect ratio, extracting current branch from circuit, adjusting current branch to be in position, transferring the slot structure into slicing tree, top-down partition and bottom-up placement.

2.1 Preliminary Process

Before taking proceeding, we calculate the approximate area and determine the aspect ratio of the chip and hope that the final result of placement will approach the size we get in preliminary process.

Step1 Estimating the total chip area

The unit device area is defined as the sum of the unfolded device area plus the source and drain contact area. To obtain the device area, should be multiplied by the effective gate area, *WL*, where *W* is the gate width and *L* is the effective gate length. And the source and drain contact area *C* is given by

$$C_i = W \times (C_e + C_p + C_o) \times 2 \qquad (1)$$

where C_e is the square root of contact area, C_p and C_o are the distance from contact to poly and oxide definition.

The whole cell area *A* is the sum of each unit device area plus an additional *k* percent area for routing. We get the whole cell area *A* by the formula under mentioned:

$$A = \left\{ \sum_{i=1}^{n} (W_i \times L_i + C_i) \right\} \times (1 + k) \qquad (2)$$

Step2 Choosing aspect ratio of chip

We can choose a suitable aspect ratio of chip. By way of illustration, if the height *H* and the width *W* are in the ratio 1:2, and the total area of chip is A, then we can obtain the relationship between *H* and *W* easily

$$W = 2H = 2 \times \sqrt{\frac{A}{2}} \qquad (3)$$

2.2 Main loop of placement

After determine the size of chip, we begin to approach the subsequent process of partition and placement.

Step3 Extracting current branch from circuit

A current branch [1] is a current path between the two power rails, namely Vdd and Vss. Current branches can be extracted from Vdd to Vss through diffusion. A complete current branch is named as a 'slot'. From the schematic as shown in Fig. 1, we extract current branches as shown in Fig. 2. Current branches are recognized first and are used afterwards to recognize the other structures.

Step4 Adjusting current branch to be in position

The set of current branches generate in step3 is rough, and it is necessary to adjust current branches to be in position.

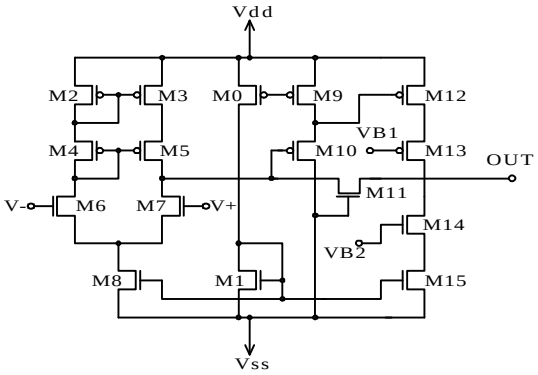

Fig.1 The voltage-controlled oscillator.

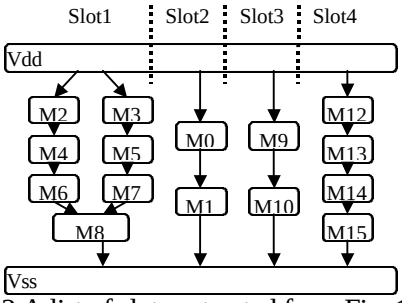

Fig.2 A list of slots extracted from Fig. 1.

The input wires of the differential pair require a fully symmetric placement and routing to reduce offset voltage [4]. Symmetric current branches prefer symmetric layouts in case not bring the other cost too high. The two *current-blanches* of the symmetry line involving the differential pair are served as a cell kernel that other symmetric current branches are placed around the cell kernel according to their connectivity. A current branch including the node of output signals should be move to the dextral border away from the input differential pair to avoid undesirable coupling between critical signal nets. Otherwise, the large changes in the output signal may be coupled into the input, resulting in undesired feedback. Other slots of current branch are rearranged with the minimum number of signal interconnection. If a unit device is out of a current branch, we merge it into the slot which device's drain connect with. Besides, we integrate two current branches into a slot when devices are matched. After adjust current branches to be in position, we can create a complete list of slots with devices.

Step5: Transferring the slot structure into binary tree

The brand-new list of slots with devices will be transfer to a different mode. Now we construct a binary

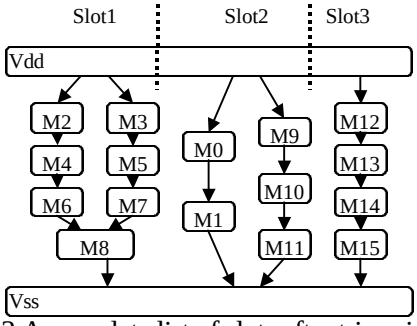

Fig.3 A complete list of slots after trimming.

tree, and all the devices in the list of slots are the members of leaves. The nodes in the structure of binary tree are the connecting type of their two children. If children connect in series, the node is denoted as '--' ; oppositely, the node is denoted as ' | ' if children connect in parallel. The right child must be nearer to the *VDD* than the left child or on the right side of the left child. Propose to combine all the devices into a structure of binary tree in order of precedence as listed below:

1. Devices are the same type and size, and have common drain (or source) and common gate
2. Devices are the same type and size, and have common drain (or source)
3. Devices are the same type and size, and have common gate
4. Devices are the same type and size
5. Devices are the same type

In conformity with preceding rules, we transfer the slot structure (Fig. 3) to a binary tree in Fig. 4.

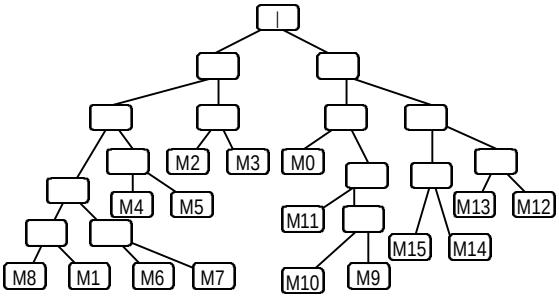

Fig.4 The binary tree transferred from Fig. 3.

Step6: Top-down partition

We already calculated the approximate area *A* of the chip in step1. Referring to the structure of binary tree, we compute the area of right child and left child of root respectively by summing up unit device area of all devices included in it. From the area of right child and left child of root, we find the ratio of right child to left child. Subtract the lacy zone reserving for channel routing from the total area of chip, we apportion the rest between right and left child by the ratio of them. Concurrently, we divide the chip into two proportioned parts. Repeat the process to acquire dimension of each child iterative until the child is the leaf of the tree, too. After top-down partitioning, every device gets its own space for the following placement.

Step7: Bottom-up placement

According to the size of the space prepared for every device in previous step, we adjust the figuration of layout to fit it, and sometime it is necessary to fold the device to seek better aspect ratio. Calculate the layout area of every device adjusted, and start to place from the left leaf of the binary tree. We incorporate one child with another to obtain a combined range. We define the width of combined range as the wider one of two children, and the length as summation of lengths of children when they connect in series. Besides, we define the width of a combined range as summation of widths of two children, and the length as the longer one of children when they connect in parallel. Execute the aforecited procedure recursively, we'll achieve the bottom-up placement easily.

3 Experimental results

Based on the methodology of placement described in this paper, we implemented the placement for the voltage-controlled oscillator shown in Fig. 5.

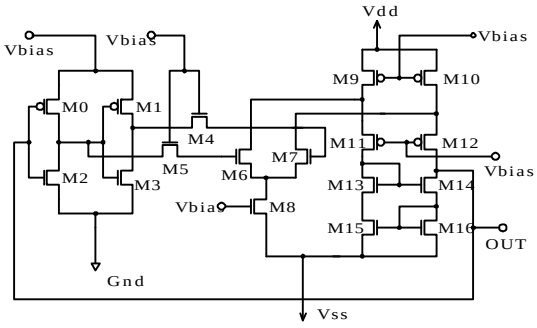

Fig. 5 The voltage-controlled oscillator

Now, we approach the methodology of placement step-by-step. When choosing the constant *k* of (2) to be 0.4, we compute the area of devices singly. The approximate area of total chip we calculate is 2925.51ì m^2. Since the aspect ratio of the chip is expected to be 1 to 1, we estimate the final area of the chip is 2970.25ì

m^2, and the length of the chip is 54.5 micrometer. After taking previously process, we'll start to execute the main loop of placement.

Conforming to the rules of our placement methodology, we obtain a complete list of slots with devices shown in Fig. 6. From the ensuing procedure, a graph of the top-down partition and another graph of the bottom-up placement eventuated, and were shown in Fig. 7 and Fig. 8. Finally, we derive the total area of the chip as 3003.90ìm^2, and the aspect ratio of the chip to be 1 to 1.05.

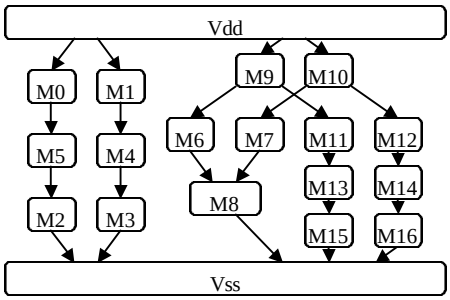

Fig. 6 The list of slots with devices.

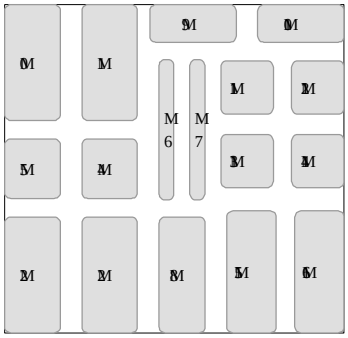
Fig. 7 The graph of the top-down partition

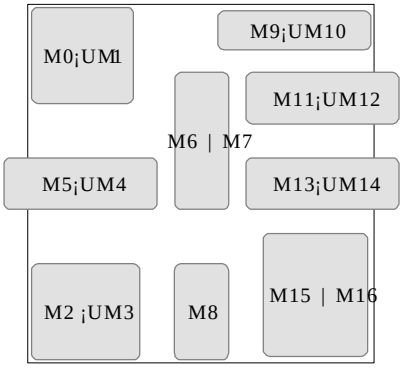

Fig. 8 The graph of the bottom-up placement

4 Conclusions

In this paper, we have presented a new placement methodology for analog CMOS layout design. The objective of the placement methodology is to achieve better matching and symmetry expectably, and to prevent layout from signal coupling and parasitic. It has been accomplished since our placement basing on the characteristics of current paths and the layout constrains.

The methodology we proposed can reduce the waste of space on chips, shorten design time, and contribute to improve the performance of analog CMOS layout design. On the side, experimental results have shown our methodology produced placement that can control the size and aspect ratio of chips with errors less than 1.13 and 15 . The foregoing will be subservient to construct an analog CMOS automatic layout generator.

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