A Mathematical Analysis of Analog and Digital summation techniques in compensation Block for I/O Buffers

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ABSTRACT

Compensation circuits have been employed in the o/p buffers to compensate for the effects of the mobility, threshold voltage and other parameters variations with the change in the PVT conditions. The aim is to optimize the performance of the o/p buffer in terms of the parameters namely the frequency of operation, current slew and the o/p-drive. For the change in PVT (Process, Voltage, Temperature) conditions the current in the p-mos and n-mos transistors vary independently. A compensation code is supplied to both n-mos and p-mos transistors to optimize the performance. In this document a comparison of two techniques namely Analog and Digital summation has been presented which are employed to produce a seven bit code for controlling the operation of the circuit by setting the aspect ratios of the pre-driver and the o/p buffer. A statistical approach has been taken to augment the empirical relations to reach at a best optimized solution for generating the codes.

Terms used: *Iref(the reference current generated in compensation block to be compared with Isat to generate the seven bit code),I_{r0} the value of Iref at typical PVT conditions, Iqn/p(the quantized value of the saturation currant in the n-mos/p-mos transistor) .kn/p denotes their respective process parameters and Weqi, Weqo denoting the equivalent Widths of the pre-driver and the o/p buffer section as a function of the code. Iref can vary in the positive and the negative directions with the y% and z% variation respectively i.e. it can vary from $I_{r0}(1-z/100)$ to $I_{r0}(1+y/100)$with a uniform probability.*

1. INTRODUCTION

In an I/O cell various quantities have to be optimized to interface the core to the o/p world and guarding against noise and excess charge etc to damage the core or the signals through which it is interfaced to the o/p world .To operate the cell under various PVT conditions we have to make sure that certain parameter constraints are satisfied for the proper operation. For this we employ the compensation circuitry to compensate the effects of mobility and threshold variation with temperature, process and voltage variations. To this effect a compensation code is supplied to a pre-driver as well as the o/p buffer so that our o/p buffer can perform at its best. The quantities that are to be optimized are namely

1. Current Slew $(di/dt)_{max}$
2. O/P drive i.e. the o/p impedance
3. Frequency of operation

By "best performance" it is meant that to be operating at the maximum frequency, the slew should be below a certain value as more slew (current) causes more noise at the o/p pad as this contributes a noise due to the parasitic inductance of the pad. The o/p impedance should be matched to the external world i.e. a constant to avoid the reflections. To generate the compensation code (7 bits) the unit saturation current I_{sat} at any particular PVT is compared to I_{ref} the reference current at the typical PVT conditions and the magnitude of the error dictates the codes .The reference current and the unit saturation current depending on the PVT conditions are generated(refer [3],[4],[5]) in the compensation block itself where they are compared by a flash comparator circuit to generate a seven bit code. The number of transistors switched on in the pre-driver circuit and the o/p buffer depends on the code generated.

Presented below are some guidelines that form the basis of the analysis in the following sections:

1. The variation in the saturation current due to the parameters like mobility and the threshold voltage for the n-mos and the p-mos transistors can be up to 150% i.e. to be more explicit the assumption is that the currents in the n-mos and p-mos vary independently of each other following a uniform probability distribution in their respective range of variations
2. At a time only one of the parameters influence the change in the absolute value of the current but in actual case both vary in the same directions to drift the current in the opposite directions by the different amounts to give a net change in the value of current.
3. I_{ref} can vary about its mean value say I_{r0} by only 4 %.

To state there are two methods of generating a compensation code i.e. by the analog or the digital means

1 In the Analog domain the currents in the p-mos and the n-mos transistor at any PVT are added in their absolute values and compared to the value $2*I_{ref}$ to generate a common seven bit compensation code.

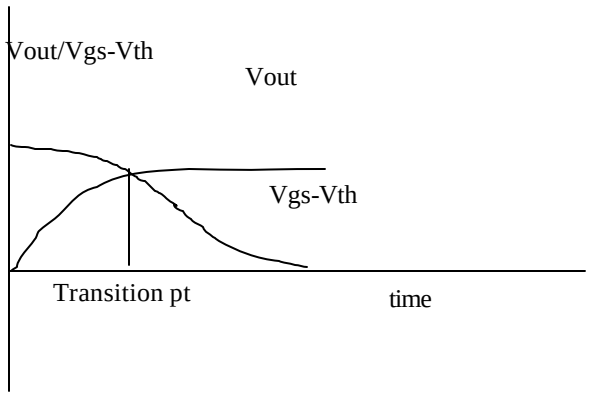
2 In the digital technique the currents in the p-mos and the n-mos transistor are compared individually to I_{ref} the value of the reference current at the typical PVT conditions to generate the two respective digital codes which are processed by a combinational digital circuit to give a seven bit digital code which optimizes the performance of the o/p buffer.

In the following discussion a quantitative description of the parameters has been presented followed by the complete analysis in the digital and the Analog domains finally presenting a conclusion as to the best technique.

2. MATHEMATICAL DERIVATIONS FOR FREQ/SLEW AND OUTPUT IMPEDENCE

We first identify the various relations between the parameters and the codes. Let's say we land on a particular code for a given PVT conditions i.e. the code has been expressed as a function of kp and kn where kp/n are the functions of the PVT $k_{n/p} = f(P,V,T)$ and the code can be written as $c = h(kn,kp)$ where `c` can be written as a function of these parameters(For compensation refer. to [1][2][4]) To find the expression for the maximum slew current(for Slew rate control refer [6]) , a rational approach is adopted as di/dt can be max when $\frac{d}{dt}(Vgs - Vt)$ is maximum, the gate of the o/p buffer is being charged through the pre-driver section it is contemplated as being charged through an RC section, R being composed of the Weqi of the prediver and C denoting the gate capacitance of the o/p buffer sections .Now assuming the signals to transit ideally at the NIN and PIN stages(refer the structure of the o/p buffer) the Vgs rises exponentially the fastest rise being near the origin of co-ordinates so to start with the analysis we assume that the max slew occurs in the saturation region of the o/p buffer itself .

To explicitly show this refer to the figure 1 below



Figure;1. Operating regions of the o/p transistor while the o/p is falling through n-mos transistor.

By reasoning we can conclude that the max slew occurs before the crossover point the slew can be written as follows

$$i = k.\frac{W}{L}.\frac{(vgs - Vt)^2}{2} \qquad ..2.1$$

Now since the Vgs gate potential is being charged through the RC

$$Vgs = Vdd(1 - e^{-t/R_i C_g}) \qquad ..2.2$$

where in the above equation Ri is the i/p resistance denoted by the Weqi of the prediver, it can be expressed as

$$Ri = \frac{1}{kn \cdot Weqi / L \cdot (Vgs - Vth)} \qquad ..2.3$$

, here in the eq2.3. The p-mos transistors in the pre-driver for the falling o/p offer the resistance. Now for our reference the term Vgs –Vth is a constant as the codes are supplied i.e. Vdd-Vth =const .the expression for the o/p current can be written as

$$i = \frac{kn.Weqo_n}{2} \cdot (Vdd(1 - e^{-t/RiCg}) - Vth)^2 \qquad ..2.4$$

To find the maximum value of the slew the above equation is differentiated

$$\frac{d}{dt} i = \frac{kn.Weqo_n}{RCg} \cdot (Vdd - Vth - Vdde^{-t/RCg}) \cdot Vdde^{-t/RCg} \qquad ..2.5$$

Differentiating once again and setting the expression equal to 0, time at which the slew maximizes is obtained as

$$t = RC_g \log(\frac{2Vdd}{Vdd - Vth}) \ , \qquad ..2.6$$

Putting this value above we get the max slew at any particular PVT conditions as

$$\frac{d}{dt} i(Slew) = \frac{kn.Weqon}{LRC_g}.(\frac{Vdd - Vth}{2})^2 \qquad ..2.7$$

and for the o/p drive ,the calculated impedance offered in the linear region can be expressed as

$$Rn/p = \frac{1}{k_{n/p}.Weqi_{n/p} / L.(vgs - Vth)} \qquad ..2.8$$

and the frequency of operation can be found by assuming that up to the transition point for the moderate values of the o/p capacitances the rate of drop of the o/p voltage is slow. So that we assume that the o/p does not drop at all and thereafter it starts discharging through the n-mos transistor s. so the total delay incurred in the path is

$$t_{total} = tr + tf + tdn + tdp \qquad ..2.9$$

,in the above equation tr denotes the rise time ,tf the fall time , tdn and tdp the delay incurred in the charging of the gate capacitances of the o/p buffers of the respective transistors .tr and tf can be found from the equations of the mos transistors in the saturation and the linear regions in that

order as when the o/p is high the o/p starts discharging until the transistor comes out of the saturation. The time of rise/fall can be written as

$$t = \frac{C_L.Vth}{I_{sat}} + \frac{C_L.\log(17)}{(Vdd - Vth).kn/p.Weqon/p} \quad . \quad ..2.10$$

putting the value of Isat in the above equation we get

$$t = \frac{C_L.Vth}{k_{n/p}.Weqo_{n/p}.(Vdd - Vth)^2} + \frac{C_L.\log(17)}{(Vdd - Vth).k_{n/p}.Weqo_{n/p}}$$

..2.11

and the delay that occurs in the pre-driver section we have $tdp/n = 4Rip/nC$,to be more explicit it can be written as

$$tdp/n = 4\frac{C}{kp/n.Weqip/n.(Vdd - Vt)} = G2.\frac{1}{kp/n.Weqip/n}$$

..2.12

, for the frequency the generic expression can be written as

$$f_{op} = \frac{1}{tr + tf + tdn + tdp}$$

..2.13

Where Ri can be written as above, operating in the linear region The tr and tf can be written in a simplified form by noting that at a certain PVT Vdd-Vth=z(const)

$$tf/r = (\frac{C_L}{z^2} + \frac{C_L.\log(17)}{z_2}).\frac{1}{kn/p.Weqon/p}$$

Lets say that $C/z^2 + C.\log(17)/z^2 = G1(const)$

So putting the above relations and simplifying the equations for frequency we get

$$f_{op} = \frac{1}{G1(\frac{1}{k.Weqon} + \frac{1}{kpWeqop}) + G2(\frac{1}{knWeqin} + \frac{1}{kpWeqip})}$$

..2.14

In the discussion to follow as a generic case we have the input and the o/p matrices as

$$Weqi^T = [wi1\ wi2\ wi3\ wi4\ wi5\ wi6\ wi7\ wi8]$$

$$Weqo^T = [wo1\ wo2\ wo3\ wo4\ wo5\ wo6\ wo7\ wo8]$$

..2.15

3 STATISTICAL ANALYSIS

3.1 Analysis in Analog Domain for 4% variation of Iref

To work with the addition in the real domain i.e. we add the ip or in components to get the I_{total} which is quantized and compared to the total reference current $2I_{ref}$ to get a final digital code .The probability of landing at a particular digital code can be found as below by abiding the above assumption

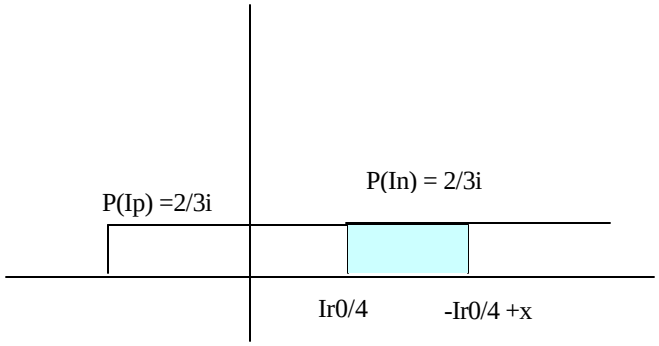


Figure: 2 Convolution of the two probability densities for the sum

To find the probability of landing at a particular code i.e $Z(say) = Ip + In$ Where In and Ip are to be independent of each other so the

P(Z) = P(Ip=x).P(In =Z-x) ..3.1.1

, which is equivalent to convoluting the two probability densities to get the following result

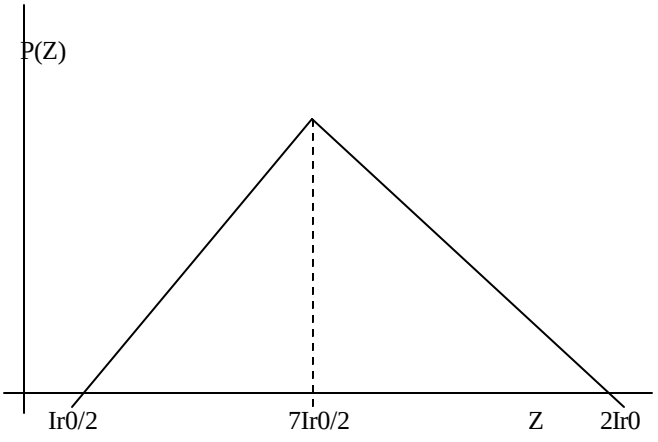


Figure:3 Probability of landing at a particular value

To analyze the probabilities of landing at a particular code the same equation is used as

above

$$P(a/ana\log) = P(noerr) + P(err \mid a-1, a) + P(err \mid a+1, a)$$

..3.1.2

In the above expression we have P(noerr) denoting the probability of landing at a particular code with no error . To see this explicitly as expressed earlier

$$Ip/n = Ir0/4 + 3Ir0/32 + a.3Ir0/16$$

..3.1.3

Once we have quantized the currents, in the above expression we have q_D=3Ir0/16 as the quantization interval for the digital case. To see this more clearly the figure below discusses the Flash comparator, which is the code generator for the above circuit. In the comparator circuit we have seven transistors with the aspect ratios properly tuned so that we generate a different code for the current landing on a different quantization level. The sizes of the transistors are decided by the fact that at every branch the current in the n-mos (Iref) is being compared with the amplified current A(Isat) in the p-mos transistors where this A(amplification/de-amplication factor) is different for each branch. It can be seen that the aspect ratios for the flash are as 8/7, 8/10, 8/13, ……8/25 giving a general expression of 8/[4+3a] where `a` varies from 1to 7.To visualize as to how the codes are different in the analog case from the digital case, the generic expressions of Ip and In add

$$Ip + In = Ir0/4 + a.3Ir0/16 + f1 + Ir0/4 + b.3Ir0/16 + f2$$

,in the above expression f1 and f2 stand for their respective fractional parts. Two cases arise as now the quantization interval for I_{total} =Ip +In is q_A =2q_D =3Ir0/8 depending on the magnitude of f1 and f2

$$Ip + In = Ir0/2 + (a+b)3Ir0/16 + f1 + f2 = I_{total}$$

.3.1.4

1. 0 < f1 + f2 <q_A when the code corresponds to (a+b)/2 i.e. (a+b)/2 when a +b is even
   $Ip + In = Ir0/2 + ((a+b)/2)3Ir0/8 + f1 + f2$ and
   (a+ b –1)/2 when it is odd
   $Ip + In = Ir0/2 + ((a+b-1)/2)3Ir0/8 + f1 + f2 + 3Ir0/16$

2. q_D < f1 + f2 .Here again two cases follow when a+b is even
   $Ip + In = Ir0/2 + ((a+b)/2)3Ir0/8 + f1 + f2$ which fetches us the same code (a +b)/2 as in the digital case and when a+b is odd we get
   $Ip + In = Ir0/2 + ((a+b-1)/2)3Ir0/8 + f1 + f2 + 3Ir0/16$

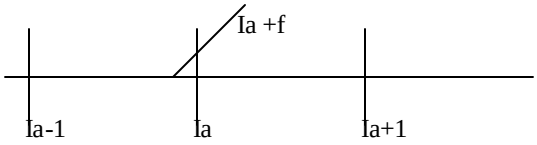
Now since f1+f2 add up greater than q_D we get the same code as (a+b)/2 which is different from that in the digital code (a + b – 1)/2 giving us a offset of one.

So to calculate the Probability of landing at a particular code as considering a generic case of current say

$$Ina = Ir0/2 + a.3Ir0/8 + f$$

.3.1.5

Landing on a quantization level `a ` now the lower level is that corresponding to the code a-1 and the upper level is that corresponding to the code a+1 so the transistor in the flash circuit size their aspect ratios as 16/(4+3(a-1)), 16/4+3a, 16/[4+3(a+1)] and so on in that sequence, the error occurs when at a quantization interval if the In is so that f satisfies Now the error would occur when



$(Ia + f)8/4 + 3a < Ir0(1 + y/100)$, where y is the %variation in the Iref, which could be to a max of two percent. Putting the value of Ia(quantized) from the above equation

$$(Ir0/2 + a.3Ir0/8 + f)8/4 + 3a < 2Ir0(1 + y/100)$$

$$f.\frac{8}{4+3a} < 2Ir0.y/100$$

.. 3.1.6

So to find the probability of error we get

$$P(erra, a-1) = \int_0^{f\max} p1.df.25/Ir0.(Ir0/50 - f.8/4 + 3a)$$

..3.1.7

in the above expression P(a) is the probability of landing at a particular value of I_{total} corresponding to the a`th quantization level . The maximum value of the fractional part can be $f\max = \frac{2Ir0.(4+3a)}{16\times 50}$ integrating the above expression between the above limits we get the expression

$$P(erra, a-1) = p1.p2.0.5.\frac{(4+3a)\times Ir0^2}{16\times 50^2}.$$

.. 3.1.8

In the above expression p1 is the approximated probability of current having a value very near to the quantization interval i.e. the trapezium around the quantization interval has been approximated to a rectangle around that point. Similarly the expression for the P(err a ,a+1) can be derived based on the above lines to give us the probability of landing at a particular code as the area under the trapezium formed in the probability density curve of the analog data.

The probabilities corresponding to the various values for the current in the analog domain are

$P(7i/8) = 3i/8.(2/3i)^2 = P(25i/8)$

$P(10i/8) = 6i/8.(2/3i)^2 = P(22i/8)$
$P(13i/8) = 3i/8.(2/3i)^2 = P(19i/8)$
$P(16i/8) = 12i/8.(2/3)^2$

Table:1 Probability of landing at a particular code (Analog)

Code c	P©
0	1/32
1	3/32
2	5/32
3	7/32
4	7/32
5	5/32
6	3/32
7	1/32

3.2 Analysis in Analog Domain for 40% variation of Iref

In the Analog domain the fractional part cannot be approximated assuming it lies near to the intervals, so the equation for the probability density of lying at a particular value in the analog domain is

$p(x) = 4/9i^2(x - i/2)$ for $c < 4$
$p(x) = -4/9i^2(x - 7i/2)$ for $c >= 4$

In the analog addition in the real domain the currents would add to be scaled/quantized wrt 2Iref, In one technique the I_{total} is scaled down to I_{ref} to be compared in the comparator circuit (Flash converter), As proceeded above the fractional part can vary to the full quantization interval's length i.e. $2q_D$ current in the interval (i/2,7i/2)
Working analogously as in the digital case the error probability can be found for the two-bit error by the equation

$$P(err2b \mid LH) = \int_{f\min}^{2qD} p4.p2.I_{r0}.(\frac{1}{5} - \frac{z}{100}).df$$

..3.2.1

$$P(err2b \mid LH) = \int_{f\min}^{2qD} \frac{4}{9i^2}(x_{a-2} + f - \frac{I_{r0}}{2}).\frac{5}{2I_{r0}}.I_{r0}.(\frac{1}{5} - \frac{z}{100}).df$$

.. 3.2..2

there would be different cases for the intervals (4,5) and (6,7) as the probability density p4 would now be written as from the above equation

Table:2 **ANALOG** Probability of a two bi transition from low to high level

CODE	P(err2b|LH)
0	----------
1	----------
2	----------
3	----------
4	0.0018228
5	0.003417
6	0.049
7	0.034216

Table:3 Probability of two-bit error for two level transition from a higher to a lower level

CODE	P(err2b|HL)
0	----------
1	----------
2	----------
3	----------
4	0.000194
5	0.0010744
6	0.0019533
7	----------

For a one-bit error for a transition from a lower to a higher level the cases can be separated as follows i.e.

$$I_{r0}(\frac{i_{a-1} + f}{i_a}) > I_{r0}(1 - \frac{z}{100})$$ and,

$$I_{r0}(\frac{i_{a-1} + f}{i_{a+1}}) < I_{r0}(1 - \frac{z}{100})$$, so that a two-bit error can be prevented the error probability for a >2 can be written as

$$P(err1b \mid LH) = \int_{0}^{f\min 2} p1.p2.df.I_{r0}.(\frac{1}{5} - \frac{2q_D - f}{i_a}) + \int_{f\min 2}^{2q_D} p1.p2.df.I_{r0}.(\frac{4q_D - f}{i_{a+1}} - \frac{2q_D - f}{i_a})$$

..3.2.3

where the value of f_{min2} can be written as

$$f_{\min 2} = 4q_D - \frac{i_{a+1}}{5}$$

Solving the above equation to express it in a generic form for both the cases as a < 2 and a > 2 respectively we get the following expressions
For **a < 3** i.e. up to ***a = 2***

$$P(err1b \mid LH) = \int_{0}^{f\min 1} p1.p2.df.I_{r0}.(\frac{1}{5} - \frac{2q_D - f}{i_a})$$

.. 3.2.4

$$f_{\min 1} = 2q_D - \frac{i_a}{5}$$

Table:4 Probability of having a one bit error for transition of one bit on either side

CODE	P(err1b|LH)	P(err1b|HL)
0	----------	0.00841
1	0.0061625	0.02312
2	0.0184	0.0445
3	0.005738 + 0.0298 = 0.035538	0.079
4	0.02479 + 0.0323 = 0.05709	0.04882
5	0.02587 + 0.03 = 0.05587	0.03123
6	0.01265 + 0.0277 = 0.04035	0.00947
7	0.00349 + 0.01539 = 0.0188	----------

The probability for having an one-bit error entailing a transition from higher to a lower quantization level the probabilities can be segregated for the three different intervals as

$$P(err1b \mid HL) = \int_0^{f\,\max 1} p1.p2.I_{r0}.(\frac{1}{5} - \frac{f}{i_{a+1}})df \quad \text{for a < 3}$$

..3.2.5

$$P(err1b \mid HL) = \int_0^{q_D} p1.p2.I_{r0}.(\frac{1}{5} - \frac{f}{i_{a+1}})df \quad \text{for a = 3}$$

... 3.2.6

$$P(err1b \mid HL) = \int_0^{f\,\max 2} p1.p2.I_{r0}.(\frac{q_D + f}{i_a} - \frac{f}{i_{a+1}})df + \int_{f\,\max 2}^{q_D} p1.p2.I_{r0}.(\frac{1}{5} - \frac{f}{i_{a+1}})df$$

..3.2.7

$$f_{\max 1} = \frac{i_{a+1}}{5}$$

$$f_{\max 2} = \frac{i_a}{5} - q_D$$

, Rewriting these equations into their general form wrt to the quantization levels we get

$$P(err1b \mid HL) = \frac{7+3a}{150} \quad \text{, for a < 3}$$

$$P(err1b \mid HL) = \frac{6a-1}{32(7+3a)} \quad \text{, for a = 3}$$

$$P(err1b \mid HL) = \frac{(3a-11).(37+39a)}{160\,(7+3a)(4+3a)} + \frac{(26-3a)}{48}(\frac{1}{5} - \frac{3a+4}{10(7+3a)})$$

for a > 4

We tabulate our calculations below:

Table:5 ANALOG

CODE	P(err1b|HL)
0	0.00841
1	0.02312
2	0.0445
3	0.079
4	0.04882
5	0.03123
6	0.00947
7	----------

Various Probabilities of occurrence and their numerical values that occur in the Analog summation case are tabulated below.

CODE	P(noerr)	P(err|LH) 1-bit	P(errHL) 1-bit	P(errHL) 2-bit	P(errLH) 2bit
0	0.02330	----------	0.00841	----------	----------
1	0.0668816	0.0061625	0.02312	----------	----------
2	0.096296	0.0184	0.0445	----------	----------
3	0.1145	0.035538	0.079	----------	----------
4	0.094046	0.05709	0.04882	0.000194	0.0018228
5	0.057197	0.05587	0.03123	0.0010744	0.003417
6	0.02982	0.04035	0.00947	0.0019533	0.049
7	0.01875	0.0188	----------	----------	0.034216

Table:6 Various Probabilities

The probabilities of landing at a particular code in the Analog domain are tabulated below

Table:7 Probability of landing at a particular code with the 40% variation in the reference current

CODE	P©
0	0.03171
1	0.096164
2	0.159196
3	0.229038
4	0.20197
5	0.14878
6	0.13059
7	0.071766

3.3 Analysis in Digital Domain for 4% variation in Iref

In the digital method for generating the codes, the saturation currents for the n-mos and the p-mos transistors are compared separately to the reference value at the typical conditions to get the two different codes say Cp and Cn, now these codes are combined in a digital circuit to produce a unique seven bit code for the particular PVT conditions. The generalized expressions for the current in the n-mos and the p-mos transistors as

$$In = Ir0/4 + a.3Ir0/16 + f2 \quad \text{..3.3.1}$$

, where f2 is the fractional part greater than zero and the code is `a, as the fractional part vanishes on quantization .Similarly for the p-mos case

$$Ip = Ir0/4 + b.3Ir0/16 + f1 \quad \text{..3.3.2}$$

, the code for which is b. The digital circuit has been so designed that the final o/p code is (a`+b)/2 if a+b is even teland (a+b-1)/2 if it is odd .To analyze the probability of landing at a particular code we follow the assumptions given in the section 1.the probability of error can be obtained in analogous manner as in the analog case.

$$P(erra, a-1) = \int_0^{f\max} p1.p2.df.(Ir0/50 - f.16/4 + 3a)$$

..3.3.3

and $f\max = Ir0/50.(4+3a)/16$ and the probability of arriving erroneously from the higher level to the lower level due to the Iref variation is

$$P(erra+1, a) = \int_0^{f\max} p1.p2.df.(Ir0/50 - f.16/7 + 3a)$$

..3.34

and the $f\max = Ir0/50.(7+3a)/16$ and the probability densities p1 and p2 denoting the uniform probability of the Isat and Iref variations respectively. The probability of no-error can be calculated as sum of two probabilities namely when the

$$Ir0/50.\frac{4+3a}{16} < f < Ir0/50.\frac{7+3a}{16}$$

where there is zero probability of error and the other as $f < Ir0/50.\frac{4+3a}{16}$ and $f > Ir0/50.\frac{7+3a}{16}$ which corresponds to the region of finite error probability. Hence an expression analogous to the analog case can be written as

$$P(c) = P(noerr) + P(err \mid c-1, c) + P(err \mid c+1, c)$$

..3.3.5

Putting the values of the expressions above we land on to the following table

Table: 8 Probability of landing at a code c (Digital)

Code c	P©(digital)
0	3/64
1	7/64
2	11/64
3	15/64
4	13/64
5	9/64
6	5/64
7	1/64

3.4 Analysis in Digital Domain for 40% variation in Iref

Considering the Digital domain a one-bit error would occur if

$$I_{r0}(\frac{i_a + f}{i_a}) < Iref \quad \text{..3.4.1}$$

putting the values of the above parameters from the eq.
and for the error occurring for the negative variation we get

$$I_{r0}(\frac{i_{a-1} + f}{i_a}) > I_{r0}(1 - \frac{z}{100}) \quad \text{..3.4.2}$$

which gives us the limit for the y and z ,the positive and the negative variations respectively as

$$\frac{z}{100} > \frac{q-f}{i_a} \quad ..3.4.3$$

$$\frac{y}{100} > \frac{f}{i_a} \quad ..3.4.4$$

An offset of two bits can occur in the digital case as compared to the analog addition. The P(err|HL) can be reached as follows

$$P(err \mid HL) = P(err \mid c+1, c) + P(err \mid c+2, c) \quad ..3.4.5$$

the second term denotes the probability of 2 bit error can be written as follows

$$P(err \mid 2Bit) = \int_{f\min}^{qD} p1.p2.i.df.(1/5 - z/100) + \int_{0}^{f\max} p1.p2.i.df.(1/5 - y/100) \quad ..3.4.6$$

The first function defines the error for a code coming from (a-2)'th level and the other function depicts the transition probability from the upper to lower level to give an error.

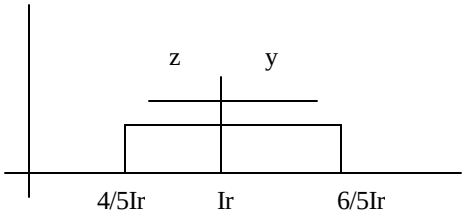


Figure:4 The variation range of the current

where in the above equations the values of fmax/min can be specified as follows entailed by the relation that the max fractional part on either side is limited to 20%.

$$f_{\max} = \frac{1}{5}.x_{a+1} - q_D \quad ..3.4.7$$

$$f_{\min} = 2q_D - \frac{1}{5}.x_a \quad ..3.4.8$$

i.e. the fractional part needed for the two-bit error depends on the quantization level. The value of the first integral and the second can be written in terms of the quantization level as

$$P(err \mid 2Bit \mid LH) = \int_{f\min}^{qD} p1.p2.i.df.(1/5 - z/100) = \frac{1}{50}.x_a + \frac{{q_D}^2}{2.x_a} - \frac{1}{5}.q_D \quad ..3.4.9$$

where the above equation is valid for a∈(4,7)

$$P(err \mid 2Bit \mid HL) = \int_{0}^{f\max} p1.p2.i.df.(1/5 - y/100) = \frac{1}{50}.x_{a+!} + \frac{{q_D}^2}{2.x_{a+1}} - \frac{1}{5}.q_D \quad ..3.4.10$$

And this equation is valid for a∈(3,7)

To calculate the error probability for the one-bit error case the procedure is analogous with the fractional part constrained to the following conditions,

$$\frac{iq_{a-1} + f}{iq_a} > I_{r0}(1 - \frac{z}{100}) \quad ..3.4.11$$

but the two-bit error must be avoided ,as to land the code in the (a+1)`th quantization level

$$\frac{iq_{a-1} + f}{iq_{a+1}} < I_{r0}(1 - \frac{z}{100}) \quad ..3.4.12$$

The concern is that one-bit error can occur but the fractional part does not go beyond the limits to favor two-bit error. The limits can be expressed as when a<3 a two bit error cannot occur landing on the (a-1)'th quantization level in which case the probability can be written as

$$P(err \mid 1Bit \mid LH) = \int_{f\min}^{qD} p1.p2.i.df.(\frac{1}{5} - \frac{q-f}{iq_a}) \quad ..3.4.13$$

and

$$f_{\min} = q_D - \frac{i_a}{5}$$

and for the quantization levels higher than 2 the result can be modified for a∈(3,7)

$$P(err \mid 1Bit \mid LH) = \int_{0}^{f\min 2} p1.p2.i.df.(1/5 - z1/100) + \int_{f\min 2}^{qD} p1.p2.i.df.(1/5 - z1/100) \quad ..3.4.14$$

$$f_{\min 2} = 2q_D - \frac{x_{a+1}}{5}$$

Considering the error of transition from a higher level to a lower quantization level the analogous steps can be performed, the error would occur when the fractional part is constrained to be such that it propels the one-bit error and the two–bit error is avoided

$$\frac{iq_{a+1} + f}{iq_{a+1}} < Ir0(1 + \frac{y}{100}) \quad .. 3.4.15$$

$$\frac{iq_{a+1} + f}{iq_a} > Ir0(1 + \frac{y}{100}) \quad .. 3.4.16$$

, very analogously to avoid the two-bit error as in the L|H(transition) case. From the above conditions we get that for a<4

$$P(err \mid 1Bit \mid HL) = \int_{0}^{f\max 1} p1.p2.i.df.(1/5 - y/100)$$

$$P(err\,|1Bit\,|HL) = \int_0^{f\max 1} p1.p2i.df.(1/5 - f/iq_{a+1}) \quad .. 3.4.17$$

$$f_{\max 1} = \frac{x_{a+1}}{5}$$

If we consider the quantization levels a∈(4,7), then we can have a possibility of 2-bit error occurring and the values landing instead on the quantization level (a-1) for this case the above equation can be rewritten as

$$P(err\,|1Bit\,|HL) = \int_0^{f\max 2} p1.p2i.df\,.(1/5 - z1/100) + \int_{f\max 2}^{qD} p1.p2i.df\,.(1/5 - z1/100)$$

$$f_{\max 2} = \frac{x_a}{5} - q_D \quad .. 3.4.18$$

To have a final code by combining the codes from the p and the n-mos transistor same digital logic is followed as above. The probability of landing at a particular code in individual p and n-mos can be written as

$$P(c) = P(c\,|noerr\,) + P(err1b\,|\,c-1,c) + P(err1b\,|\,c+1,c) + P(err2b\,|\,c+2,c) + P(err2b\,|\,c-2,c)$$

..3.4.19

The probability of no error can be written as the probability of fractional part varying from zero to q_D and the percent variation in Iref to be constrained so as to cause no error. The probability of having no error can be categorized for three levels as for a ∈ (4,6)

$$P(noerr) = \int_0^{qD} p1.p2.df\,.I_{r0}.(\frac{f}{i_a} + \frac{q_D - f}{i_{a+1}}) = \frac{15.(11+6a)}{32.(7+3a).(4+3a)}$$

.. 3.4.20

The constraint has to be met that the maximum and the minimum variations are constrained in the limits (0,1/5) when

$\frac{q_D}{i_a} < \frac{1}{5}$ and $\frac{q_D - f}{i_{a+1}} < \frac{1}{5}$

for ***a < 3***

$$P(noerr) = \int_0^{f\min} p1.p2df\,.I_{r0}.(\frac{f}{i_a} + \frac{1}{5}) + \int_{f\min}^{f\max} p1.p2.df\,.I_{r0}.(\frac{f}{i_a} + \frac{q_D - f}{i_{a+1}}) + \int_{f\max}^{qD} p1.p2.df\,.I_{r0}.(\frac{q_D - f}{i_{a+1}} + \frac{1}{5})$$

..3.4.21

above rule is a bit different for *a =0* as the condition on the constraints change, here the lower limit on the fractional part exceeds that of the upper limit as we can realize from the equation that the condition

$\frac{q_D}{i_{a+1}} > \frac{1}{5}$ for the lower case and the similar limit goes for the upper case constraint ,so the equation can be modified as

$$P(noerr\,|\,a=0) = \int_0^{f\max} p1.p2.df\,.I_{r0}.(\frac{f}{i_a} + \frac{1}{5}) - \int_{f\min}^{f\max} p1.p2\,df\,.I_{r0}.(\frac{2}{5}) + \int_{f\min}^{qD} p1.p2.df\,.I_{r0}.(\frac{q_D - f}{i_a + 1} + \frac{1}{5})$$

.. 3.4.22

and for ***a =3*** the following equation is applicable

$$P(noerr) = \int_0^{f\max} p1.p2.df\,.I_{r0}.(\frac{f}{i_a} + \frac{q_D - f}{i_{a+1}}) + \int_{f\max}^{qD} p1.p2.df\,.I_{r0}.(\frac{q_D - f}{i_{a+1}} + \frac{1}{5})$$

.. 3.4.23

$$f_{\max} = \frac{i_a}{5}$$

$$f_{\min} = q_D - \frac{i_{a+1}}{5}$$

for ***a =7***, the error due to the higher transition level is not possible and we get

$$P(noerr) = \int_0^{qD} p1.p2.df\,.I_{r0}.(\frac{f}{i_a} + \frac{1}{5}) \quad .. 3.4.24$$

Tabulating the above probabilities to get the probability of landing at a particular level individually for the n-mos and the p-mos transistor the following is obtained

Table:9 Probability for various codes for occurrence of no error

CODE	P(noerr)
0	0.13707
1	0.0656
2	0.072
3	0.06465
4	0.053967
5	0.04598
6	0.040056
7	0.08125

Table : 10 Probability of error on one bit for Transition from low to high Quantization level

CODE	P(err1b|LH)
0	----------
1	0.01458
2	0.0208
3	0.026876
4	0.031578
5	0.03493
6	0.03749
7	0.0395

Table : 11 Probability of two bit error for transition either sides

CODE	P(err2b|LH)	P(err2b|HL)
0	----------	----------
1	----------	----------
2	----------	----------
3	----------	0.0001302
4	0.0001302	0.001754
5	0.001754	0.00464
6	0.00464	----------
7	0.00833	----------

Finally the probability of landing at a particular code in the n-mos /p-mos tx can be tabulated as

Table : 12 Various Probabilities

Code	P(noerr)	P(err|LH) 1-bit	P(errHL) 1-bit	P(errHL) 2-bit	P(errLH) 2bit
0	0.1020833	----------	0.01458	----------	----------
1	0.089582	0.01458	0.02083	----------	----------
2	0.07708	0.0208	0.02708	----------	----------
3	0.06471	0.026876	0.03320	----------	0.0001302
4	0.053967	0.031578	0.03774	0.0001302	0.001754
5	0.04598	0.03493	0.03452	0.001754	0.00464
6	0.040056	0.03749	0.04023	0.00464	----------
7	0.08125	0.0395	----------	0.00833	----------

As analogously the probability of reaching at a seven-bit digital code which is supplied to the pre-driver and the o/p buffer section can be written by considering all cases to land on a particular code

Table : 13 Total combinations for landing at a particular code

CODE `c`	Number
0	3
1	7
2	9
3	15
4	13
5	9
6	5
7	1

CODE	P(err1b|HL)
0	0.01458
1	0.02083
2	0.02708
3	0.03320
4	0.03774
5	0.03452
6	0.04023
7	----------

Table : 14 Probabilities of landing at Erroneously one bit to lower Quantization levels

Table :15 Probability of getting a particular code

CODE 'c'	P(`c`)
0	0.1167
1	0.124992
2	0.12496
3	0.1249162
4	0.125162
5	0.121824
6	0.122416
7	0.129080

Putting the above values of the probability in the occurrence relations exhausting all the possible combinations we get the final probabilities of landing at a particular code when summing the codes in the digital domain to finally obtain a seven bit digital code.

The probability that we land onto a particular code is

$$P(c) = P(c).P(c) + P(c-1).P(c+1) + P(c-2)P(c-2) + P(c-3)P(c-3)..$$

..4.31

Earlier a calculation was presented to get the probability of occurrence of a particular code due to process variations in the individual p-mos or n-mos transistors, Now these codes are combined through a digital Logic circuitry to get a final seven bit code which would be put on the data-lines to the pre-driver and the O/P buffer section. The final codes that would come on the seven bit lines occur with the probabilities given below

Table :16 Probability of landing at a code in the digital domain

CODE 'c'	P(`c`) Seven-bit
0	0.042792022
1	0.105182
2	0.1357076
3	0.228355588
4	0.19821666
5	0.13987135
6	0.07803
7	0.0166164

4 ANALYSIS FOR THE MAXIMUM DEVIATIONS

As derived earlier the expressions for the slew (max), frequency of operation and the o/p resistance can be written solely in terms of the code c after quantizing the process parameters.

$$\frac{d}{dt}i(Slew) = \frac{kn.Weqon}{LRiC}.(\frac{Vdd - Vth}{2})^2 \quad ..4.1$$

$$Ri = \frac{1}{kp \cdot Weqi/L \cdot (Vgs - Vth)} \quad ..4.2$$

Putting this value of R in the above equation we have slew as

$$SL = Q(const).kn.kp.Weqon.Weqip \quad ..4.3$$

and proceeding in the same direction we get the value of the o/p drive as $Ro = \frac{P(const)}{kn/p.Weqon/p}$ and putting the above equations in the eq 2.4. we have

$$f_{op} = \frac{1}{G1(\frac{1}{k_n.Weqon} + \frac{1}{kpWeqop}) + G2(\frac{1}{knWeqin} + \frac{1}{kpWeqip})} \quad ..4.4$$

Working on the assumption that kp and kn vary in the same direction i.e. they both lie in the same quantization level at a particular PVT conditions and the Weqi and Weqo are the same function of the code we can reasonably see that frequency depends linearly on the codes and the slew has somewhat quadratic dependence on the codes which both peak at code 3. Considering the case when we tune the o/p buffer for a constant o/p drive and a constraining slew we adjust the i/p and the o/p W`s, once this is done the frequency is automatically fixed to a particular value for any PVT conditions. The solutions above are only valid for the case when we quantize k`s in an ideal case. To analyze the effect of this tuning on all possible cases of variation of the k`s the extreme case is evaluated for the error in the required values. Out of the various combinations of kp and kn for each code, the extreme case can be tabulated as

Table: 17 Process Parameter combination for various codes

Codes	Kn	Kp
0	K0	K1
1	K0	K3
2	K0	K5
3	K0	K7
4	K1	K7
5	K3	K7
6	K5	K7
7	K7	K7

Assuming that for the min max case the kp always lies at the higher extreme, the assumption just generalizes the extreme case, which is equally valid for the other case when the k 's are at the opposite extremes .In the above table Kc denotes the k lying in the c'th quantization level corresponding to the code `c`. In generic sense the k(process parameter) corresponding to a code `c`

$$kn/p(c) = \frac{Ir0/4 + c.3Ir0/16 + .3Ir0/32}{W/L.(Vdd - Vth)^2} \quad ..4.5$$

and the value of k at the typical conditions can be specified as

$$kp/n(4) = 35Ir0/32.\frac{1}{W/L.(Vdd - Vth)^2} \quad ..4.6$$

and writing the k at any PVT condition in terns of that at typical

$$kn/p(c) = \frac{11 + 6c}{35}$$

, where the values of k have been quantized at the middle of the quantization interval. Putting this value of k in the above equation for the operating parameters we get seven solvable equations for the Weqi and Weqo to get these matrices. Lets say once the circuit has been tuned to give a frequency f_0 for all the codes, in the min max case we get the deviation for the frequency as tabulated below for each code.

Table: 18 Relative frequency

Code c	Relative Frequency for the min-max case
0	1.214
1	.9388
2	.7546
3	.6282
4	.7369
5	.9143
6	.9837
7	1

Similarly if the circuit has been tuned for the constant slew for all codes the relative slew can be tabulated for the min-max case as

Table: 19 Relative Slew

Code c	Relative Slew(max) for the min-max corner
0	$\frac{17}{11}$
1	$\frac{11\times 29}{17^2}$
2	$\frac{41\times 23}{23^2}$
3	$\frac{53\times 11}{29^2}$
4	$\frac{53\times 17}{35^2}$
5	$\frac{53\times 29}{41^2}$
6	$\frac{53\times 41}{47^2}$
7	1

Carrying on analogously the o/p resistance for the n-mos and the p-mos transistor can be tabulated as follow

Table: 20 Output Resistance(code specific) for p and n drive seperately

Code `c`	Ro/p	Ro/n
0	11/17	1
1	$\frac{17}{29}$	$\frac{17}{11}$
2	$\frac{23}{41}$	$\frac{23}{11}$
3	$\frac{29}{53}$	$\frac{29}{11}$
4	$\frac{35}{53}$	$\frac{35}{17}$
5	$\frac{41}{53}$	$\frac{41}{29}$
6	$\frac{47}{53}$	$\frac{47}{41}$
7	1	1

Considering a step ahead, let's say that I_{ref} varies by 40% i.e. from $I_{r0}.4/5$ to $6I_{r0}/5$ with a probability density varying uniformly as p(3)=5/2Ir0 , the current ip/n can be expressed as in eq .With this large a variation in Iref there is a possibility of a two-bit error as the variation is itself greater than the quantization interval.

5 CONCLUSIONS

After we have calculated the relative parameters for the min max case presented below are certain numbers to draw a conclusion on the analog and digital performance. The aim is to have the highest operating frequency and a low slew still conforming to the values of the o/p drive.
Tabulating the errors in frequency, slew and the o/p drive a measure of the `best` performance can be made as offset from the values at which the k's lie in the same quantization interval f_0, S_0 and R_0

Table: 21 Parameters Deviation for various codes

Code `c`	Frequency deviation f-f0	Slew Error S0-S	O/p Drive error Rp |R-R0|p	O/p Drive error Rn |R-R0|n
0	0.214	-0.5454	0.3529	0
1	-0.0612	-0.1038	0.4138	0.5454
2	-0.2454	0.1474	0.439	1.09
3	-0.3718	0.30677	0.453	1.63
4	-0.2361	0.26449	0.34	1.059
5	-0.0857	0.08556	0.2264	0.4138
6	-0.0163	0.0163	0.1132	0.1463
7	0	0	0	0

Table: 22 Average values of various parameters

Variation %	Frequency deviation f-f0	Slew S_0-S	O/p Drive Rp |R-R0|p	O/p Drive Rn |R-R0|n
4% ANALOG	-0.1853	0.13609	0.337	0.888
40% ANALOG	-0.1858	0.1892	0.341	0.89385
4% DIGITAL	-0.187	0.13489	0.3519	0.91375
40% DIGITAL	-0.171339	0.126	0.3159	0.8565

In the worst-case conditions it is required to have the frequency deviation (f- f_0) to be less and so for the slew variation (S_0-S), and the o/p impedance variations. In that case in the 40% variation of Iref the Digital summation performs the best as seen from the above table.

Conforming to our requirement the analog method gives us a less frequency deviation, lower slew and less error for the o/p-drive as compared to the digital case.

In the 40% variation of Iref it is observed that there is a shift towards obtaining higher codes in the analog domain as compared to that of the 5% variation case and the opposite trend can be seen in the digital domain i.e. the codes have more probability of landing in the lower codes as compared to the earlier 5% variation in the Iref variation

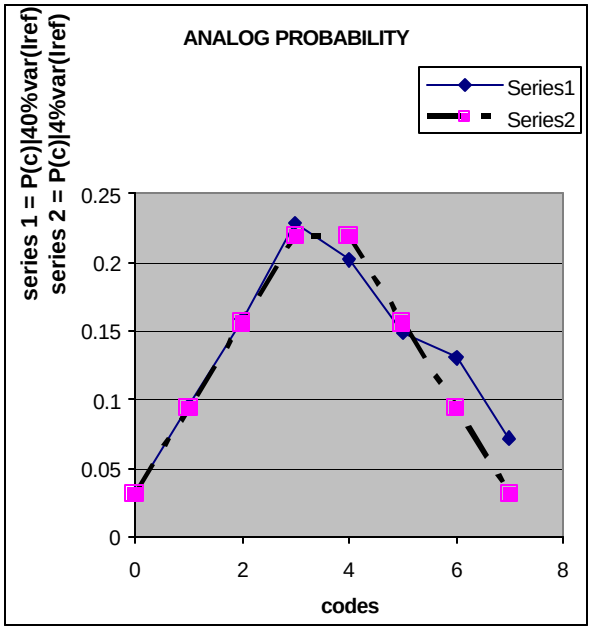


Figure :5 Probability of getting a particular code by Analog processing in the compensation Block with the two different variations in the reference current

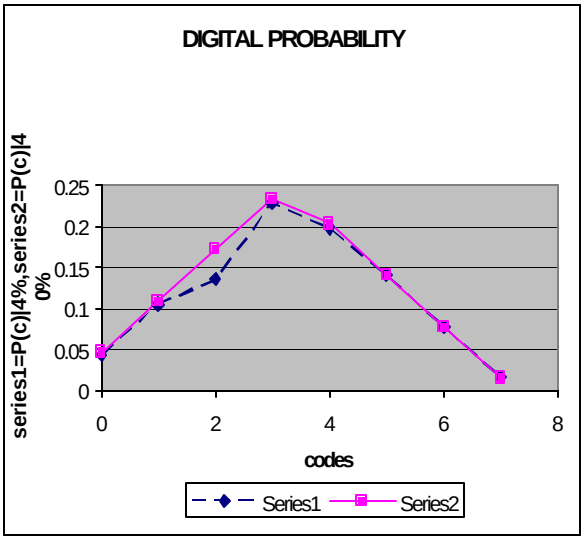


Figure :6 Probability of getting a particular code in the Digital domain with two different variation in the reference current

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