A Low-Cost CMOS Control System
With Complete Analog Signal Processing

Daniel Batas,   Klaus Schumacher

University of Dortmund,
Dept of Microelectronics,
44221 Dortmund, Germany

Abstract

In this paper an integrated microsystem for control applications is presented. The signal path is completely designed in analog CMOS-technique to exploit the advantages of the signal continuity. Digital blocks are only used as peripheral devices e.g. to implement a common programming interface. Especially by integrating particular analogous functions a big advantage can be obtained in terms of overall fabrication costs. A motor controller was chosen as an example to present the specific components of the control system. Furthermore their contribution to the entire system is discussed. Based upon statistical examinations it can be shown that the yield of this analog system is competitive to respective digital solutions when considering mismatch behaviour in an early design stage.

1.   Introduction

Analog CMOS circuits often are not favoured for integrated systems. This paper intends to reveal that a complete integration of an analog microsystem is capable of reducing external components which are extensively used in common analog circuits. Therefore not only costs can be saved but new applications are feasible which will be presented here. This solution should substitute a microcontroller-based design for controlling electrical motors resp. it is optimized for all power-controlled AC-consumers in general. In principle the concept of this control application can be realized in both techniques, analog and digital. The facility of integrating all analog subcircuits onto a single die allows to place the whole system into smallest spaces e.g. inside a grip of a drilling machine. Furthermore this is a very cost-effective solution, especially suited for low-cost applications. So a completely analog realization of the concept can achieve some advantages compared to a digital microcontroller-based solution. However the control-characteristics of the designed system should in no case be fixed to a specific application but rather be kept very general. Thus it can handle a great deal of controlling tasks and is not restricted to the range of applications defined in the beginning. For this purpose it is essential to provide some kind of programming possibility for the control function, regardless if the system is designed analog or digital.

The analog realization of the basic controller concept has a relatively short and completely analog signal-path. In this case the essential is that the signal amplitude remains its analog continuity. Therefore the controller is very fast and isn't subjected to discretization effects. Designs of equivalent digital solutions of the same concept for a parametric field show an output signal wobbling between two discretization steps although it should be at a constant value. This is due to insufficient discretization precision and could be demonstrated on digital controllers with an 8-bit resolution. To overcome this problem digital solutions have to be designed with higher computational accuracy of at least 12-bit, thus the required chip size is increased. However, the analog parametric field in this realization doesn't require the same high resolution and can be concepted with a minor resolution and therefore has a smaller die size. These advantages in combination attend an analog realization of the control concept to be with good prospects.

2.   Parametric field

The core of the whole circuit is the analog parametric field that builds the basic control function. In general parametric fields have a transfer function in the form of $F : \mathbb{R}^n \rightarrow \mathbb{R}^m$. However, for many applications a two-dimensional parametric field with one output is required only ($n = 2$, $m = 1$).

Control applications based on a parametric field can be built with a wide range of control behaviour. Here, the generation of a configurable transfer function is implemented using small pieces of planes to form the desired overall transfer function. By allocating more planes, higher adaptation to the given transfer function can be obtained. Starting with equidistant distributed planes, the approximation-accuracy can be enhanced by relocating some of the planes, preferable to locations of the graph where its gradient has fast alternations. In most applications the grid of planes which form the overall transfer function even does not require to have a notably high resolution. There is rather need for a highly cost-efficient implementation.

The use of planes implicates a piecewise linear interpolation between the intended sampling points in the grid. An analog drive of the input results in a time- and value-

continuous output signal. Through this, the circuit has the property of high processing speed despite of its low circuit complexity.
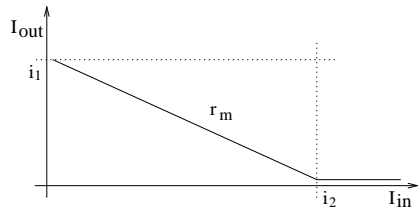

Figure 1. ramp function

To generate a single plane in the 3D-grid two ramps and one cell subcircuit are required. Here each cell is driven by its associated pair of ramps which define the position inside the grid. The rise of this plane is stored in 4 programmable switches in the cell. In this realization an array of $7x7$ cells was applicated using a CMOS technology line with a minimum feature size of $1.2\mu m$. Of course the number of planes can be increased, but then it is advisable to employ a much more modern technology line because the required die size is growing by square when increasing n. For the given technology line a value for n of 7 is the most economical solution resulting in 49 weighted cells. The use of simple ramps indicates a linear interpolation method. This was chosen because the circuit to form a ramp consists of a small number of transistors only, thus the circuit complexity can be kept low. The total number of ramp-generators can be reduced enormously by not providing two ramps for each cell but only one ramp for each line resp. column of cells in the grid. This results in some smaller restrictions to the adaptability of the transfer function, but the savings of total chip size is a point of more importance.
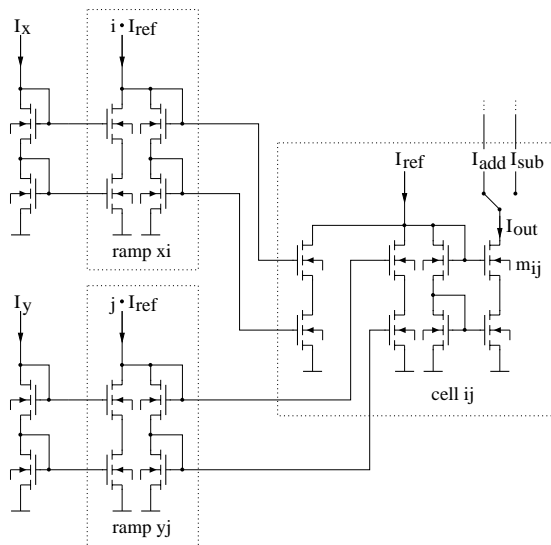

Figure 2. signal path for one cell

The connections of the cell outputs to the common circuit output isn't drawn in figure 3 to simplify the depiction.
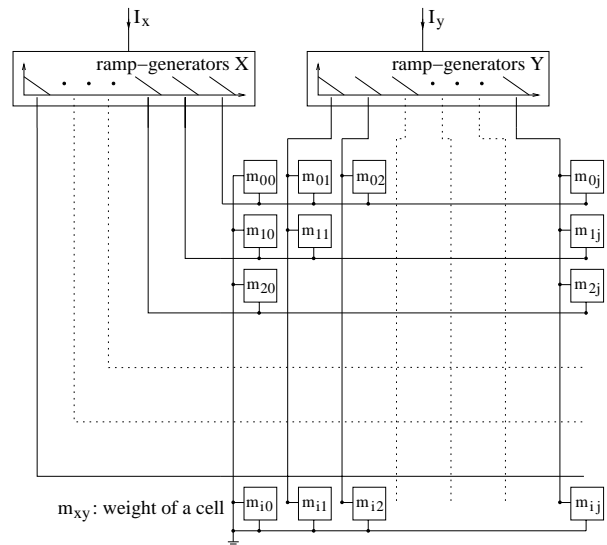

Figure 3. block diagram

Each cell adds a share (positive *or* negative) to the total output current depending on its assigned range of the input current which is determined by its respective ramps. This current contribution is adjusted by the weight of each cell. To be able to obtain a gain or a reduction of the total output current by a single cell, the weight is defined as a signed value. Inside the circuit first the positive and negative contributions of all cells are collected separately to be totalized afterwards.
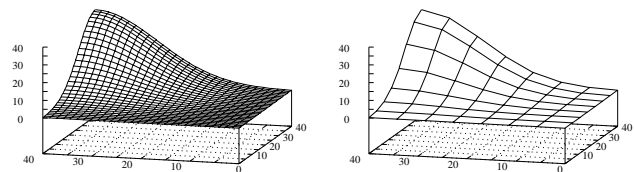

Figure 4. an ideal function & its real approximation

3. System overview

The project was defined to build this analog system on a single chip only and further on to reduce the number of external components to an absolutely necessary minimum. It must be clarified that there is no way to omit all externals; some components like power-semiconductors or power-resistors cannot be integrated in standard CMOS-technology. The programmability ensures a versatile control system for all electric motors. Therefore the system can be manufactured in high quantities at very low costs.

A power-supply-subcircuit converts the mains voltage to the low DC-voltage required by the rest of the system. Here only 5 cheap passive external components are needed. In the integrated part of this module the ripple of the DC-supply-voltage is controlled. A Zero-Crossing-Detector scans the mains voltage and provides 100Hz reference impulses to synchronize the controller with the

electric motor. For this purpose only 1 ordinary external resistor is required. Furthermore this signal is fed into the PLL-block as the reference-frequency. To start at a defined initial point a Power-On-Reset-circuitry is integrated. The input e.g. a speed demand for the motor is fed into the parametric field in conjunction with the signal from the loop-back.
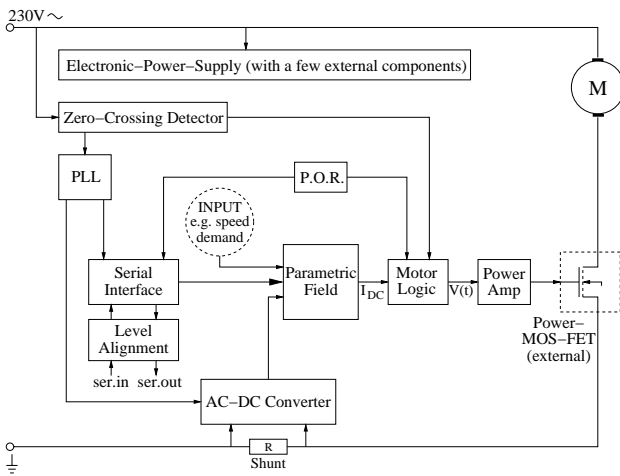

Figure 5. block diagram of the system

The output current of the field flows into the motor logic block where it is converted into a time variant voltage signal. Because Power-MOS-FETs have huge Gate-Source-capacitances this new signal must be boosted up by a Power-Amplifier. Via the external MOS-FET the current- consumption of the motor can be affected. A small shunt resistor in the current-path of the consumer causes a voltage difference depending on the motor's power load. Because the voltage-drop over this shunt is alternating it must be averaged into a Direct-Current for the loop-back of the parametric field. To read-in the parameter of the transfer function the serial block provides a digital interface to the outside. Onchip all signals use standard CMOS-voltage-levels.

3.1. Motor logic

For controlling electric motors the current-output of the parametric field cannot be used directly. As it is intended to control the motor via a Power-MOS-FET, the Direct-Current-output of the parametric field must be converted into an equivalent time-variant gate-source-voltage for the Power-MOS-FET. Thus the motor runs with alternating current controlled by the Power-MOS-FET.

The functional principle of the motor logic is similar to a common phase controlled modulator using thyristors but here the power is not switched *on* but it is projected to be *cut off*. So, disadvantages of common modulators can be eliminated e.g. it is possible that with a single firing-impulse the thyristor is not fired at once, so another impulse must be started again. Therefore sufficient firing energy must be kept in a big external capacitor

which increases the size and cost of the circuit. Further, using common phase controlled modulators in conjunction with electric motors result in a non-harmonic movement of the rotor through high frequency waves caused by high switch-on currents. All these effects can be eliminated using Power-MOS-FETs instead of thyristors.
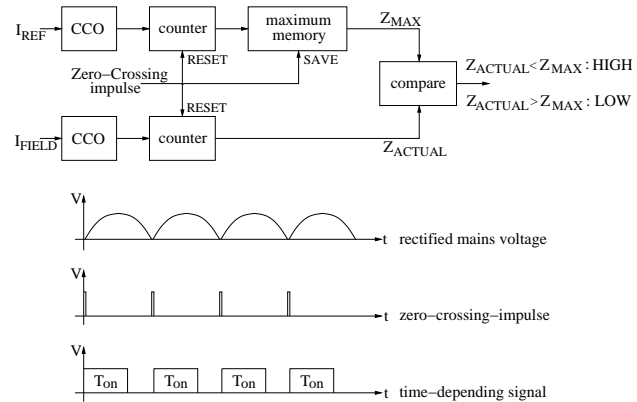

Figure 6. motor logic overview

The output-current of the parametric field feeds a MOS-capacitor causing a time-linear voltage increase. As the room for an integrated capacitance is extremely limited, here a switched technique is applied. A relatively small capacitor is charged with the Direct-Current from the parametric field. When a defined threshold voltage is reached, a "Schmidt-Trigger" generates a counter-impulse and the capacitor is discharged immediately to be ready for the next cycle. So, each counter-step represents the charges of one complete charging cycle. Depending on the amperage of the current the cycle lengths have different speeds. When the counter reaches its specified maximum the Power-MOS-FET disconnects the motor from the mains.
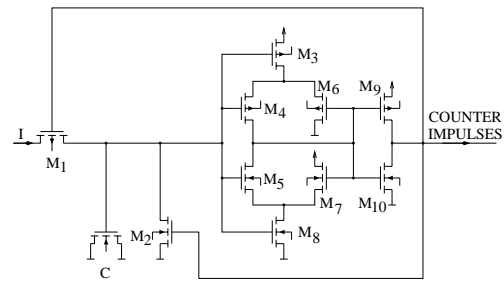

Figure 7. a single CCO (current controlled oscillator)

To determine the right moment to disconnect the motor from the mains two CCOs are started when the mains-voltage crosses zero. The main CCO is fed with the field-current, the other CCO is used as a reference source. Its reference current is set to the allowed minimum field-current resulting in a maximum speed utmost equal to the main CCO. At each zero-crossing of the mains the value of the reference counter is stored into a 9-bit static memory-cell and is then reset.
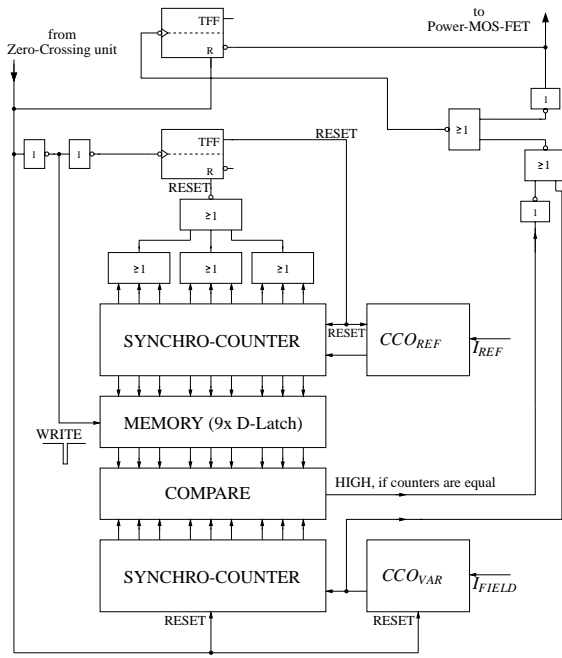
Figure 8. motor logic block

ternating mode, it must be averaged and converted into Direct-Current. Therefore this subcircuit behaves like an integrated lowpass-filter. Measuring the rotational speed of the motor directly would be a somewhat better solution but also much more expensive. So, here the current-consumption of the motor has been chosen as a feedback for the controller. To obtain a high RC-constant for the filter, switched-capacitor-technique was applied.
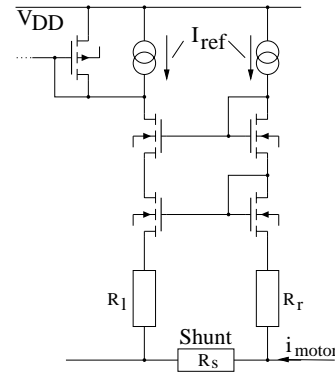

Figure 9. input stage of the converter

Figure 9 shows the branches of the input state with 2 equal currents. In dependence on the shunt-voltage a small difference in the left current can be detected. This is amplified by a current mirror and averaged by the following SC-stage. Resistors R_l and R_r are implemented onchip.

3.3. Power supply

To be independent from additional supply-voltages this controller has been concepted to generate its own simple supply out of the $230V \sim$ power mains. Only 5 external passive devices are needed, all others are integrated. First the AC-voltage is rectified, then down-scaled and smoothed via a resistor and a capacitor two times (figure 10). The integrated part of this subcircuit controlles the generated voltage to a specified constant value by cropping the superfluous current.
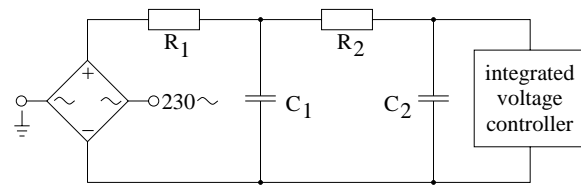

Figure 10. power supply externals

In the next cycle this value is used to be compared with the counter of the main CCO. Because it is running faster, the two counters definitely equal each other during the period. This state defines the criterion to disconnect the motor from the mains. The use of counters may seem to have a discretization on the field-current but as the amperage exactly defines the speed of the counting-cycles, the cut-off-edge can be initiated at *any* (time-continuous) point within the period. Therefore no discretization step is performed here. Especially when working with motors the environmental temperature can differ in a wide range. Anyhow, for operation at all temperatures without any additional cooling facilities, the reference-CCO has been added. In fact one CCO would be sufficient but with a reference-CCO there is the advantage of automatically readjusting the cut-off-point to changing environments. By this, temperature offsets can be eliminated. Further, the very low-frequency fluctuations of the mains-frequency can be taken into account because the reference-CCO will be updated two times a period. So, this effect is compensated as well. From the view of the motor-logic-block the change of the field-current is extremely low because the feedback is depending on a mechanical component. Therefore the dimension of the current-alteration is app. in the range of the rotational speed of the motor.

3.2. Active AC-DC-converter

An important module of the system is the loop-back-branch from the motor-side back to one of the inputs of the parametric field. The value for the feedback is generated by measuring a voltage difference over a small shunt-resistor placed in the main current-path of the motor. Because the voltage-drop over the shunt is in al-

3.4. Serial interface

A standard serial interface is integrated to be able to program the desired transfer function. Using a serial interface has the advantage that only a few additional pads are required. So, a very small chip case can be used. This

part of the circuit uses digital signals as a matter of course but is the only completely digital subcircuit in the entire system. The interface offers an easy way of defining the proper control behaviour and thus makes the whole system very adaptive to any kind of control functions.

To ensure secure data transfers, the circuit is able to detect transfer errors. Just a single bit-error can have unforeseen consequences on the behaviour of the parametric field which could result in serious security risks because one error influences all successive data words. On this account an input buffer has been applied. So data is read in, checked for transfer errors and mirrored into the memory-cells, if no error has been detected.

3.5. PLL

The integration of the PLL-subcircuit is an important factor because it is needed by many blocks of the system e.g. the programming interface or the SC-circuits. The requirements regarding the accuracy to the frequency are not very high. Therefore the integration of an accurate time-normal-circuitry is not required. The transmission of a single data word on the serial bus defines the minimum frequency requirements of the PLL. In this case the actual frequency should not have a greater drift than 4.86% from the specified carrier-frequency ($9600Hz$). For this control application the external $50Hz$ mains voltage signal can be used as a trigger for the PLL. DIN EN 50160 [3] defines that the frequency at maximum varies for $\pm 0.5Hz$ but most time it is even better. This already leads to an adequate PLL-frequency. As described above, here the zero-voltage-detector can be used to generate a symmetric $50Hz$ signal out of the mains voltage. The base-frequency of the VCO is set to $153.6kHz$ by choosing a factor for the divider of $3*2^{10}$. For the serial interface a frequency of $9600Hz$ is needed. This can be grabbed from the divider chain.
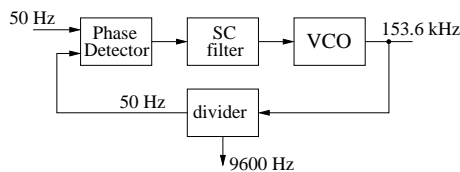

Figure 11. PLL

The analog filter-subcircuit which generates a low-frequency DC-voltage signal out of alternating impulses from the phase-detector is realized in switched-capacitor-technique in order to shrink the required capacitor to an acceptable dimension for onchip integration. Here, $20pF$ are integrated.

4. Matching

The mismatch behaviour has been analysed by measuring some stand-alone subcircuits of the system. It has been proved, that the current-mismatch of the parametric field has a relative standard deviation below 1.4%. This has been achieved by considering the mismatch-effects early in the design process using the tool GAME [4]. A drilling machine as an application does not even need such an accurate absolute output value. Here, the overall form of the generated curve is more important.

In the PLL-subcircuit the variations of the output-frequency are primary depending on the mains frequency. Here transistor mismatch is negligible because the base-frequency is completely controlled by the input-frequency and the divider via the feedback-loop. All subcircuits have been developed and tested in the same CMOS technology line. The idea of a completely integrated controller-chip was already though of in [1], therefore as a common basis for all subcircuits the same technology line had to be applicated, which has a minimum feature-size of $1.2\mu m$ only. Most notably the overall die-size could be reduced significantly when applying a more modern CMOS process.

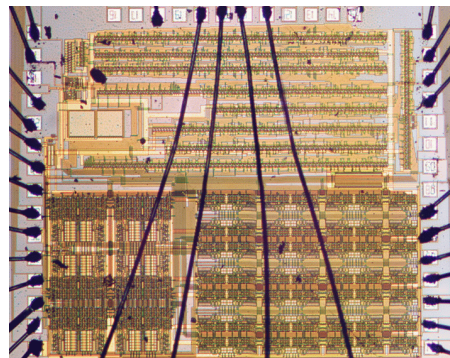Figure 12. chipfoto

5. Conclusion

In this paper a control system based on a pure analog-path parametric field has been presented. Standard-CMOS-technology was chosen because of the big amount of static gates and to obtain lowest cost of production. All subcircuits were developed to require only a minimum of external components. Most could be fully integrated. Therefore this analog system is very cost effective and does not need much space for installation. Here, the advantages of both, analog and digital techniques, were consequently exploited. Most notably when applying multi-dimensional inputs the parametric field concept can also be used as a fuzzy-controller.

[1] D. Batas, J. Oehm, K. Schumacher "A low cost solution for programmable analog parametric fields", Proceedings of the 6th ICECS, ISBN 0-7803-5682-9, Vol.II,pp.1035, Sep. 1999

[2] J. Oehm, M. Gräfe, T. Kettner, and K. Schumacher "Universal Low Cost Controller for Electric Motors with Programmable Characteristic Curves", IEEE Journal of Solid-State Circuits, Vol. 31, pp. 1041-1045, July 1996

[3] DIN standard EN 50160:1999 section 2.1

[4] "GAME – General Analysis of Mismatch Effects", Statistics simulation program, manual at http://www.zkom.de