A Novel Cascode Differential Amplifier

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Abstract – A novel cascode circuit, the Differential Cross-Connected Cascode, is proposed and investigated. Its fundamental distinction from the Differential Ordinary Cascode consists in the input signal voltage being applied simultaneously to the inputs of common emitter/source and common base/gate stages, and besides the inputs of CE/CS and CB/CG being cross-coupled. We show that the input signal is amplified in the input circuit, furthermore the input impedance and the current gain increase considerably and the bandwidth is essentially expanded. Simulation results of such a cascode designed with IBM BJT transistors are presented. The actually obtained bandwidths (18.7 GHz) proved as predicted to be more than twice as wide as compared with the bandwidth of the ordinary cascode (8.6 GHz).

Key – Words: - Cascode, cross-connected cascode, cross-coupled cascode, differential amplifier.

1 Introduction

One of the most efficient and frequently used circuits, favoring enhancement of the features of the main amplifying stages is the cascode circuit, i.e. common emitter/source-common base/gate (CE/CS-CB/CG) connections. An uncountable number of papers dealt with its investigation and different applications. However, research work continues to appear and new application opportunities are proposed. This is due, first of all, to the features of the functional circuit itself. The simplest version of this circuit is shown in Fig. 1 in the form of a differential pair.

Further on, we shall call this circuit Differential Ordinary Cascode (for brevity DOC) and for clarity's sake we will consider only its BJT-based type.

A rather full presentation of the properties of the ordinary cascode circuit is given, for instance in [1]. But this simple configuration does not allow increasing cascode current gain, input and output impedances and frequency band of the circuit as compared to the standard CE cell. The main cause is the rigidity of the circuit structure, which provides feeding of the input signal to the base of the CE stage only.

A great number of inventions and scientific research work has been dedicated to overcoming the drawbacks and limitations of the standard cascode and developing its merits. Let us mention at first the original patent [2], which proposed to use input matched resistors cross-coupled between the bases of the CE and emitters of the CB cascades to increase gain and dynamic range. Then denote the work [3], which proposes to apply a negative feedback between emitter and base of the CB stage by means of a dedicated amplifier in order to considerably increase the output resistance of the cascode. Finally, the urge increase of allowable output voltage, power, efficiency and enhanced matching with the load has lead to the creation of various multistage cascodes [4] and [5] made up of a CE stage and several CB stages.

This brief overview is aimed to show that a signal additionally applied to the base of a CB stage may considerably increase the output impedance and output voltage of the circuit and somewhat improve the circuit parameters, but does not permit of

changing appreciably its transfer function and input resistance. This is quite natural, because the characteristics of the CE stage remain unchanged.

Using regularly the cascode in its differential form, we paid attention to some of its fundamental features, which allow to improve the basic characteristics of the circuit. We will describe the qualitative features of the novel circuit, analyze it theoretically, and compare it with the standard cascode. We will also present a few results of the development of a cascode with a bandwidth up to 20 GHz.

2 Fundamental

In the framework of this paper we will confine ourselves to the study of a standard (as to the implemented functions) differential cascode, i. e. of a circuit in the form of a differential pair intended to convert the input voltage into output current. We will show that feeding in-phase signal current to emitters of the CB stages and simultaneously the anti-phase input voltage signal to its bases permits of:

- increasing the current gain;
- expanding the bandwidth of the amplified signals;
- modifying, specifically, diminishing the input admittance.

Strictly speaking, such a circuit is no longer a cascode, i. e. a combination of CE-CB stages. Nevertheless, it seems rational to keep this term and, therefore, we call this device hereinafter Differential Cross-Connected Cascode (for brevity - DCC cascode). Its functional circuit is shown in Fig.2 [6].

Let us explain how it works. The transistors T_1 and T_2 are connected in a CE-configuration. Transistors T_3 and T_4 – in a CB configuration. The transistors T_1 and T_3, as well as T_2 and T_4 are connected in series to form two cascodes. The bases T_1 and T_4, T_2 and T_3 are interconnected and form a DCC cascode. The differential input voltages Vin and -Vin are applied to the bases T_1 and T_2 and generate the currents J and -J, which are injected into the emitters of transistors T_3 и T_4. The same input voltages are applied to the bases T_4 and T_3. The base voltages and the base currents of the CB stages are approximately opposite by phase (at low frequency approximation) and are, therefore, perceived by the input voltage sources as negative load impedances.

That is why, the base currents of the CB transistors that are equal to $J\alpha_1(1 - \alpha_2)$ are flowing back to the bases of the CE transistors and are subtracted from the CE base currents $J(1 - \alpha_1)$. As a result, the total input current of the circuit is decreased to the amount of $J(1 - 2\alpha_1 + \alpha_1\alpha_2)$ thus decreasing the cascode input current and its input admittance. In our formulas α_1, α_2 are the collector-emitter current gain for CE and CB transistors accordingly, and J is the emitter current of the CE stage. A more accurate analysis and simulations with account for the relationship α as a function of frequency and time delay show that the real part of the input admittance is getting negative and the imaginary (capacitive) part is getting much smaller as frequencies go up. It can be shown that owing to this phenomenon (negative real part of the input admittance) the magnitude of the input voltage at the inputs of the cross-connected circuit grows at frequencies close to the transistor's maximum operating frequency. As a result, the bandwidth of the circuit can be doubled and the total frequency response flatness is improved.

We want to stress that although we investigate circuits using n-p-n BJT only, all the drawn conclusions are valid for cascodes made of any other amplifying elements.

3 Analysis

3.1 The equivalent circuit and restriction

The goal of our theoretical analysis is to investigate the most important phenomenological features of the novel circuit, but in no way to compare in details the theory with the experimental data. That is why; we used the simplest equivalent transistor circuits and, sometimes, even excluded from the cascode circuit some components, which, although important for its normal functioning, are of minor importance for the analysis of its fundamental features. We used also standard p-type models for the transistors. Formally, these models are suitable for the majority of transistor types. This simple model includes: transconductance Gm, input, output and transient conductances Yp, Yo and Yf. The differential form and cross-connection of the

cascode were reflected by introducing an ideal input signal phase inverter for the CB stage.

First of all, we will investigate the DCC cascode itself and only afterwards its input circuit. To do this we have to establish beforehand some general rules and restrictions.

- In the frame of this work we consider only the circuit with identical transistors in CE and CB cascades. The general case will be consider elsewhere.
- All conductances (resistances) are dimensionless values, normalized on Gm – transconductance CE, so Gm = 1. However, for convenience's sake, the parameter Gm is not replaced by 1 when interpreting the formulae. Where it seems desirable, we will use the substitution Z·Gm = T, for instance, Ze·Gm = Te. Obviously, T is a certain gain factor. The currents and voltages are also dimensionless values.
- In most cases the exact solutions of equation (1) don't have great practical importance, because the transistor model is represented in a simplified form. We assume |Yp|, |Yf|, |Yo| ≪ 1 and |Yf|, |Yo| < |Yp| at all frequencies within the bandwidth of the amplifier and we will, generally, investigate the relationships correct to the terms not higher than the second order relatively to these values and/or their cross-referenced terms of the same order.

3.2 Cascodes with identical transistors

Let us consider at first the simplest DCC cascode made up of idealized and identical transistors Yp ≠ 0, Yf = 0, Yo = 0. The exact solutions are given in Eqs.1 and 2.

$$Yin = \frac{Yp^2}{(Gm+Yp)\left[1+Ze(Gm+Yp)\right]} \qquad (1)$$

$$Gout = \frac{Gm^2}{(Gm+Yp)\left[1+Ze(Gm+Yp)\right]} \qquad (2)$$

Let us consider the input current and, therefore, the input conductance of the DCC cascode, which makes its major distinction from the regular DOC. It follows from the circuit and from the relation (1) as well that the input current represents formally the difference of the two base currents of the transistors CE and CB respectively. However, since the current gain of the cascode is a multiplicative process, the cascode input current contains in fact additive and multiplicative components and this peculiarity is extremely important. The additive components are in opposition and in case of identical transistors they cancel one another. This provides wide opportunities in controlling the input impedance. In turn, the multiplicative components allow, for instance, conversing reactive components into active ones. We have to point out that the hereinafter-discussed possibilities to control the frequency dependence of the input conductance in the neighborhood of the bandwidth boundaries are of crucial importance for solving the problem of expanding the DCC cascode bandwidth. We will investigate a few most interesting particular applications of this method.

We assume Yp = i·x·Gm, where x is a certain relative frequency and x ~ 1 corresponds to a frequency close to the limit one. This, of course, refers to BJT and CMOS transistors as well. Then, proceeding from (1) the dependence of the input conductance $Y_{DCC}(x)$ upon the frequency becomes a very simple one

$$Y_{DCC}(x) = \frac{-Gmx^2}{(1+ix)[1+ZeGm(1+ix)]} \qquad (3)$$

It can be seen from (3) that $Y_{DCC}(x)$ gets a zero value of the second order at x = 0 and two poles on the imaginary axis (at real Ze). At the same time, we can see from (4) that input conductance of the DOC cascode $Y_{DOC}(x)$ gets only one zero at x = 0 and one pole on the imaginary axis.

$$Y_{DOC}(x) = \frac{ixGm}{1+ZeGm(1+ix)} \qquad (4)$$

The fundamental distinction between of two cascodes is shown in Fig.3 representing the characteristic dependences of the real component of the input conductance - curves (1) and (2) - and of its imaginary component - curves (3) and (4) – for both cascode types with the parameter Gm_1 = Ze = 1.

There are two major features: a considerable reduction of the input conductance and a negative real component of the conductance in the amplifier bandwidth. The last feature is linked to the conversion of the purely imaginary (capacitive) conductance into negative real conductance. The dependence of this real component upon the frequency is quadratic at the beginning, but at high frequencies (x ≈ 1) it depends upon the character

and the magnitude of the impedance Ze. Thus, at Im(Ze) = 0 (curve (1) Fig.1), the conductance shows a minimum and is nullified beyond the bandwidth at the point $Xo = (1+1/Ze \cdot Gm)^{0.5}$.
Let us emphasize that the transconductance G(x) of both cascodes is described by the single relationship:

$$G(x) = \frac{Gm}{(1+ix)[1+ZeGm(1+ix)]} \qquad (5).$$

3.3 Total transfer function

The total transfer function of the cascode is the product of the transfer function of cascode itself and transfer function of its input circuit. For the same case of identical ideal transistors Yp = i·x·Gm, Yf=Yo= 0.

$$Y_{21}(x) = \frac{Gm}{1+ix+Tgx^2+Te(1+ix)^2} \qquad (6)$$

Here and hereinafter Te = Gm·Ze and Tg = Gm·Zg. The module $|Y_{21}|$ is of primary interest. The squared denominator (6) is a polynomial of the 4th order in x. With a predetermined deviation |δ| from 1 (|δ| < 1), the optimum transfer function is expressed either by the Butterworth polynomial (δ = 0), or by the Chebyshev polynomial.
Fig.4 shows three transfer functions (6), where (1) and (3) relate to the DCC cascode and function (2) to the regular cascode. The frequency axis x of the function (14) is normalized in such a way, that at x = 1 the gain drop of the regular cascode be equal to –3 dB. Then (1) – the Butterworth characteristic – shows a bandwidth 1.53 times wider and (3) – the Chebyshev characteristic – a bandwidth 2.25 times wider at |δ| = 0.1.
The cause of such an important broadening of the bandwidth at the same transfer function of the cascode itself (5) is evident. At the input of the regular cascode the signal is attenuated owing to the effect of the input capacitive conductance of the CE stage. And on the contrary, the signal is amplified at the input of the DCC cascode at high frequencies owing to the effect of the negative real component of the input conductance (3).

4 Simulation

We have designed and tested several modifications of the cascode circuit using BJT and FET transistors. The work was aimed to verify the increase of the input impedance, current gain and bandwidth expansion of the DCC cascode predicted by the approximation theory as compared to the DOC cascode.
In the framework of this study we intended to minimize the side effects and the influence of secondary factors affecting the investigation results and the circuit comparison, and also to simplify as far as possible the description of the actually used circuits. In this connection simulation has been limited to the most simple cascode circuits Figs.1 and 2. The dc voltage and current sources are ideal ones. The currents, the voltages and all the components of both the investigated circuits and the transistors themselves are identical and shown in Tables 1 (see below). The main parameters of DCC and DOC cascodes designed in IBM SiGe BJT technology are given in the following table.

Table 1.

	T_1...T_4 μ	**Zg Ω**	**Ze Ω**	**Zc Ω**	
DCC	16 x 0.5	50 ‖ 50	1.6	41	
DOC	16 x 0.5	50 ‖ 50	1.6	41	
	Io mA	**Vcc V**	**ß dB**	**Go dB**	**BW GHz**
DCC	4.2	5.1	75	12.2	18.7
DOC	4.2	5.1	38	12.0	8.6

We describe and briefly discuss the simulation results obtained using the SPECTRE CADENCE simulator. Fig. 10 (see below) shows in detail the data regarding the BJT-based cascode. The curves represented on the respective figure are marked in the text as type-"(3)".

4.1 Input conductance

Fig.5 shows the dependence upon frequency of the real (a) and imaginary (b) components of the transistor input conductances CE (1) and CB (2) and also their sum (3) – that is, the input conductance of the DCC cascode. In full concordance with the analysis given before CB (2) transistor conductance is negative resulting in a dramatic reduction of both the components of the cascode input conductance. If the transistors are identical, the real component of the input conductance is always negative within the bandwidth since the delay causes the capacitive component to convert into negative active component.

4.2 Frequency response

The various Gain transfer functions of the cascodes – the main characteristics of any amplifier – are given in Figs.5c,d. As repeatedly pointed out before, the voltage transfer function of the cascode itself (1) is identical for both the circuits. Its bandwidth makes 17.1 GHz. The bandwidth of the voltage transfer functions of the input circuits DCC (2) and DOC (3) cascodes make 29.5 GHz and 11.5 GHz respectively, in full compliance with the formerly carried out analysis (see, e. g. Fig. 6b). The first one shows a maximum of 1.6 dB at the frequency of 12.9 GHz. As a result, the voltage transfer functions of the DCC (4) and DOC (5) cascodes have a bandwidth of 18.7 GHz and 8.6 GHz respectively.

4.3 Current gain

The current gain β of both cascodes is shown in Fig.6. It is evident that β_{DCC} is high and amounts to $\beta_{DCC} \cong \beta_{DOC}^2$ (β_{DOC} - (2)) up to ~1 GHz. Further, $\beta_{DCC} < \beta_{DOC}^2$ and this inequality builds up with frequency.

Obviously this is connected with the effect of the output and transient collector-base impedances, which differ in each of the cascodes.

5 Comparison with Darlington Pair

The DCC cascode and the Darlington pair (hereinafter DP) [1] show similar dependence of the current gain factor ~ β^2. Therefore it is very desirable to compare main features and characteristics of these two circuits. First of all, there is the fundamentally different mechanism of input current reduction. In the DP circuit the high input resistance is provided by negative emitter current feedback, not being linked with the differential circuit structure. On the contrary, the high input resistance in the DCC cascode is provided by positive base current feedback, which is implemented just by the differential circuit structure. Owing to this distinction it is impossible, for instance, to amplify signal in the input circuit of the DP. Detail consideration of the DP shows also that in the most cases it has a considerably narrower bandwidth. It is our opinion that regardless of the formal similarity of certain characteristics, the DCC cascode provides the designer with by far greater opportunities in developing various electronic circuits.

6 Conclusion

The frequency dependences of the input impedances and transfer functions inherent to these circuits have proven to coincide and the approximately twofold bandwidth expansion and the considerable increase of the current gain and input impedance predicted by the theory have been confirmed.

Owing to these features the DCC cascode provides essentially better parameters as compared to the regular cascode [6] in all circuits implemented in our development work using BJT and CMOS transistors.

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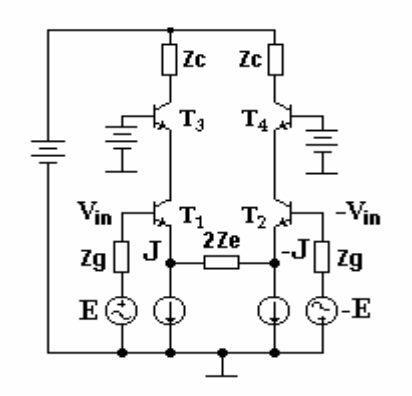

Fig. 1 DOC – Differential Ordinary Cascode schematic.

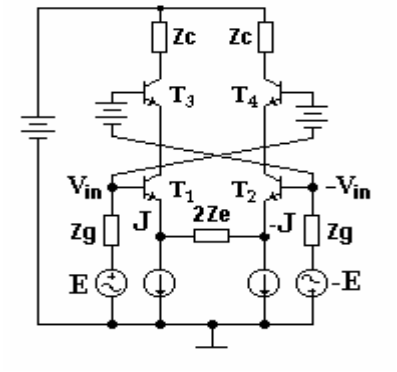

Fig.2 DCC - Differential Cross-Connected cascode schematic.

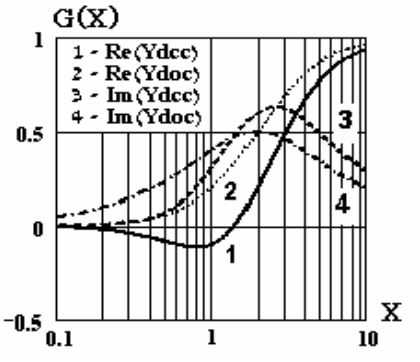

Fig.3. Frequency dependencies of the input conductance of DOC and DCC cascodes.

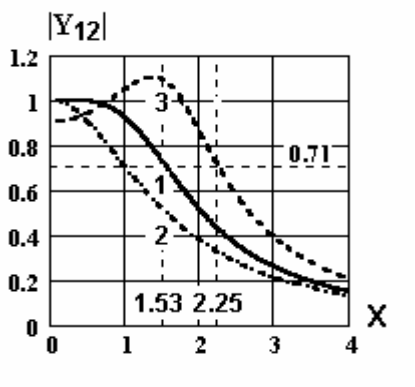

Fig.4. Frequency transfer functions of DOC and DCC cascodes: 1 Butterworth characteristic of DCC cascode (T=1, Tg=1.25), 2 Butterworth characteristic of DOC cascode (Te=1, Tg=1.25), 3 Chebyshev characteristic of DCC cascode (Te=1, Tg =4.29, δ=0.1).

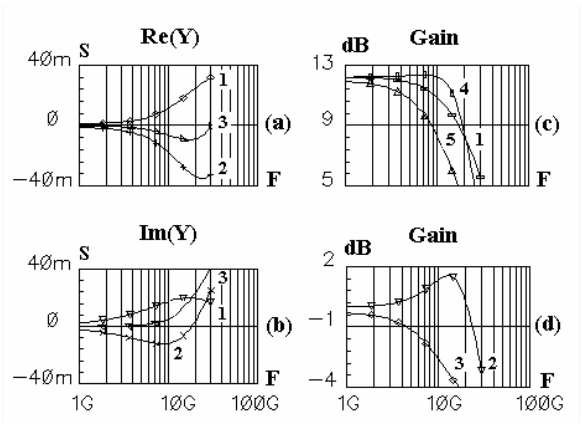

Fig.5 BJT-based DCC and DOC cascodes. Simulation results (see description in the text).

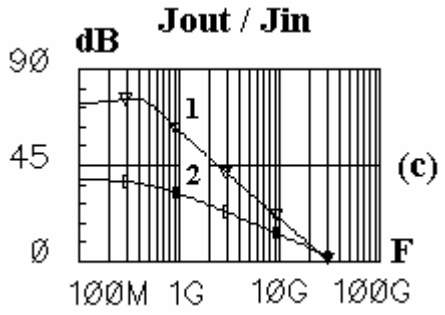

Fig.6 Current gain of DCC (1) and DOC (2) cascodes