

A 23dB 7GHz Bipolar Wideband Amplifier

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Abstract: - In this work we report an inductor-less, two stage wideband amplifier with a gain of 23.5 dB and a 3-dB bandwidth of 7 GHz. It employs the pole zero cancellation technique to realize the aforesaid characteristics. It exhibits a low noise figure of 3.6 ~ 4.3 dB in the entire operating range. The power consumption of the circuit is around 30mW with a 3 Volt supply.

Key-Words: - Bipolar Wideband Amplifier, inductor-less, pole zero cancellation

1 Introduction

In recent years, wideband amplifiers have proven their significance in commercial communication devices like optical receivers, video amplifiers, cable television applications, etc. One of the key challenges in the design process is to minimize the cost by reducing the component count and thus the die area. The cost minimization can be achieved by choosing among the cheapest device fabrication technology.

Cascoding [5] and capacitive feedback [1], [2] are some of the techniques to improve the bandwidth of an amplifier. Moreover [3] uses a DC coupled amplifier with a Darlington configuration in the second stage. This increases the bandwidth, by providing low impedance to the first stage. Peaking capacitor technique [4] is one of the well known methods to improve bandwidth, but is very sensitive to process variations. Cascoding pushes the input dominant pole further in frequency thus increasing the bandwidth. But this technique is not effective for high speed bipolar circuits due to the dominant pole created by the output parasitic capacitance. Some bandwidth enhancement techniques employ active feedback networks to provide positive feedback at high frequencies which nullify the effect of poles. However, such procedures require additional active devices which tend to increase the noise figure of the amplifier.

Gain-bandwidth product can be increased by proper positioning of the poles as demonstrated by [1], [2]. In this work, we have used a combined approach of pole-zero cancellation along with re-arrangement of poles and zeros which maximizes gain-bandwidth product for the topology under consideration.

2 Circuit design

The proposed amplifier consists of two common emitter stages with a DC coupling. The bandwidth enhancement is achieved by using a balanced feedback technique. The two R-C feedback pairs are responsible for generation of zeros in the transfer function of the amplifier. The design is simulated incorporating the bond-wire inductance of 3nH from the power supply. Low noise is achieved by biasing the transistors at near optimum current levels.

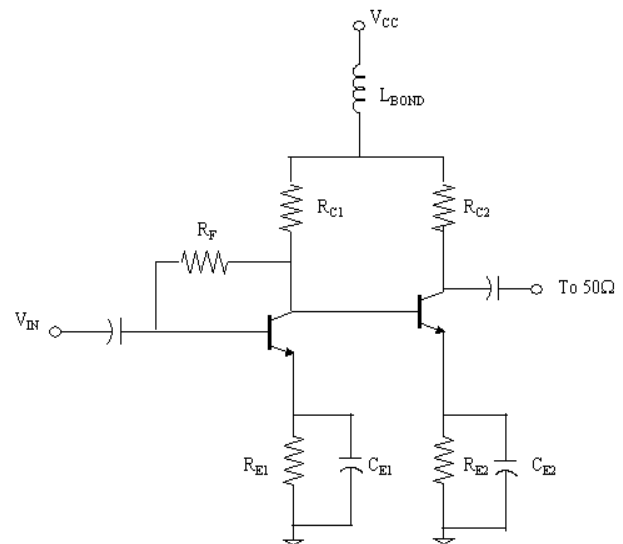


Fig 1 Circuit Configuration of the proposed amplifier

In Fig 1, the base biasing resistor R_F also acts as a negative feedback resistor which enhances the bandwidth of the first stage. The base biasing of the transistor in the second stage is achieved by using the collector voltage of the transistor in the first stage. R_{C1} and R_{C2} primarily determine the gain; R_F , $R_{E1}-C_1$ and $R_{E2}-C_2$ determine the bandwidth.

3 Circuit Analysis

The small signal AC equivalent circuit of the proposed amplifier is shown in Fig 2.

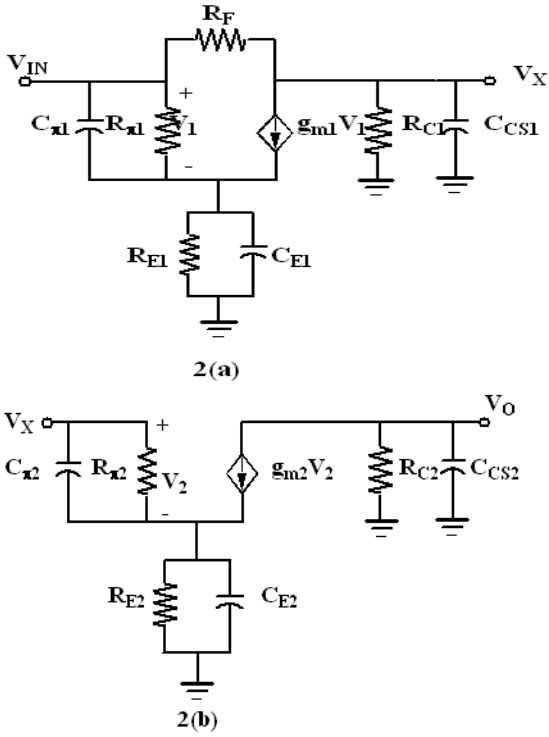


Fig 2 Small signal equivalent of the circuit in Fig 1 2(a) first stage, 2(b) second stage

From the small signal analysis of the circuit in Fig 2, the dominant poles and zeros are found to be

$$P_0 = \frac{R_{\pi 1} + \beta_1 R_E}{R_{\pi 1} R_{E1} (C_{E1} + C_{\pi 1})}$$

$$P_1 = \frac{1}{R_{C2} C_{CS2}}$$

$$P_2 = \frac{1 + g_{m2} R_{E2}}{R_{E2} (C_{E2} + C_{\pi 2})}$$

$$Z_0 = \frac{R_{\pi 1} + \beta_1 (R_{E1} - R_F)}{R_{E1} C_{E1} (R_{\pi 1} - \beta_1 R_F) + R_{E1} R_{\pi 1} C_{\pi 1}}$$

$$Z_1 = \frac{1}{R_{E2} C_{E2}}$$

The pole P_1 is found to be at 9.323 GHz. The values of R_{E2} and C_{E2} are chosen in such a manner that the zero Z_1 cancels the pole P_1 . The zero Z_0 is found to be at 1.579 GHz. The pole P_0 is found to be at 3.94 GHz and the pole P_2 at 22.29GHz. Hence, it is observed that the zero is prior in frequency to the poles P_0 and P_2 of which, the pole P_2 is at a very high frequency.

4 Simulation Results

The bipolar transistor model used for simulations has the parameters shown in table 1. All the simulations have been performed in Agilent ADS.

Table 1 BJT model parameters

Parameter	Value
C_{JC}	16.68fF
C_{JE}	33.25fF
C_{CS}	180fF
I_S	10.42aA
β	145
F_{TMAX}	27GHz

The simulated frequency response of the circuit is shown in Fig 3(a). A sudden rise in the gain is observed around 2GHz, which is due to the zero Z_0 . The gain at 10GHz is around 16dB. The -3dB frequency is 6.98GHz and the gain peaking is within 1dB. If the effect of bond wire is not considered, the bandwidth drops to 6.8GHz. The input and output reflection coefficients of the circuit are shown in Fig 3(b). Fig. 5 shows the plot of noise figure of the circuit and the minimum achievable noise figure for this topology.

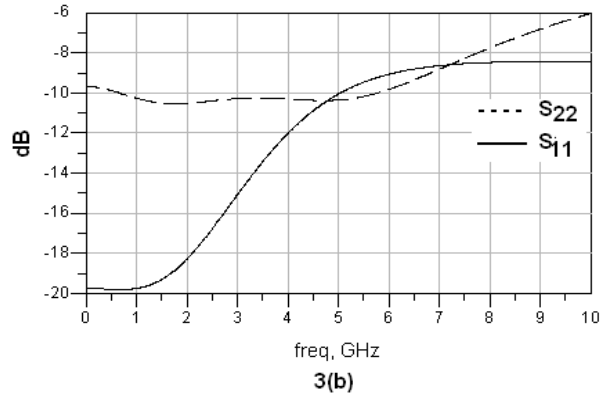
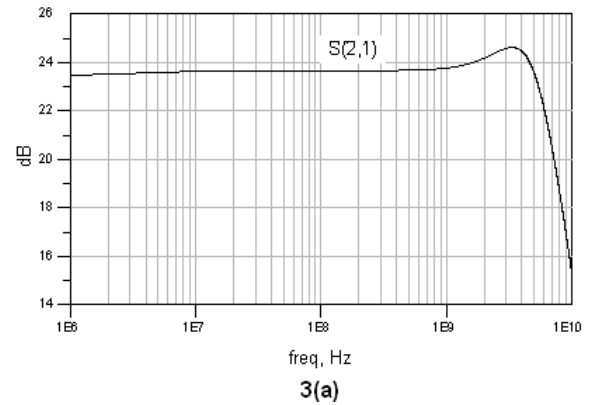


Fig 3 (a) Simulated S_{21} and (b) Simulated S_{11} and S_{22} against frequency

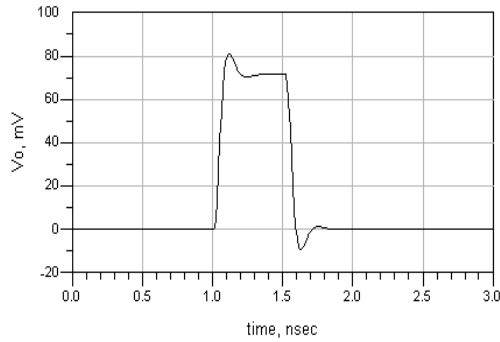


Fig 4 Transient response of the circuit to a 0.5nSec pulse

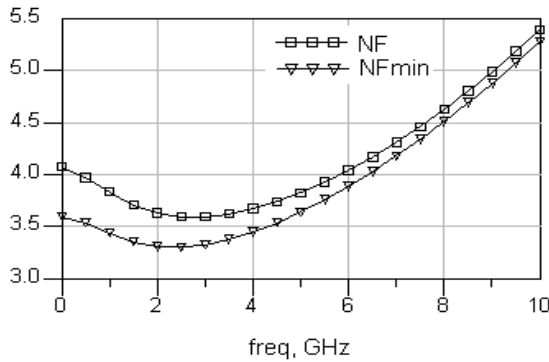


Fig 5 Noise Fig of the proposed circuit

Table 2 Change in gain and bandwidth with component variation

Component variation	Gain variation	Bandwidth variation
C_1 $\pm 10\%$	$\pm 0\%$	$\pm 0.43\%$
R_{E1} $\pm 10\%$	$\pm 0.8\%$	$\pm 2.48\%$
C_2 $\pm 10\%$	$\pm 0\%$	$\pm 1.73\%$
R_{E2} $\pm 10\%$	$\pm 3\%$	$\pm 4.5\%$

In Table 2, the variation in R_{E2} affects the gain and bandwidth the most. This is because the zero Z_1 and g_{m2} depend on R_{E2} . Also, g_{m2} variation affects P_2 as well as the gain. Table 3 shows that this work displays a marked improvement of around 17% in gain-BW product in comparison to [1].

Table 3 Gain-BW Comparison

Topology	Gain-BW product
Differential pair (DP)	54.56
DP with emitter degeneration	74.72
Reference [3]	77.4
Vadipour topology [2]	110.4
Reference [1]	140.8
This work	164.5

5 Conclusion

In conclusion, the simulated frequency response of the amplifier was in good agreement with the calculated values of poles and zeros of the circuit. The emitter degeneration RC networks in the circuit can be used to balance out the effect of circuit poles. This implies that the voltage series negative feedback in an amplifier is an introduction of a zero in its transfer function.

References:

- [1] F. Centurelli, R. Luzzi, M. Olivieri and A. Trifiletti, "A Bootstrap Technique for Wideband Amplifiers", *IEEE Transactions on Circuits and Systems-I Fundamental theory and Applications*, Vol.49, No.10, Oct 2002, pp. 1474-1480.
- [2] M. Vadipour, "Capacitive feedback techniques for Wideband amplifiers", *IEEE Journal of Solid State Circuits*, Vol.28, No.1, 1993, pp. 90-92.
- [3] C. Loh, "Low Cost DC to 3.6GHz Silicon Broadband Amplifier", *2003 Asia-Pacific Conference on Applied Electromagnetics*, Aug 2003, pp. 72-75.
- [4] Y. Akazawa, N. Ishihara, T. Wakimoto, K. Kawarada and S. Konaka, "A Design and Packaging technique for a high-gain, gigahertz-band single-chip amplifier", *IEEE J. Solid State Circuits*, Vol.SC-21, 1986, pp. 417-423.
- [5] P.R. Gray and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, New York: Wiley, 1984