

Fast Acquisition Digital Tanlock Loop with Adaptive Time Delay

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Abstract: - In this paper, a novel approach that enhances the locking and acquisition characteristics of the Time Delay Digital Tanlock Loop is developed. The idea revolves around replacing the single time delay unit with a dual time delay structure. This approach extends the tracking range of the loop and exploits the desired characteristics induced by each time delay on its own. Simulation results of the new structure show that the newly developed loop can offer rapid acquisition and good tracking performance over a wide locking range. Application of the loop to the demodulation of FSK signal is demonstrated.

Key-Words: - Digital Phase-Locked Loops, Tanlock Loops, Adaptive Time Delay.

1 Introduction

Phase-Locked Loops are used in a variety of communication, control and signal processing applications [1]. Digital Phase-Locked Loops (DPLLs) have been introduced to overcome the problems associated with their analogue counterparts particularly in the applications of subcarrier tracking and bit synchronization of digital data stream. The use of DPLLs alleviates other problems inherent with the analog PLL such as aging, component tolerances and dc drift [2]. One of the most promising DPLLs is the Digital Tanlock Loop, which offered many advantages over other architectures such as the linearity of its phase characteristics and insensitivity to fluctuations of the signal power [3].

Recently, a modified architecture of the original Digital Tanlock Loop, called the Time Delay Digital Tanlock Loop (TDTL), has been introduced. The modified architecture overcomes the complexities of designing the Hilbert transformer, which is an essential part of the Conventional Digital Tanlock Loop [4]. However, the linearity of the phase error and the locking range characteristics are no longer preserved in some parts of the locking region. The time delay is a dictating parameter in defining the locking range and the frequency acquisition characteristics of the TDTL [4,5].

This paper proposes a novel structure of the TDTL that utilizes the best behavior of the loop in terms of carrier acquisition characteristics over a wide locking range. This is achieved by utilizing two time

delay blocks, exhibiting different phase shifts, instead of a single one.

The following section describes the structure of the proposed loop and presents an analysis of the main mathematical principles underlying the operation of the loop. Section 3 shows the results of the system simulation under different operating conditions.

2 Loop Structure and Analysis

2.1 Loop Structure

The proposed loop architecture is depicted in Fig. 1. It is composed mainly of two sample and hold blocks, Sampler 1 is preceded by two time delay units, whereas Sampler 2 has the same input signal as that of the loop.

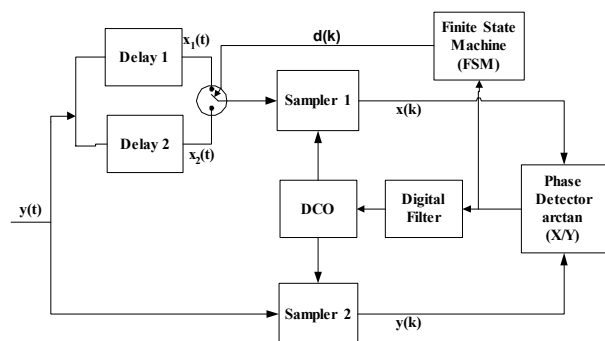


Fig. 1 Adaptive Time Delay DTL

The generated samples from both arms of the loop are fed to a phase detector, which has a characteristic function of $\tan^{-1}(y/x)$, generating an error signal. This error signal will be applied to a

digital filter, in order to produce a driving signal for the Digitally-Controlled Oscillator (DCO), which is merely a variable-period clock triggering the sample and hold blocks. The Finite State Machine (FSM) will decide, according to the phase error, which of the delayed signals will pass to Sampler 1.

2.2 Loop Analysis

The input to the loop is assumed to be a continuous-time sinusoidal signal with AWGN (Additive White Gaussian Noise) follows

$$y(t) = A \sin[\omega_o t + \theta(t)] + n(t) \quad (1)$$

Where A is the amplitude of the signal, ω_o is the free running frequency of the DCO, $\theta(t)$ is the information bearing phase and $n(t)$ is the AWGN. Assuming a frequency step at the input then the phase process will be

$$\theta(t) = (\omega - \omega_o)t + \theta_o \quad (2)$$

Where ω is the radian frequency of the input signal and θ_o is a constant. A phase lag $\Psi_i = \omega \tau_i$, where $i \in \{1, 2\}$ will be induced on the input signal after it passes through two time delay units τ_1 and τ_2 . Therefore, the following signals will be generated

$$x_1(t) = A \sin[\omega_o t + \theta(t) - \Psi_1] + n'_1(t) \quad (3)$$

$$x_2(t) = A \sin[\omega_o t + \theta(t) - \Psi_2] + n'_2(t) \quad (4)$$

Where $n'_i(t)$ is the time delayed AWGN due to τ_i . The control signal $d(k)$ will decide which of the signals specified by (3) and (4) will be passed to Sampler 1, similarly, $y(t)$ will be passed to Sampler 2 producing the following discrete time signals

$$y(k) = A \sin[\omega_o t(k) + \theta(k)] + n(k) \quad (5)$$

$$x(k) = A \sin[\omega_o t(k) + \theta(k) - \Psi_i] + n'_i(k) \quad (6)$$

Where $t(k)$ denotes the total time elapsed up to the k -th sampling instant. The sampling interval of the DCO between the sampling instants $t(k+1)$ and $t(k)$ is given by

$$T(k) = T_o - c(k-1) \quad (7)$$

Where $T_o = 2\pi / \omega_o$ is the free-running period of the DCO, and $c(k-1)$ is the output of the digital filter at the previous sampling instant. The total time up to the k -th sampling instant can be defined as

$$t(k) = \sum_{i=1}^k T(i) = kT_o - \sum_{i=0}^{k-1} c(i) \quad (8)$$

And consequently the phase error between the input signal and the DCO is given by

$$\phi(k) = \theta(k) - \omega_o \sum_{i=0}^{k-1} c(i) - \Psi_i \quad (9)$$

Now, (5) and (6) can be redefined as

$$y(k) = A \sin[\phi(k) + \Psi_i] + n'(k) \quad (10)$$

$$x(k) = A \sin[\phi(k)] + n(k) \quad (11)$$

These signals will be applied to the phase detector producing the error signal $e(k)$ given by

$$e(k) = f \left[\tan^{-1} \left(\frac{\sin[\phi(k)]}{\sin[\phi(k) + \Psi_i]} \right) \right] + \zeta(k) \quad (12)$$

Where $f(\gamma) = -\pi + [(\gamma + \pi) \bmod 2\pi]$, $\zeta(k)$ is a random phase disturbance due to AWGN. The error signal $e(k)$ will serve as an input to the digital filter whose transfer function is $D(z)$ and its output is the signal $c(k)$ that will drive the DCO. Therefore, the system difference equation can be derived from (7) and (9) as

$$\phi(k+1) = \phi(k) - \omega c(k) + A_o \quad (13)$$

Where $A_o = 2\pi(\omega - \omega_o) / \omega_o$. Unlike the single delay TDTL, the dual delay variant allows for the exploitation of the influences of changing the value of the time delay, which affects the performance of the loop in terms of the locking range and the acquisition speed [4,5].

In the first order loop, the digital filter comprises only a gain block G_1 , causing the system equation to be redefined as

$$\phi(k+1) = \phi(k) - K'_1 h[\phi(k)] + A_o \quad (14)$$

Where $K_1' = \omega G_1$ and all AWGN terms are neglected since noise free analysis is to be performed. Defining K_1 as $\omega_o G_1$ will result in $K_1' = K_1 / W$, where $W = \omega_o / \omega$. The nominal phase lag Ψ_{oi} induced by the time delay units on the input can be initially arranged by manipulating the parameters ω_o and τ_i in the manner given by $\Psi_{oi} = \omega \tau_{oi}$. Following the analysis in [4], the lock range of the first order loop can be found by numerically solving the inequalities given by

$$K_1 < 2W \frac{\sin^2(\alpha) + \sin^2(\alpha + \Psi_{oi}/W)}{\sin(\Psi_{oi}/W)} \quad (15)$$

$$K_1 > 2|1 - W| \quad (16)$$

Where $\phi_{ss} = \sigma + j\pi$, $j \in \{1, 0, -1\}$ ϕ_{ss} is the steady state phase error.

Fig. 2 shows the locking range for $\Psi_{o1} = \pi/2$ and $\Psi_{o2} = \pi/3$. It can be clearly seen from Fig. 2 that the locking boundary curves defining each lock range are in parts nonlinear, and the areas covered by each curve differ in terms of the loop gain and the frequency range.

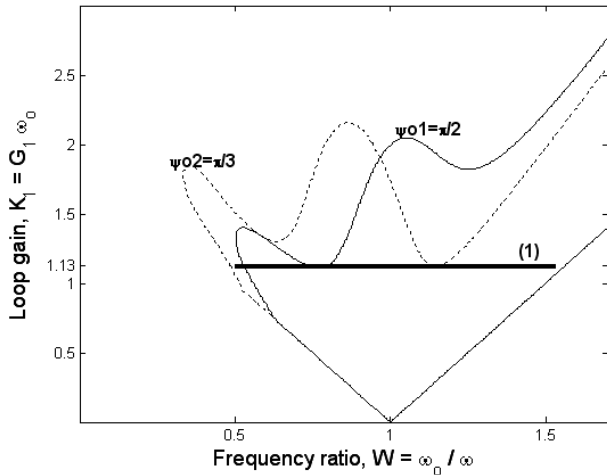


Fig. 2 Locking Range of First Order TDTL with different values of Ψ_o , the Tracking Range is the Bold Line (1).

Since the value of the time delay is of great influence on the convergence behaviour of the loop [5]. The conflicting requirements of fast acquisition and wide locking range necessitate adopting more than one time delay.

In the proposed system, the time delay units have been arranged so that $\Psi_{o1} = \pi/2$ and $\Psi_{o2} = \pi/3$, this will ensure a symmetric tracking range from $W = 0.5$ up to $W = 1.5$. Hence, the system will exploit the good range and acquisition characteristics of Ψ_{o1} in the area where $W > 1$, and of Ψ_{o2} in the area where $W < 1$. The loop gain $K_1 = 1.13$ has been selected to ensure good performance and wide locking range for both values of the time delay.

The states of the FSM are defined by the phase error and the control signal $d(k)$, if the system is subjected to a frequency step which causes the input signal frequency to go higher than ω_o , i.e. $W < 1$ and the phase error is greater than a predefined threshold $\varepsilon_1 > 0$, the control signal $d(k)$ will allow the signal $x_2(t)$ to pass to Sampler 1, whereas if the system is subjected to a frequency step which causes the input frequency to go lower than ω_o , i.e. $W > 1$, the FSM will monitor the phase error until it is below another threshold $\varepsilon_2 < 0$, then the control signal $d(k)$ will allow the signal $x_1(t)$ to pass to the sampler. The parameters ε_1 and ε_2 allow fine-tuning of the FSM behavior for any intended region of operation of the loop in order to ensure fast acquisition behavior.

3 System Simulation Results

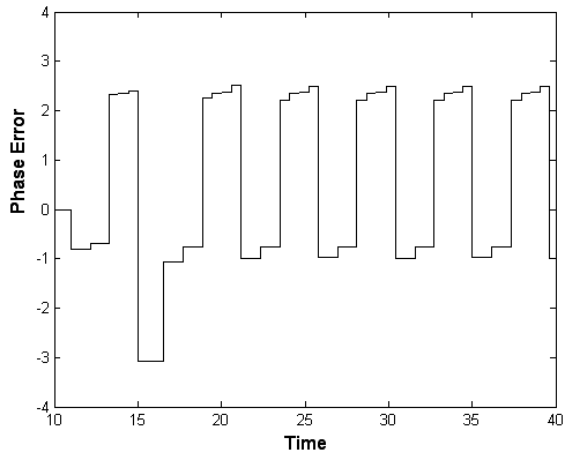
Fig. 3 (a) shows the transient response of the single delay loop with $\Psi_{o1} = \pi/2$ and $K_1 = 1.13$ to a frequency step with $W = 0.5$. Since this mode of operation is outside the locking range of the loop, the phase error will diverge resulting in an unstable state, thus throwing the loop in the unlocked mode.

This is also illustrated in Fig. 3 (b), which shows the phase plane plot for the same frequency step, where it is clear that the phase will not converge to a steady state value.

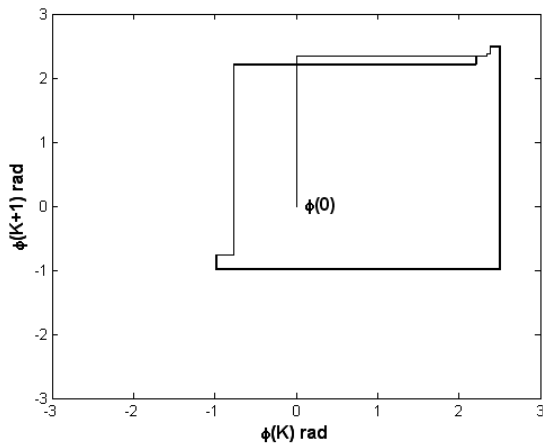
The result of applying the same frequency step to same TDTL but with $\Psi_{o2} = \pi/3$ is shown in Fig. 4 (a). It can be clearly seen that the phase error will settle to a steady state value within a few samples.

This property is of great importance for a wide range of communication and signal processing applications. The same behavior is also illustrated by the phase plane plot shown in Fig. 4 (b), where

the phase error converges rapidly to a steady state value.



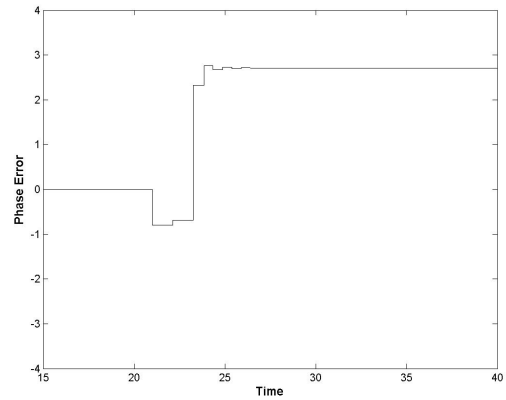
(a)



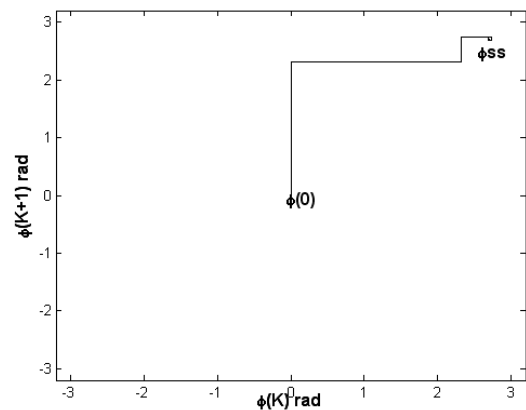
(b)

Fig.3 (a): Transient Response of the Single Delay TDTL with $\Psi_{o1} = \pi/2$ and $K_1=1.13$ to a frequency step with $W = 0.5$ (b) Phase Plane Behavior

The solid performance of the loop can also be demonstrated for frequency steps less than ω_o , i.e. $W > 1$, as shown in Fig. 5, which shows the transient response of the single delay TDTL with $\Psi_{o2} = \pi/3$ and $K_1=1.13$ to a frequency step with $W = 1.25$. The response of the loop under the aforementioned parameters is poor, and it is clear that the phase error is not converging to a steady state value within an acceptable time. Whereas the transient response of the same TDTL with $\Psi_{o1} = \pi/2$ for the same frequency step, demonstrated in Fig. 6, shows that the phase error converges to a steady state value in two samples.



(a)



(b)

Fig.4 (a): Transient Response of the Single Delay TDTL with $\Psi_{o2} = \pi/3$ and $K_1=1.13$ to a frequency step with $W = 0.5$ (b) Phase Plane Behavior

A Potential application of the adaptive delay TDTL, with wide locking range and fast acquisition characteristics described above, is FSK demodulation. The single delay TDTL might not respond within an adequate time to some frequency changes as demonstrated by the FSK demodulated signal of Fig. 7, where the settling in the response to the higher frequency W_1 is lasting for more than five samples.

In addition to settling, the single delay TDTL imposes restrictions on the Symbol Rate R_s , in this example β , which is the ratio between the free running frequency of the loop f_o and the symbol Rate R_s , is equal to 20 in order to allow enough time for the loop to settle for each symbol. The adaptive delay TDTL overcomes this limitation owing to its fast acquisition characteristics. As

illustrated in Fig. 8, the loop can respond rapidly to the modulating frequencies and settle within two samples. In addition to that, the symbol rate can be increased allowing for high data transmission rate, in this example β has been decreased to 7.5.

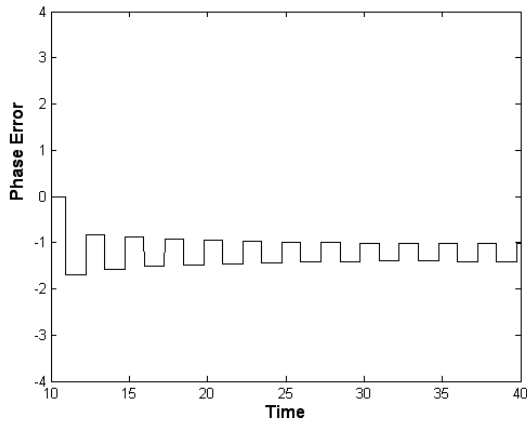


Fig. 5: Transient Response of the Single Delay TDTL with $\Psi_{o2} = \pi/3$ and $K_1=1.13$ to a frequency step with $W = 1.25$

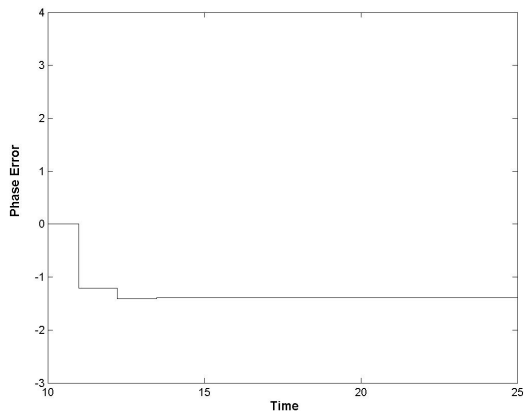


Fig. 6: Transient Response of the Single Delay TDTL with $\Psi_{o1} = \pi/2$ and $K_1=1.13$ to a frequency step with $W = 1.25$

4 Conclusion

A new Digital Tanlock Loop with adaptive time delay has been proposed and the mathematical analysis governing its performance has been outlined. The loop exchanges the single time delay with a dual structure in order to take advantage of the best characteristics of the individual loops. The loop utilizes the best performance for $1 > W > 1$.

The loop has been simulated using MATLAB/SIMULINK. The results reported above

demonstrate the superior performance of the loop by its ability to rapidly track all inputs within the locking range. The application of the adaptive delay loop in the demodulation of FSK signals was demonstrated with satisfactory performance.

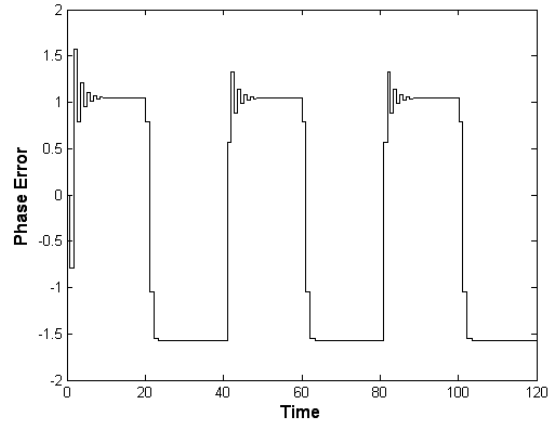


Fig. 7: FSK Demodulation Using the Single Delay TDTL with $\Psi_{o1} = \pi/2$, $W_1 = 0.83$, $W_2 = 1.25$, $K_1=1.13$ and $\beta=20$.

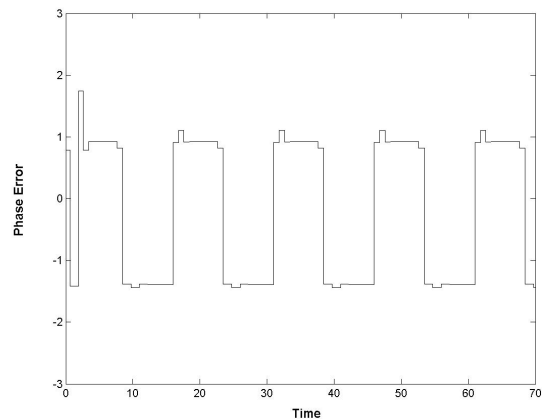


Fig. 8: FSK Demodulation Using the Adaptive Delay DTL with $W_1 = 0.83$ and $W_2 = 1.25$ and $\beta=7.5$

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