

TESTABILITY STRUCTURE FOR CONTINUOUS TIME ANALOG FILTERS IN MIXED-SIGNAL DEVICES

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ABSTRACT

This paper discusses the importance and difficulties associated with testing analog circuits in general and those residing within mixed-signal circuits in particular. It proposes a tested method that is not specification oriented. The method is based on the excitation of the circuit-under-test with a pseudo random binary sequence and the subsequent analysis of the captured response. The fault detection capabilities of the test and data analysis methods are demonstrated by applying them to a continuous time filter circuit operating in the mid-band frequency range. The paper then explores the impact of the test sequence length on the detectability of faults. It also proposes a design for testability structure that supports the proposed test technique.

Keywords: Analog, Mixed-Signal, Test, Testability, Fault

1. INTRODUCTION

The demand for analog circuits in the present digital age is increasing. This is due to the fact that most digital systems need to process information that is analog in nature. The increase in the demand and improvements in the manufacturing process resulted in mixed-signal circuits in which the analog and digital modules are integrated within the same chip. These devices are nowadays developing into systems-on-chip (SOC). Such systems within a single chip offer substantial improvements in performance and reduction in cost. Application areas of SOCs include telecommunications, computers, consumer electronics, and automotive industry.

Testing and characterizing circuits, be it digital, analog or mixed-signal prior to the integration into larger systems is extremely important. In the case of digital circuits, which have extremely high density, enormous advancements have been and continue to be achieved in testing, design for testability (DFT) and built-in self-test (BIST) aspects of such devices [1]. However, such advancements have not been paralleled in the analog circuits domain due to the non-structured nature of analog circuits, continuous behavior, wide variety of modes of failure, tolerance and drift problems, specification oriented testing, and inefficient device based simulations [2,3].

In the case of a mixed-signal environment the task of testing the analog modules is even more difficult than that of testing the same module in an all-analog environment. This is due to the difficulties associated with testing analog circuits, which were outlined above, and the lack of controllability and observability of embedded circuit modules. The testing task is exacerbated further by the presence of interface circuit block, such as analog-to-digital and digital-to-analog converters, and

other circuit modules (e.g. switched capacitor circuits) that exhibit both analog and digital characteristics.

Continuous-time analog filter circuits form an important part of many types of mixed-signal circuits. This paper presents a detailed experimental study of testing active analog filter circuits. The study assesses the effectiveness of a test technique, presented in section 3, at detecting single catastrophic and soft fault conditions as discussed in section 2. Section 4 discusses an analysis method that evaluates the confidence in the detection process. Section 5 presents the results of testing a second-order continuous-time state variable filter circuit. Section 6 explores the impact of the test sequence length on the detectability of the injected faults. Then section 7 proposes a feasible design for testability structure that supports the proposed test method.

2. FAILURES AND FAULT MODELS

Many types of failure mechanisms affect the operation and performance of integrated circuits [4]. These mechanisms, may lead to a wide variety of faulty circuit behavior that are technology, layout and process dependent. To represent the behavior of defective integrated circuits, fault models are used.

Fault models serve two purposes during the testing process. First, they help generate tests that verify the correct functionality of the circuit. Second, they help evaluate test quality defined in terms of coverage of modeled faults. In general, faults in an integrated circuit (IC) basically fall into two categories: catastrophic faults (hard faults) or parametric faults (soft faults).

Catastrophic faults are random defects, which cause structural deformations leading to hard failures such as shorts and opens, in an IC component. Examples of random defects include over or under etching of various layers, oxide pinholes, spot defects, and photolithographic errors. Parametric faults are excessive statistical variations in the manufacturing process conditions, such as a turbulent flow of gasses and inaccuracies in the control of furnace temperature, which cause a soft failure of components of an IC. A soft failure is one which is not sufficient to result in a completely malfunctioning IC, but sufficient to cause performance to deviate outside the limits of the allowable tolerance region. An example of a parametric fault is a deviation in the width-length ratio of a transistor causing the gain of the device not to meet the specifications.

For digital circuits many fault models that cover both catastrophic and parametric faults have been proposed in the literature [1]. These models enable efficient testing of digital circuits using an optimum set of test vectors. Unfortunately, equivalent models do not exist for analog circuit. Therefore, the simple fault model illustrated in (Figure 1) is adopted in this paper to evaluate the applicability and fault coverage of the testing

techniques proposed in the paper. The model shows the catastrophic faults in resistors, capacitors and MOS transistors. A short circuit is represented by $R_s=1.0\Omega$, while an open circuit is represented by $R_o=100M\Omega$. The faults synthesized by the model can be simulated using a device level circuit simulator such as SPICE.

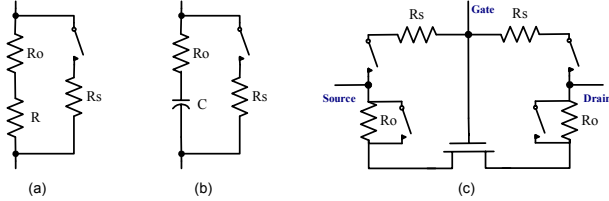


Figure 1: Fault Models (a) Resistor, (b) Capacitor, (c) MOS

3. TEST METHOD AND INPUT SIGNAL

The proposed testing method is based on the excitation of the analog circuit being tested with a sequence of pulses, and subsequent comparison of the captured circuit response with a signature of the known fault-free response.

Testing by applying a sequence of pulses with varying amplitudes was discussed in [5]. In the proposed test method the type of test sequence to be applied to an analog circuit under test (CUT) is a PRBS (pseudo random binary sequence). The PRBS is chosen because it can be easily generated, it is compatible with digital DFT and BIST circuitries, such sequences have well defined properties [6] and can be used to estimate the impulse response of the analog CUT as outlined below.

For an analog CUT with an impulse response $h(t)$, the output $y(t)$ is given by Equ.(1). The cross-correlation between $x(t)$ and $y(t)$ is defined by Equ.(2). Manipulating Equ.(2) results in Equ.(3).

$$y(t) = \int_{-\infty}^{\infty} h(u) x(t-u) dt \quad (1)$$

$$\begin{aligned} \Phi_{xy}(\tau) &= \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T x(t) y(t+\tau) dt \\ &= \lim_{T \rightarrow \infty} \frac{1}{T} \int_0^T x(t) \int_{-\infty}^{\infty} h(u) x(t+\tau-u) du dt \end{aligned} \quad (2)$$

$$\Phi_{xy}(\tau) = \int_{-\infty}^{\infty} h(u) \Phi_{xx}(\tau-u) du \quad (3)$$

Equ.(3) shows the cross-correlation between the input $x(t)$ and the output $y(t)$ is the convolution of the impulse response $h(t)$ with the auto-correlation of the input signal. If the input signal consists of broadband white noise then its auto-correlation function $\Phi_{xx}(\tau)$ would be an impulse response. The reason being that a noise signal only correlates with itself at $\tau=0$. Therefore, it follows from Equ.(3) that for broadband noise input the output $\Phi_{xy}(\tau)$ would result in a direct measure of $h(\tau)$, as indicated by Equ.(4).

$$\Phi_{xy}(\tau) = \int_{-\infty}^{\infty} h(u) \delta(\tau-u) du = h(\tau) \quad (4)$$

Taking the Fourier transform of both sides of Equ.(3) and doing a bit of manipulation gives

$$H(\omega) = \frac{S_{xy}(\omega)}{S_{xx}(\omega)} \quad (5)$$

where $S_{xy}(\omega)$ is the cross-power spectral density of $x(t)$ and $y(t)$, $S_{xx}(\omega)$ is the auto-power spectral density of $x(t)$, and $H(\omega)$ is the transfer function. The impulse response can be extracted by taking the inverse Fourier transform of Equ.(5).

The generation of the broadband white noise input signal required by Equ.(4) is normally very difficult to achieve. However, PRBS signals have very good randomness properties and are a very good approximation to the required white noise signal. Equations (1) through (5) above outline the theoretical justification for using PRBS as the input test signal and some of the possibilities for analyzing the response that such input signals generate.

4. ANALYSIS OF TEST DATA

The transient response data captured at the output of an analog CUT is analyzed to determine if the fault has been detected or not and to establish the relative confidence level in the detection.

The detection method used in this paper is based on comparing the signatures of the auto-correlation and cross-correlation functions of the fault free circuit with those of the CUT. To take into account deviations in the component values from the ideal ones, tolerance analysis is carried out using Monte-Carlo method. This establishes an envelope around the nominal response indicating the acceptable bounds of the circuit performance and constitutes the signature of the fault-free circuit.

Single catastrophic and soft fault conditions are introduced to the CUT, and the auto and cross correlation functions are computed and compared with those of the tolerated fault-free circuit. If either of the correlation function of the CUT generates a signature that falls outside the boundaries of the tolerance window of the corresponding fault-free correlation function on at least one instant, then that fault is considered detectable. This means that the width of the tolerance window will affect the probability of detecting a particular fault.

To measure the relative confidence in the ability to detect a fault by the method outlined above, and to compare the detectability of the same fault by the auto and the cross correlation functions, a figure of merit RDCL (Relative Detection Confidence Level) is computed for every fault condition that was detected at least at one instant. RDCL is defined by Equ.(6).

$$RDCL = \left(\frac{D_n}{S_n} \right) * \sum_{i=1}^{S_n} |Yf_i - Yfr_i| \quad (6)$$

where

$i = 1, 2, \dots, S_n$	
Yf	CUT response
Yfr	Fault-Free response
S_n	Total no. of samples

D_n No. of detection instances

The fault coverage (F_C) achieved by a particular test method or measured parameter is given by Equ.(7)

$$F_C = \left(\frac{F_D}{F_I} \right) * 100\% \quad (7)$$

where F_D and F_I refer to the number of the detected and injected faults respectively. The results of applying the test strategy and the associated data analysis method are discussed in the next section.

5. CONTINUOUS TIME FILTER CIRCUIT

The testing technique and data analysis method presented in the preceding sections were applied to the continuous-time state-variable benchmark circuit [7] shown in Figure 2 below. The circuit incorporates low-pass, band-pass and high-pass filters. The values of the components used are: $C1=C2=20nF$, $R1=R2=R3=R4=R5=10k\Omega$, $R6=3k\Omega$, and $R7=7k\Omega$. The fault-free frequency responses of the circuit, at the low-pass, band-pass and high-pass output nodes, are depicted in Figure 3.

The band-pass, low-pass, and high-pass transfer functions of the second-order state-variable filter [8-9] in Figure 2 are given by Equ.s (8), (9) and (10) respectively.

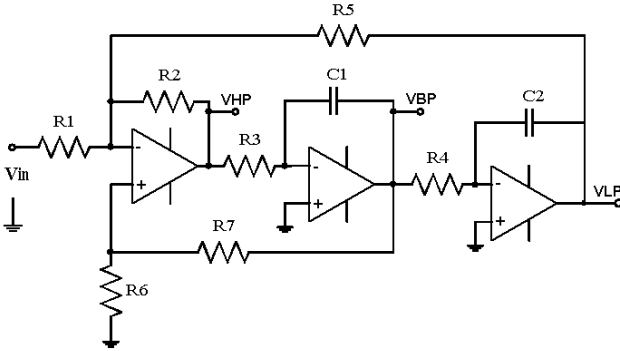


Figure 2: Continuous Time State-Variable Active Filter

$$\frac{V_{LP}}{V_{in}} = \frac{K'/(R3R4C1C2)}{s^2 + \frac{1}{R3C1} \frac{1}{Q} s + \frac{1}{R3R4C1C2}} \quad (8)$$

$$\frac{V_{BP}}{V_{in}} = \frac{K'/(R3C1)s}{s^2 + \frac{1}{R3C1} \frac{1}{Q} s + \frac{1}{R3R4C1C2}} \quad (9)$$

$$\frac{V_{HP}}{V_{in}} = \frac{K's^2}{s^2 + \frac{1}{R3C1} \frac{1}{Q} s + \frac{1}{R3R4C1C2}} \quad (10)$$

where

$$K' = \frac{2R6R7}{R1R7 + R1R6 + R6R7} \quad (11)$$

$$Q = \frac{2R1R6}{R1R7 + R1R6 + R6R7} \quad (12)$$

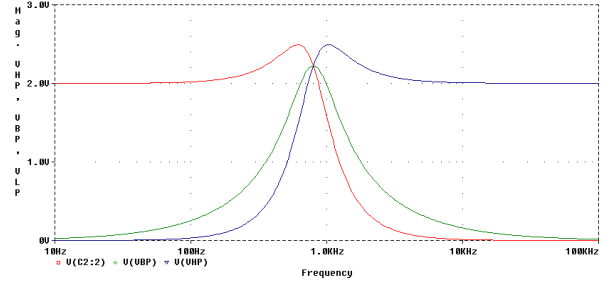


Figure 3: Low-Pass, Band-Pass & High-Pass Frequency Responses

The circuit of Figure 2 was initially tested by applying a 63-bit long PRBS test signal, with a bit interval of 200 μ sec, and capturing the transient responses at the filter output nodes VLP, VBP and VHP. The simulation results, using SPICE, showing the input PRBS test signal (V_{in}) and the resulting fault-free responses of the filter are illustrated in Figure 4. Monte-Carlo analysis, assuming a tolerance of 5% for the resistive and capacitive component values, was carried out in order to establish the bounds of the tolerance envelope around each one of the fault-free circuit outputs. Fault-free auto-correlation and cross-correlation signatures, with the appropriate tolerance bounds, were computed for each one of the output nodes.

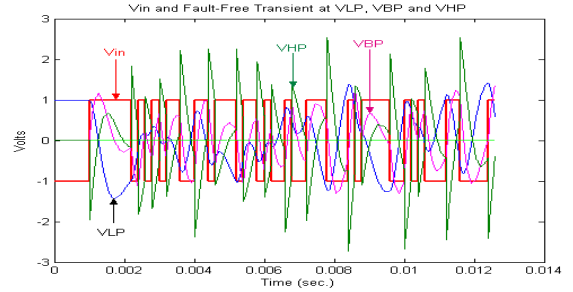


Figure 4: V_{in} and Fault-Free Transient Responses

A set of 45 single fault conditions, were introduced to the filter circuit of Figure 2. The faults were a mixture of catastrophic and soft fault conditions. The catastrophic faults were based on the fault models shown in Figure 1. The soft faults were variations of $\pm 25\%$ and $\pm 50\%$ in the nominal values of the resistive and capacitive components, and the widths and lengths of some of the internal transistors of the operational amplifier circuits.

Both the auto and cross correlation functions corresponding to the captured transient response, at the VLP, VBP and VHP nodes, of each injected fault were calculated. The fault signatures data was subsequently analyzed extensively to determine the fault coverage, number of detection instances and relative detection confidence levels.

Analysis of the simulation data indicated that fault coverage of nearly 98% was achieved by both the auto and cross correlation functions irrespective of the output node being monitored. The fault coverage calculations were based on

determining the number of instances at which a fault was detected as shown in Figure 5 for the low-pass node case.

To determine the confidence in the detection Equ.(6) was applied and the result for the autocorrelation at the low-pass node are shown in Figure 6. The results indicate that the detection confidence in some of the fault is relatively low, which means that the probability of detecting those faults in a practical setup may be low.

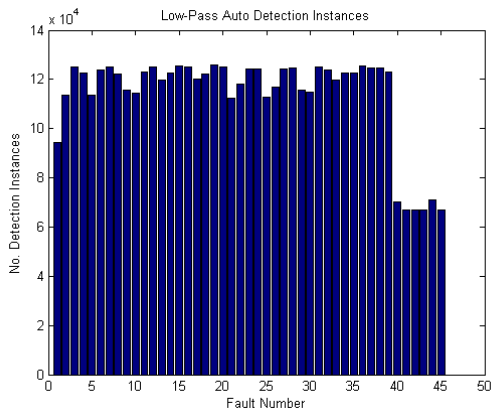


Figure 5: Low-Pass Auto-Correlation Detection Instances

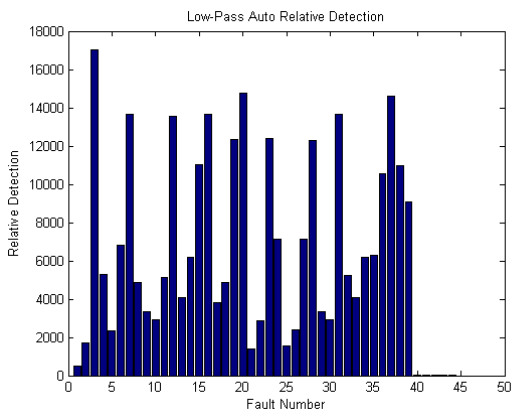


Figure 6: Low-Pass Auto-Correlation Relative Detection

The results of the number of detection instances and the relative detection confidence for the low-pass, band-pass and high-pass data based on analyzing the autocorrelation functions are combined in Figure 7. It shows that monitoring the filter circuit response at the low-pass node achieves relatively higher detection confidence than that of the other filter sections. The cross-correlation combined results are shown in Figure 8.

The results at VLP, VBP and VHP are close, however closer examination of the data indicates that VLP detects more faults with higher confidence than the others. Comparison of Figure 7 and Figure 8 indicates that detections based on autocorrelation have relatively higher confidence than those based on cross-correlation.

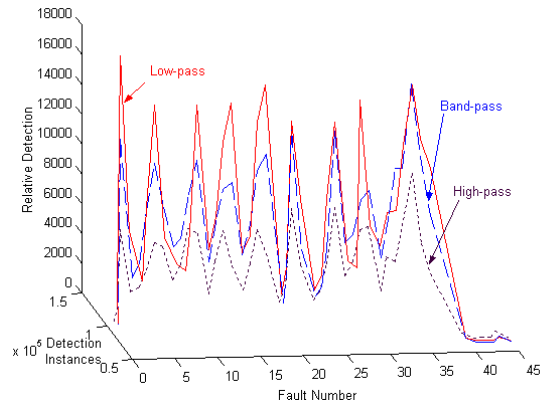


Figure 7: Combined Auto-correlation Results

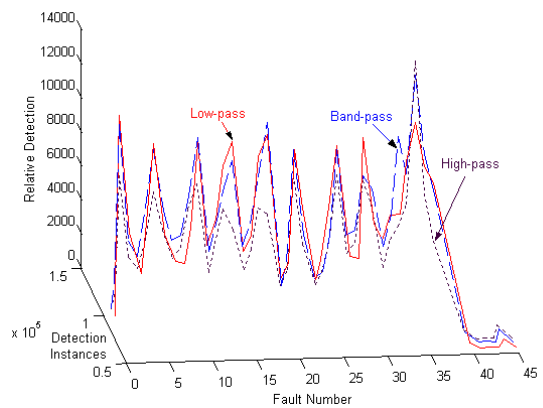


Figure 8: Combined Cross-correlation Results

6. EFFECT OF TEST SIGNAL LENGTH

The effect of the PRBS length on the percentage of detection instances and the relative detection confidence level was investigated by injecting a 31-bit sequence and then a 127-bit sequence, and simulating the circuit under fault-free and faulty conditions.

Analysis of the results from the 31-bit sequence, indicate a reduction in the fault coverage by 1%-3%, and an associated reduction in the confidence level of some of the faults. Similar analysis of the 127-bit simulations indicated an overall improvement in both the percentage of detection and the relative detection confidence levels. However, the improvement in the detection of faults with low confidence levels when the longer bit sequences were used was only marginal.

7. DESIGN FOR TESTABILITY STRUCTURE

The simulation results presented earlier were used to demonstrate the viability of the PRBS based testing method and its ability to detect a large set of faults in analog modules in a mixed-signal circuit. However, in a practical production testing, set-up it is not expected that the above detailed analysis and comparisons would need to be performed. Instead, it is envisaged that the method can be incorporated with the actual mixed-signal circuit DFT structure as shown in Figure 9.

A number of design-for-testability strategies were proposed in the literature [10-12] to enable analog circuits

testing. However, many of those strategies tended to be for specific analog modules. The envisaged DFT in Figure 9 is a general system level realization that implements an approximate form of Equ.(3). This approximation would result in an acceptable area overhead for the test structure. The estimated impulse function obtained using this approximation may deviate from the ideal one, however the result can still be used as a signature defining the state of the circuit.

In Figure 9 a delayed replica of the PRBS stimuli is multiplied with the response of the analog CUT, the multiplier output is then integrated and fed to a fault-detection circuitry. The fault detector consists of a window comparator whose bounds are determined by the tolerance imposed on the fault-free response of the analog CUT. The output of the window comparator circuit is a two level signal that can be observed directly, or integrated into the digital circuitry DFT structure.

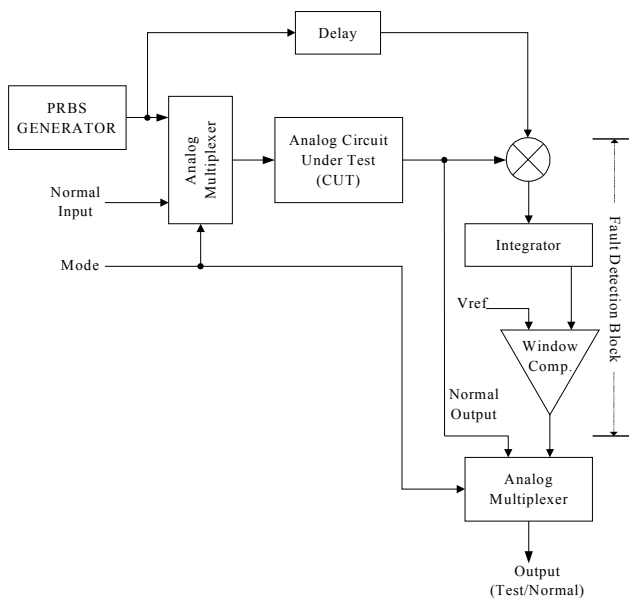


Figure 9: Analog Design for Testability Structure

The system shown in Figure 9 was simulated with the CUT being the transfer function of the filter circuit in Figure 2. The results indicate a good degree of fault coverage. However, comparison with the results given in section 5, are not possible at this stage due to the different levels of simulation used.

The circuitry of the individual blocks of the system in Figure 9 are under development and a rigorous assessment will be conducted on CUTs with varied degrees of complexity once the complete design is finished.

8. SUMMARY

The difficulties associated with testing analog circuits being in an all analog or in a mixed-signal environment have been outlined. A test method based on using a PRBS as the stimuli and the subsequent analysis of the captured transient response of the CUT has been discussed in detail.

The test method and data analysis have been applied to a continuous-time filter circuit with low-pass, band-pass and high-pass sections. The results indicate that the proposed testing technique achieves high fault coverage, and the auto-correlation function gives relatively higher detection confidence than the cross-correlation one. The initial analysis of the filter results, seem to indicate that the low-pass node gives better detection than the other. This may be attributed to the

concentration of the signal components in the sensitive part of the response. However, this point will need to be investigated in greater depth in further studies.

The influence of the PRBS length on both the detection of faults and the confidence in the detection process was explored briefly in this study. However, optimizing all the PRBS parameters based on through analysis of the CUT circuit transfer function will be the subject of future work. Also, minimization of the test data and subsequent processing will need to be addressed.

The viability of the proposed test method was studied further by applying it in conjunction with the suggested analog DFT structure. The initial results were encouraging, and more work is being done on that.

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