Offset Correction In Voltage Mode Delay Lines

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Abstract: - A novel continuous time strategy, to compensate offset, gain errors and distortion in voltage mode delay lines is presented. Compensation arrangements, based on MIFGT transistors, allow using transistors with minimum L, extending the bandwidth to intermediate frequency, without increasing the power consumption. A third-order delay line was designed in a 0.5-μm CMOS technology. An offset compensation of 84.7% was obtained.

Key-Words: - Adaptive filters, CMOS, delay line, distortion, floating gates, offset.

1 Introduction

Adaptive Filters (AF) are systems whose structure can be self-modified to improve their behavior according to the environment [1]. Systems identification, prediction and echo cancellation are some of their applications. Analog Adaptive Filter structures (AAF) are able to handle higher frequencies and lower convergence rates than their digital counterparts, besides a reduction in power consumption and area requirements. However, their precision is limited by offset contributions [2, 3, 4]. Traversal filters (TF) are the most commonly used structures to implement AAF [3]. A block diagram of a TF is shown in Fig.1. In TFs, only the transfer-function zeros are adapted and all poles are fixed [3]. Therefore, they are unconditionally stable, and the convergence to the minimum square error $E[e^2(t)]$ (where $E[\bullet]$ denotes expectation) is guaranteed by using a Least Mean Square algorithm (LMS) [3]. The expressions that govern the scheme are:

$$y(t) = \sum_{k=0}^{M-1} \omega_k u(t-k), \tag{1}$$

$$\mathbf{W}(t) = \rho \int_0^t e(t)\mathbf{U}(t), \tag{2}$$

where ω_k are the adaptive weights, ρ is a constant determining the rate of adaptation, **W** is the weights vector, **U** is the vector conformed by the input *u(t)* and their late versions *u(t-kT)* (gradient signals), and *e(t)=d(t)-y(t)* is the estimate error between the output *y(t)* and a given reference *d(t)*.

When parameter updating is performed using analogue circuitry, DC offsets will appear at the signals **U,** *e(t)* and the integrator input. Those offsets contributions degrade the filter performance, adding an excess Mean Square Error (MSE) [4]. Several techniques have been proposed to compensate those offsets. Discrete time methods, like auto-zeroing and input-output offset storage, are susceptible to offset from clock-feedthrough and 1/f noise [5]. Trimming circuits techniques [6] require treatments post-fabrication, high voltages-currents, and only prevent the mismatch offset. Algorithmic approaches [2] are limited due to their high complexity. By adding to the AAF an offset-cancellation tap [3], only the offset in *e(t)* is eliminated.

In the present work, a continuous-time technique to compensate offset contributions, gain errors, distortion and common mode voltage, in a third-order fully-differential voltage-mode delay line, for intermediate frequency operation, is proposed. That allows the use of minimum L in transistors, extending the bandwidth and reducing significantly the power consumption. The compensation arrangements are based in multiple input floating gate transistors (MIFGT), and allow offset reduction of around of 70%. The structure of the present work is as follows: Section 2 introduces the voltage follower core, which is the basic block of the delay line. Section 3 presents the proposed compensation strategy. Section 4 presents results, using HSPICE, of two third-order delay lines, uncompensated and compensated, respectively. Conclusions are enunciated in Section 5.

2 Non-Compensated Voltage Follower

The delay line is developed by connecting fully-differential feedforward voltage followers in cascade. The highly linear voltage follower of Fig.2 [7] has a extended bandwidth and a short settling time with no overshoot transient response. It consists on a differential pair M_{n2}-M_{n3} loaded with transistors M_{n5}-M_{n6}, which are coupled through folded-cascode transistors M_{p10}-M_{p11}. M_{n11} operates in triode, allows a linear adjusting of the common mode voltage. If M_{n2}, M_{n3}, M_{n5} and M_{n6} are identical, for low frequency and small signal analysis:

$$V_{inp} - V_{inn} = -\left(V_{outp} - V_{outn}\right), \qquad (3)$$

and for high frequencies and assuming that the follower's load is a similar stage:

$$BW \propto \frac{1}{2\pi}\frac{g_{m5}}{C_{outp}} = \frac{3K_n\left(V_{GS5} - V_{T5}\right)}{8\pi C_{ox} L_5^{\,2}}. \qquad (4)$$

A wider bandwidth if obtained if $V_{eff}=(V_{GS}-V_{TH})$ is increased and L decreased. However, under those conditions, the offset in a the differential pair increases, agreement with [5, 8]:

$$3\sigma_{V_G} = 3\sqrt{\frac{K_n}{g_m L^2}A_{VT}\left(V_{GS} - V_{TH}\right)} = 3\frac{A_{VT}}{\sqrt{WL}}. \qquad (5)$$

3 Compensated voltage follower

The gain and distortion compensation strategy proposed in [9] is conceptually modified in this section in order to allow offset compensation too. If (3) is satisfied in each instant *t*, the voltage follower does not present offset, gain errors and distortion. Reordering that expression:

$$V_{outp} + V_{inp} = V_{outn} + V_{inn}, \quad \text{(only DC)} \qquad (6)$$

where signal components have been eliminated. The proposed compensation consists on identifying low-frequency local control loops that allow to satisfy (6); this type of parametric feedback paths do not degrade significantly the bandwidth [9]. From Fig.2, three possible compensation nodes are identified: V_{b2}, V_{cas1} and V_{cas2}. Feedback control circuits are realized using the four input MIFGT OPAMP of Fig.3 [9]. If negative feedback, large OPAMP gain, and identical MIFGT capacitors are used, then:

$$\left(V_{1a} - V_{1b}\right) + \left(V_{2a} - V_{2b}\right) = 0. \qquad (7)$$

where the MIFGT's capacitors can be chosen small because negative feedback reduces the parasitic capacitances effect [9]. The offset caused by the pre-stored charge on the MIFGTs can be alleviated by a UV light process [10]. Equation (6) is easily realized, according to (7), using two MIFGT OPAMPs and the voltage selection of V_{1a},V_{2a}, V_{1b},V_{2b}, shown in Fig.4. If $V_{1a}=V_{2a}=V_{ref,}$ $V_{1b}=V_{outp}$ and $V_{2b}=V_{outn}$, then:

$$V_{CM} = 0.5V_{outp} + V_{outn} = V_{ref}, \qquad (8)$$

where V_{CM} is the common-mode voltage and V_{ref} is the reference voltage. Whit that voltage selection the Common-Mode Feedback (CMFB) is performed (Fig.4). To higher OPAMP's gain, better will be the offset, gain and distortion compensations. Unfortunately, when gain increases, the frequency response trend to present overshooting, which causes a not constant group delay.

4 Results

Two third-order delay lines, using voltage followers of figures 2 and 4 respectively, have been designed. Details of those designs, for a 0.5-μm AMI Semiconductor (AMIS) technology, are shown in table 1. The corresponding offsets can be approximated as the offset in (M_{n2}-M_{n3}, M_{n5}-M_{n6}) and M_{f1}-M_{f2}, respectively. The last one is smaller, because M_{f1} and M_{f2} can be formed with no-minimum L, since they work at low frequencies. Fig.5 shows the theoretical values for this offsets. A compensation of 75.4% is predicted. Simulation are performed with HSPICE and level 49 MOSIS parameters. The uncompensated voltage follower presents 0.6 V_{pp} input and output signal swing, total harmonic distortion of 1.8%, 5 ns settling time and 6.9% gain error. The compensated voltage follower presents, with $C_{fg}=C_0=40$ fF, the same performance parameters, but with a total harmonic distortion of 1.2%, and a gain error of 2.6%. Distortion reduction is a consequence of offset compensation, because even harmonics produced for mismatch are reduced. A comparison of the two third order delay lines frequency responses shows that the compensated

delay line presents distortion reduction of 33% and gain correction of 62%, but with a bandwidth reduction of 46.57%. The frequency response of the compensated delay line is shown in Fig.6. It can be observed that an overshoot in the frequency response is produced by the compensation net. However, it has a flat group-delay in the range from 20 MHz to 140 MHz. Fig.7 shows a comparison of the MonteCarlo results between the uncompensated, and two compensated delay lines with $C_{fg}=C_0=40$ fF and $C_{fg}=200$ fF, respectively. An overall offset compensation of 67% can be observed, which can be improved by using larger capacitors in the MIFGT.

5 Conclusion

A novel strategy to compensate, in continuous time, offset, gain errors, distortion and CMFB in delay lines has been presented. Compensation arrangements allow to use transistors with minimum L, extending the bandwidth without increasing the power consumption. The offset compensation strategy is highly efficient, because is better to tolerate the offset in the compensation arrangement, which operates at low frequencies, that offset in the delay line, which operates at high frequencies. A offset compensation of around of 67%, in a three order delay line has been observed.

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TABLE I. DELAY LINE DESIGN DETAILS

Parameter	Value
L_{p2}, L_{p3}, L_{p10}, L_{p11}	0.6 μm
W_{p2}, W_{p3}, W_{p10}, W_{p11}	24.3 μm
L_{n2}, L_{n3}, L_{n5}, L_{n6}	0.6 μm
W_{n2}, W_{n3}, W_{n5}, W_{n6}	9 μm
L_{p4}, L_{p5}, W_{p4}, W_{p5}	(9, 9, 12, 12) μm,
L_{f1}, L_{f2}, W_{f1}, W_{f2}	(1.2, 1.2, 10.5, 10.5) μm,
L_{n4}, L_{n7}, L_{n8}, L_{n11}	(0.9, 0.9, 0.9, 0.6) μm
W_{n4}, W_{n7}, W_{n8}, W_{n11}	(40.2,40.2, 16.2, 2.7) μm
V_{DD}, I_{bias}, I_{bias2}	3 V, 100 uA, 40 μA
$C_{fg} = C_0$ (MIFGT)	40 fF.
Power consumption	4.6 mW

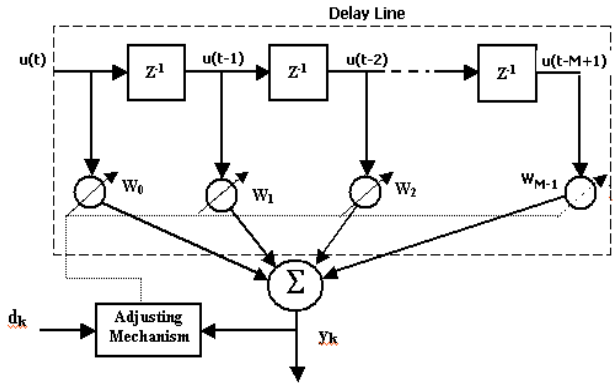

Fig. 1. Block diagram of a transversal filter.

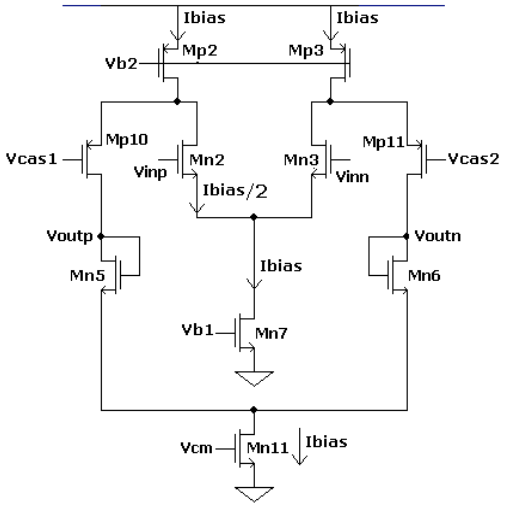

Fig. 2. Uncompensated fully-differential voltage follower.

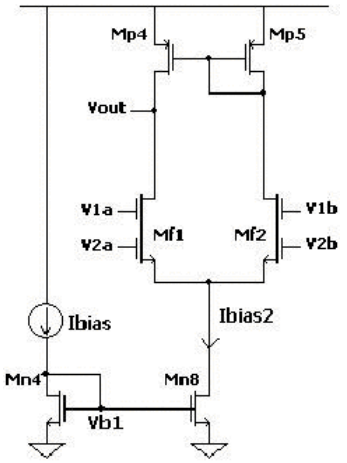

Fig. 3. Four input MIFGT OPAMP.

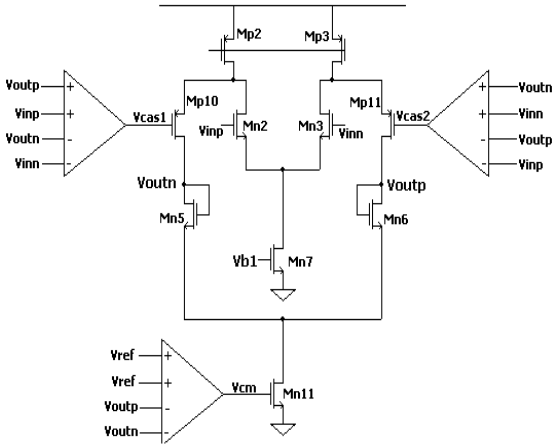

Fig. 4. Compensated fully-differential voltage follower.

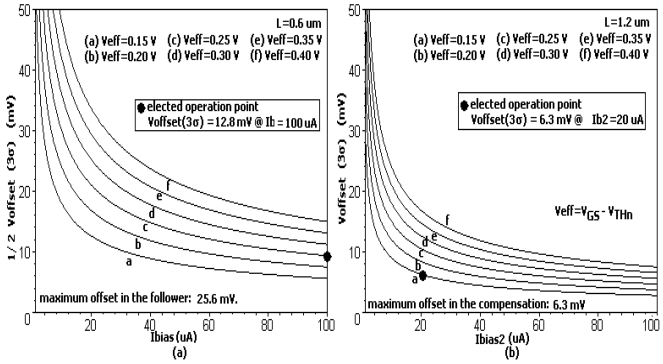

Fig. 5. (a) Theoretical uncompensated voltage follower's offset. (b) Theoretical compensated voltage follower's offset.

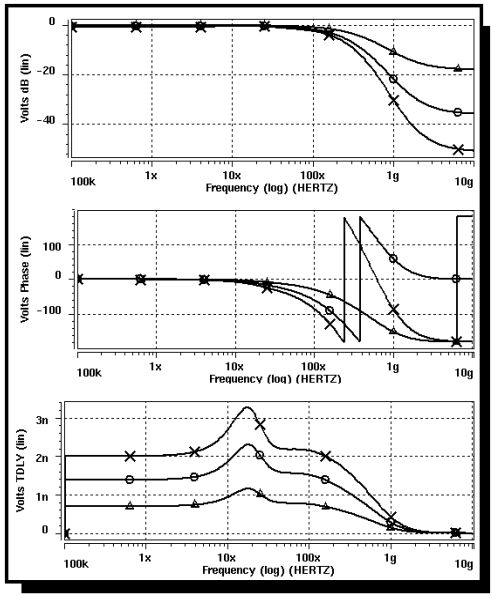

Fig. 6. Frequency response of the comp. delay line.

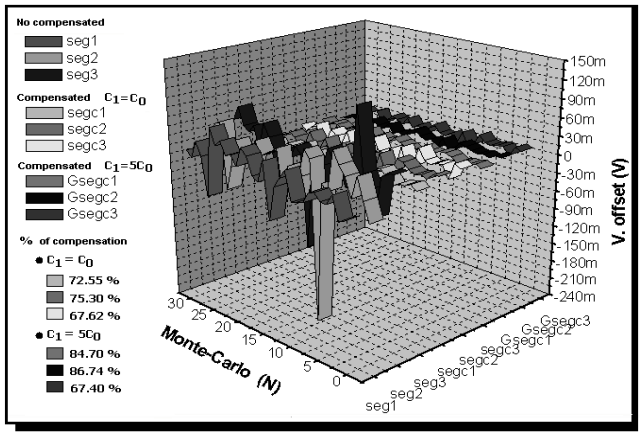

Fig. 7. MonteCarlo analysis (Offset compensation)