Efficient Datapath Design Using Novel 6*6 Conservative Reversible Gates

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Abstract - Is it possible to speak of a deterministic conversion scheme between energy, which is a physical quantity, and informational work, which is an abstract quantity? Raising this intriguing question, which laid foundations to the exciting area of reversible computation, Landauer (1961) showed that the fundamental limits of being 'energy aware' are deeply rooted in the physics of energy consumption, specifically in thermodynamics. In this paper, we present a novel 6:6 (input: output) reversible logic element and illustrate design of efficient reversible datapath using the proposed structure. Inherently being a reversible half adder itself, the gate also gives propagate and generate signals at its other output pins hence facilitating straightforward realizations of adder circuits in a reversible manner. All datapath synthesis methods proposed are technology independent (since reversible gates are widely known to be compatible with revolutionary computing paradigms like optical and quantum computing) and require minimum input constants.

Key-Words: - Reversible, Power, Datapath, Conservative

1 Introduction

Concerns of power (or Energy) dissipation have become increasingly significant given the ever-increasing need to reduce system overhead cost and prolong the operational life of VLSI systems. In such circumstances, a fact which is hard to miss is that a computing element is intrinsically a thermodynamic engine which does work and dissipates heat. Switches are probably the building blocks of most Boolean functions and the energy behavior of switching has its roots in thermodynamics whose history dates back to the seminal works of Carnot, Boltzman, Gibbs and Plank. Launder (1961) raised the question regarding the relationship between computation and the concomitant power consumption by a physical device that implements the computation.

Elementary thermodynamics tells us that irreversible physical processes involve inevitable dissipation of usable energy into heat. Often the transition function of a digital computer does not have a single valued inverse i.e. during the computing process information is lost leaving the physical device in a state whose immediate predecessor is ambiguous. Hence most of the computations are logically irreversible in the sense that the output cannot uniquely define the input. So a physical device that imitates a logically irreversible operation has to incorporate irreversibility at some point or another thus pointing to an inevitable thermodynamic cost of destruction of information [1]. Bennet [2] showed that for power not to be dissipated from an arbitrary circuit it is necessary that the circuit be built using reversible gates. He used the pebbling argument to show that it is possible to use reversible primitives to perform an irreversible operation with a modest space time trade off. Others have found that it is possible to convert all logically irreversible operations into reversible operations by specially designed reversible logic gates [3, 4, 7, 11]. Of these, the 2*2 Feynman gate (also called as controlled not or Quantum Exor) and two 3*3 universal reversible gates viz the Fredkin gate [3] and the Toffoli gate [4] have been much studied. Recently, Adder implementations based on Fredkin gate [Bruce] and optical logic gates performing classical logic functions have been proposed [4]. Reversible and conservative logic gates are naturally compatible with optical and quantum computing. Few researchers are exploring the potential of energy savings through probabilistic algorithms at a fundamental physical level based on thermodynamic models of idealized monatomic gases.

This paper continues the tradition with a two new 6:6 computationally universal reversible gates of the form V^6: (A, A, A', B, B, B') ==>> (A, A.B, A', A+B, A⊕B, A⊗B) and Q^6: (A, A, A', B, B, B') ==>> (A, A.B, A'+AB, A+B, A⊕B, (A+B)') ,where A' indicates *Not A*. The former (V) is a two through gate while latter (Q) is a one through gate, both gates innately being reversible half adders. The paper is outlined as follows. Section 2 provides definitions and background on reversible and conservative logic concepts. This section also characterizes the

functionality of the proposed logic gates. Section 3 briefly describes the design of Ripple carry and Carry Look Ahead adders using the proposed reversible gates. Some preliminary conclusions and Ideas for future circuit refinements are explained in the concluding section.

2. New Family of 6:6 Reversible Gates

2.1. Preliminaries

A gate is reversible if it has a one to one mapping between its input vectors and output vectors. It is both *injective* (one to one) and *surjective* (onto). A ramification of this definition is that the gate must have same number of inputs and outputs. A gate with k inputs and k outputs is called a k*k gate where k is called '*Logic width*' of the gate. Intuitively a reversible system is that which is retrodictable or backward deterministic. However, the concept of reversibility does not imply invariance under time reversal. A gate is conservative if the Hamming weight (number of logical ones) of its input equals the hamming weight of its output. A consequence of its consevativity and reversibility is that the gate is zero-preserving and one-preserving. Finally, a circuit is balanced if half of its minterms are ones.

2.2. Fredkin Gate

Fredkin and Toffoli showed that 3 inputs and 3 outputs is necessary and sufficient to build any arbitrary digital logic having finite number of input arguments. Figure 1 shows the three input Fredkin gate (FG).

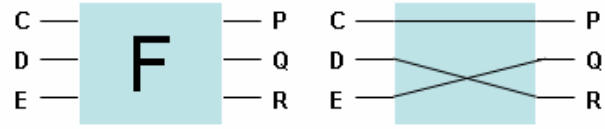


Figure 1. 3*3 Fredkin Gate

The functionality can be expressed as (P, Q, R = C, D, E if C=0) and (P, Q, R = C, E, D if C=1). The gate performs a controlled swap of the input variables D and E based on the control input C. FG is one through as one input (c) is directly transmitted to the output. Fredkin gate is considered a primitive logical element in magnetic bubble circuits [10]. As shown in figure 2 a two input AND gate can be realized by grounding input E and a two input OR gate can be realized by connecting input E to V_{dd} and swapping the inputs when C=0 rather than C=1.

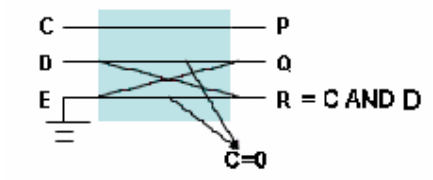


Figure 2. AND Gate

We will use the FG to generate duplication and inverse of the input signal. This can be obtained by tying the FG terminals to the supply and ground lines as shown in figure 3.Hence, for an input signal A, we get A, A and

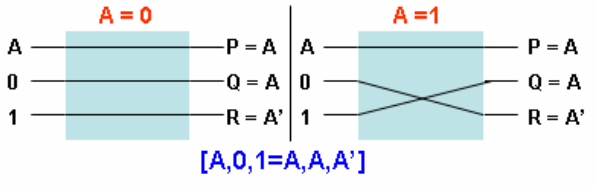


Figure 3. FG used for Duplication and Inversion

A' at the output. The functionality can be written as (A, 0, 1 =A, A, A').From the functionality it is also evident that FG is its own inverse (Classical Inverter is also Self Invertible) and input arguments can be uniquely determined form the outputs.

2.3 6*6 Conservative Reversible Logic Module

Two 6*6 reversible gates are proposed in Figure 4 and Figure 6 respectively. Both gates perform conditional crossover of five input data signals to the output pins based on the value of control signal at input 'X'. For simplicity, we will address the former gate as 'V gate' and latter as 'Q gate' respectively. Both gates are computationally universal i.e. they generate AND, OR and NOT functions which form a computationally universal set of gates. The transmission of input signals based on value of the control input X (X=0 and X=1) is shown in Fig 4(b) and 4(c). When X=0 the input signals are directly passed to the output pins and when X=1 signals at inputs Y, A, B, C are sent to outputs IV, II, VI, V respectively. The interesting consequence of performing the suggested conditional swap is that if (X,Y,Z,A,B,C= A,A,A',B,B,B') then V 6*6 Yields (A, A ***AND*** B, A',A ***OR*** B, A ***XOR*** B, A X***NOR*** B) at output pins (**I,II,III,IV,V,VI**) .

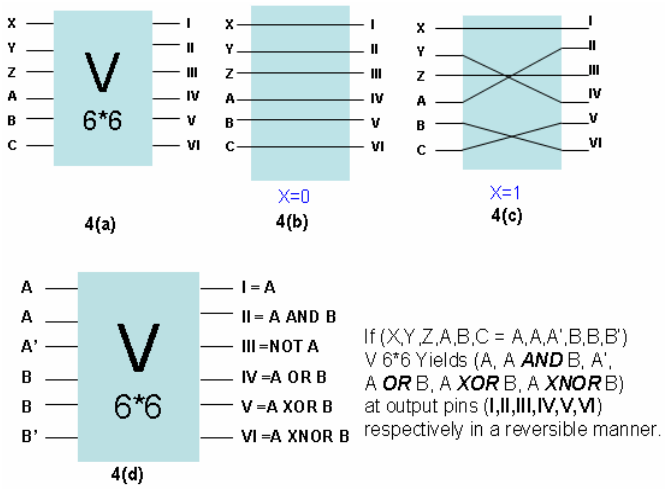


Fig.4. *V 6*6 Gate*. 4(b) and 4(c) show conditional swap of input signals to the output based on Control input X to realize Boolean AND,OR,NOT ,EXOR and EXNOR functions *Simultaneously and Reversibly.*

The input signals of the form (A, A, A') can be derived reversibly from input A using the configuration shown in figure 3.It should however be noted that the configuration of Fredkin Gate shown in Fig 3 is essential to produce duplication and inversion of inputs A and B because if we want our circuits to be reversible, Fan out >1 must be avoided. *Any branching i.e. Fan out >1 when looked in reverse appears as combination of signals hence introducing irreversibility*. In Figure 5 we have expressed the output variables as explicit functions of input variables.

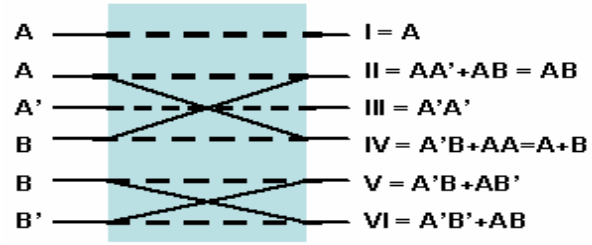


Figure 5 Behavior of V 6*6 gate.

The overall functional relationship between input and output is invertible .It can also be easily verified that the *Hamming weight of the gate is preserved for all input /output combinations indicating conservatively.* A n*n reversible gate can have 2^n possible input and output values and selectively switching them to realize useful functions (Which are classically irreversible) ultimately boils down to an input -output constraint i.e. 2^n output numbers form a permutation of 2^n input numbers. So, for a logic width of n, exactly $2^n!$ different reversible gates can exist [9]. The Q gate is obtained form the same 6*6 combination by channelizing the inputs to the outputs as shown in Fig.6. When X=0 the input signals are directly passed to the output pins and when X=1 signals at inputs Y, Z, A, B, C are sent to outputs IV,V, II, VI, III respectively. By doing so we also get a universal gate NOR at the output pin VI in addition to other Boolean functions at other output pins.

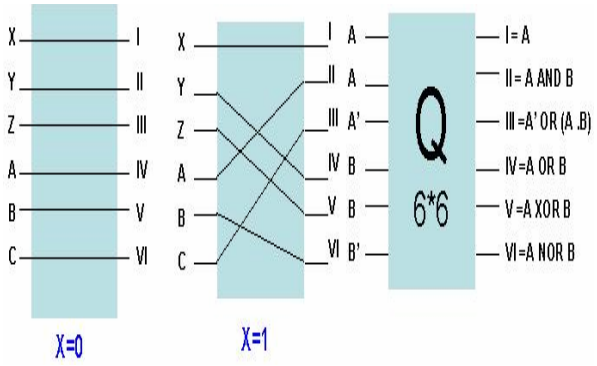


Figure 6.Conditional Swap to realize Boolean AND, OR, XOR, NOR functions *simultaneously and reversibly.*

functionality of this gate can be expressed as Q^6 (**I, II, III, IV,V,VI** = X,Y,Z,A,B,C if X=0) and Q^6 (**I, II, III, IV,V,VI** = X,A,C,Y,Z,B if X=1). It can also be seen that both the gates realize half adder operation with Sum at output 'V' and Carry at output 'II' respectively. To verify the functionality of the gates, they were implemented in CMOS .Figure 7 shows the V6*6 implementation in CMOS.

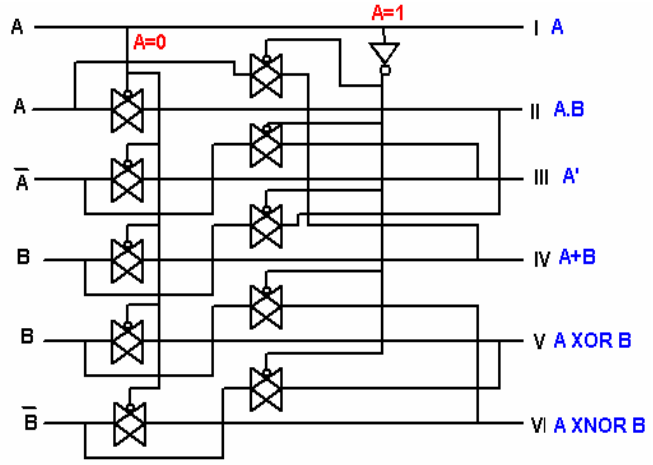


*Figure 7.CMOS implementation of V6*6 gate.*

At this point, we however emphasize that reversible logic implementation in CMOS is not optimal and we used the implementation to only validate our architecture. The proposed architectures are innately well suited for Quantum computing since each instruction performed upon quantum bits (*QBIT*) must be logically reversible. Moreover, the field of optical computing is progressing rapidly and shows many dramatic opportunities for overcoming the limitations of their current electronic counterparts. The full potential of optical logic cannot be realized without gates compatible with optical systems and Reversible Conservative gates are natural for optics. Hence, the reversible structures presented in this section promise effective simultaneous reversible synthesis of classically irreversible functions in optical technologies also.

3. Adder Realizations

In an era where efficient information processing is becoming exceedingly critical, there has always been a continuing need to improve the performance, area and functionality of an assortment of arithmetic units, central among them being the adder block. In this section we explore possibilities of efficient adder blocks in Reversible Logic based on structures presented in Section 2.*How ever it is worth noting that the synthesis of reversible logic blocks are different from the synthesis of classical digital logic. Even though some systematic reversible synthesis algorithms have been proposed in the past [7], this area is still juvenile.* Some of the constraints while syntheses of Reversible architectures are as follows: a) Branching is disallowed *since* it amounts to amalgamation in looking in reverse b) A

reversible architecture should be a *directed acyclic graph* [6] which implies no looping of gates c) All child functions in the design must be reversible d) It is also advisable to use minimum input constants and generate minimum garbage outputs even though garbage signals are an inevitable consequence of reversible computations.

The structure in fig 4 reversibly realizes XOR, XNOR, Propagate and Generate (V VI IV II) functions simultaneously, all of them being vital in implementing full adder. The block diagram of the proposed full adder implementation is shown in figure 8.In addition to the V block we have used one Fredkin gate (F) and one custom made 4*4 reversible structure whose internal functionality is elucidated in Figure 9. The 4*4 block swaps inputs as shown in Fig 9 when C=1and channelizes the input signals directly to the output when C=0.

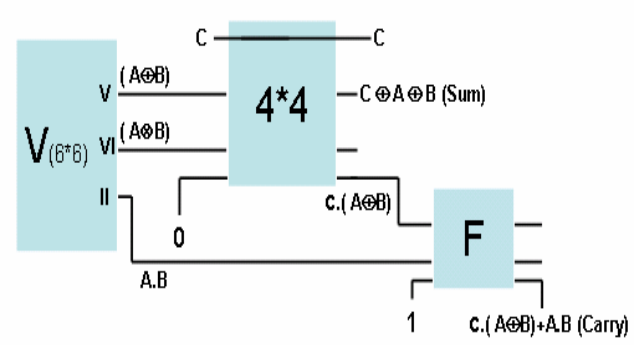


Figure 8. Full Adder using V6*6 module

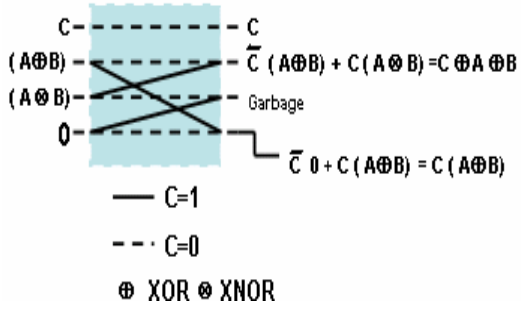


Figure 9.Internal architecture of 4*4 Block

It can be easily verified that the design in Figure 8 strictly follows reversible computing paradigms mentioned earlier and yet realizes an optimal full adder using novel custom made conservative logic structures. Ripple carry adder which is the simplest and most straightforward adder architecture uses only one major block i.e. the full adder. But when the word size is large, it is important to get rid of the rippling effect of the carry signal and most adders strive to compute carries more quickly. Theoretically carry look ahead adders offer the fastest performance. Both the architectures presented in section II yield Propagate and Generate signals and hence facilitate simple reversible implementation of CLA addition. In a fully expanded form the carry at k^{th} position can be written as:

$$C_{o,k} = G_k + P_k (G_{k-1} + P_{k-1} (..... + P_1 (G_0 + P_0 C_{i,0}) \quad (1)$$

Eqn. 1 eventually evolves a SOP of the form:

$$C_{o,k} = f (G_k , P_k, G_{k-1} , P_{k-1}..... P_1, G_0, P_0, C_{i,0}) \quad (2)$$

This multi input SOP can be effectively synthesized in a reversible manner as shown in figure 10 using generalized k*k Feynman gate proposed by Perkowski.For reasons of space we refer the reader to [7] for details of reversible multi input multi output synthesis.

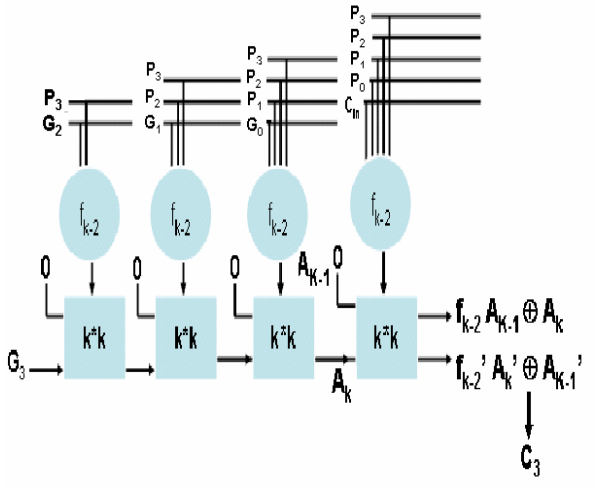
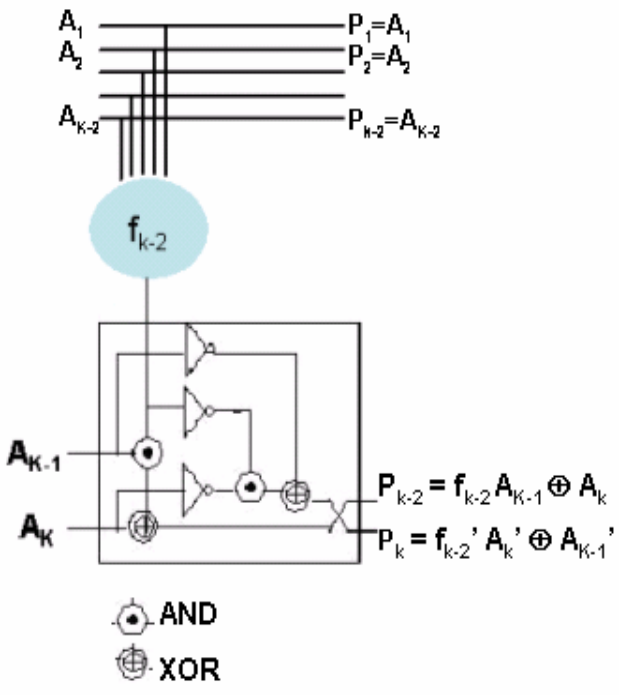


Figure 10. C_{out} block of 4 bit CLA Adder

Figure 11. Internal structure of k*k family [7]



The reversible gate in fig 11 is a K-2 through gate.If A_{k-1} =0, then, $P_k = f_{k-2} + A_k$ where f_{k-2} is the product of inputs A_1 to A_{k-2}.

4. Discussion

Computing engines of today are thoroughly wasteful as they dump billions of bits, millions of times, every second which in turn gets transformed into entropy, associated energy of which becomes heat whose removal is the most critical design criteria for today's processors. Launder argued that a computational system built using traditional irreversible gates inevitably dissipates energy regardless of the technology used to realize them. Energy efficiency is becoming a critical factor in the design of computing systems since it directly affects the cost of computation by increasing the system overhead required to get rid of the heat in addition to the inconvenience of weight, short battery life etc. Moreover, to keep the remarkable trend of Moore's law functioning in future, it is necessary to learn to compute in harmony with the fundamental laws of physics and design reversible processors in which signals just move around during the course of computation none of them either being destroyed or created. The focus of the work described in this paper was centered on finding efficient routines which rearrange tokens of input arguments into the output and *simultaneously yield much useful classically irreversible digital logic in a reversible and conservative manner.* Two such modules were proposed in this paper. We also demonstrate that efficient reversible datapath architectures can be realized by just merely canalizing a set of input signals selectively to the desired output pins without increasing entropy of the computing environment. The CMOS implementations of the circuits presented were simulated on *SWITCHER CAD*, a schematic capture tool running on a Pentium IV desktop. CMOS based implementations is not an optimal way to realize reversible gates, nevertheless, we used it to only validate our circuits. However, all data path synthesis methods proposed are technology independent since reversible gates are widely known to be compatible with revolutionary computing paradigms like optical and quantum computing. Hence with device sizes approaching atomic limits, Ballistic circuits which conserve information offer a shining prospect towards increasing energy efficiency.

The possibility of linking computation (information processing) with energy expenditure also becomes extremely relevant in the light of certain neuroscience data. In the brain there is a tight coupling between 4 quantities – 1) neural activity, 2) local cerebral blood flow, 3) local glucose metabolism, and 4) temperature changes [12]. Studies also show that external sensory stimuli evoke transient, local temperature changes in the brain [13]. So, Is it possible to define a minimal amount of work done to carry out a computation? Does fundamental law linking information processing and energy expenditure in computing devices exist? If it does then, can we achieve the lower bound of energy as proposed by Launder, in actual implementation? Or can we at least use the relation between computational reliability and energy to direct the design of circuits that implement the desired computation? Further research in this direction is hoped to answer these queries.

5. References

1) Rolf Landauer, "Irreversibility and heat generation in the computing process," *IBM Journal of Research and Development*, **5**:183-191, 1961. http://www.research.ibm.com/-journal/rd/441/landauerii.pdf.
2) Charles H. Bennett, "Logical reversibility of computation," *IBM J. of Res. & Dev.*, **17**(6):525-532, 1973. http://www.aei-veos.com/~bradbury/Authors/Computing/Bennett-CH/LRoC.html.
3) Fredkin, E. and Toffoli, T. (1980), "Reversible Computing," MIT Report MIT/LCS/TM-151.
4) Edward F. Fredkin and Tommaso Toffoli, "Conservative Logic," *Int'l. J. Of Theor. Phys.*, **21**(3&4):219-253, 1982.
5) Gershenfeld, N. (1996), "Signal Entropy and the thermodynamics of computation," IBM Systems Journal, vol. 35, Nos.3&4.
6) J.W. Bruce, M.A. Thornton, L. Shivakumaraiah, P.S. Kokate, and X. Li," Efficient Adder Circuits Based on a Conservative Reversible Logic Gate", IEEE Computer Society Annual Symposium on VLSI, Pittsburgh, PA April 25-26, 2002, pp 83-88.
7) Mozammel Huq Azad Khan and Marek Perkowski, ``Reversible Logic Synthesis with Cascades of New Gate Families," *Proceedings of 6th International Symposium on Representations and Methodology of Future Computing Technology, RM 2003,* Trier, Germany, March 10-11, 2003, pp. 43-55
8) Michael Frank, "Reversible Computing", Article in Developer2.0, January 2004, pp34-41.
9) A Khlnopotine, M. Perkowski, and P. Kerntopf, Reversible logic synthesis by gate composition. *Proceedings of IWLS*2002. pp. 261 – 266.
10) P. Kerntopf, A comparison of logical efficiency of reversible and conventional gates. *Proceedings of 9th IEEEWorkshop on Logic Synthesis*, pp. 261-269, 2000.
11) De Vos, towards reversible digital computers. *Proceedings of European Conference on Circuit Theory and Design*, Budapest, pp. 923-931, 1997.
12) L .Sokoloff, *Metabolic Probes of Central Nervous System Activity in Experimental Animals and Man*, Sunderland, MA: Sinauer Associates, 1984.
13) J.G.McElligott and R Melzack, "Localized Thermal Changes evoked in the brain by Visual and Auditory Stimulation," Experimental Neurology, vol. 17, pg 293-312, 1967