A New Low Voltage CMOS 1-Bit Full Adder for Low-Power Applications

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Abstract: - In this paper, a new low-voltage low-power CMOS 1-bit full adder circuit is proposed. The proposed full adder can provide a full voltage swing at a low supply voltage and offers superior performance in both power and speed than the conventional full adder, the transmission full adder, and the recent low-voltage full adder. Based on the simulation results performed by HSPICE, the new low-voltage design consumes a minimal power and has a minimal power-delay product in TSMC 0.35um process as the supply voltage varies from 3.3V to 2V. Besides, this new cell is demonstrated to consume the minimal power as adopted in both a 4*4 bit carry-save array adder, and a 4*4 bit pipelined carry-save array adder.

Key-Words: - Low-Voltage, Low-Power, Full-Adder, Carry-Save Adder, Pipeline, CMOS

1 Introduction

Addition, multiplication, and multiply--then--accumulation (MAC) are the fundamental arithmetic operations in the VLSI systems such as microprocessors and digital signal processing (DSP) systems. Most of such arithmetic operations are based on the adder cells. The adder cell not only lies in the critical path, but also consumes the significant power [1-3].

In mobile systems and portable computers, there is only limited amount of battery power. So we must pay more attention to the low power circuit design to increase the battery life. Most of all, the low-voltage, low power design is our particular concern because the power consumption is proportional to the square of supply voltage. Although some high-performance full adder circuits have been proposed in the literature [4-7], they can't operate correctly at a low supply voltage because of the incomplete voltage swing in some internal nodes. Therefore, a full voltage swing becomes the key factor in the low voltage full adder circuit design.

The rest of this paper is organized as follows: in Section 2, we discuss the power considerations in CMOS VLSI circuits. In Section 3, we review the previous designs of 1-bit CMOS full adder cells. In Section 4, we present the new design of our proposed low-voltage high-performance CMOS 1-bit full adder circuit. In Section 5, we describe simulation results and compare the performance of the proposed low-voltage full adder with other circuits. Finally, we make conclusions in the final Section.

2 Power Considerations in CMOS

There are three major components of power consumption in CMOS circuits.

(1). Dynamic power: consumes due to charging and discharging the load capacitance during signal transition.

(2). Short-circuit power: consumes due to the existence of direct path from power supply to ground while both p-network and n-network are on simultaneously.

(3). Leakage power: is consumed by the leakage current in the static period,

which is also called static power. We can summarize the three major terms as the following equation [8]:

$$P_{total} = P_{dynamic} + P_{short} + P_{leakage}$$
$$= f_{clk} \cdot V_{DD} \cdot \sum_i \alpha_i \cdot C_{Li} \cdot V_{swingi} + Isc \cdot V_{DD} + I_l \cdot V_{DD}$$

where f_{clk} is the clock frequency, V_{DD} is the power supply voltage, α_i is the switching activity at node i, C_{Li} is the load capacitance at node i, V_{swingi} is the signal voltage swing at node i, I_{sc} is the short circuit current, and I_l is the leakage current, respectively.

In CMOS VLSI systems, dynamic power is the dominant one which accounts for about 85-90% of the total power dissipation, and short-circuit power accounts for about 10-15% of the total power dissipation in a proper sizing arrangement [9,10] while static power is determined by fabrication technology and usually is negligible in CMOS circuits.

As designing a low power CMOS 1-bit full adder, we can first try to reduce the total number of transistors and the total number of parasitic capacitances in internal nodes to reduce the load capacitance. Second, we may try to lower the switching activity to save the dynamic power consumption. Third, we may remove some direct paths from power supply to ground to save the short-circuit power dissipation. Fourth, we must try to balance each path in the full adder to avoid the appearance of glitches since glitches not only cause a unnecessary power dissipation but may even lead to a faulty circuit operation due to spurious transitions, especially in a low voltage operation system. Besides, in order to build a low-voltage full adder, all the nodes in the circuit must possess full voltage swing. Finally, we should put special emphasis on the low-voltage full adder design because the power supply voltage is the crucial factor in reducing power dissipation.

3 Previous CMOS 1-bit Full Adder Cells

In [1], the conventional 20-transistor transmission-gate full adder has been proposed as shown in Figure 1, which is called the conventional full adder in this paper. In [2], Zhuang and Wu simplified the conventional transmission gate full adder by using the transmission function theory and then proposed a new cell, which is called the transmission full adder, as shown in Figure 2. The transmission full adder only has 16 transistors, which consumes less power and operates faster than the conventional one. In [4-7], some high-performance 1-bit full adder cells have been proposed which only need 10-16 transistors to implement. All of them perform well at a normal 3.3V supply voltage, but all such full adders suffer the problem of signal degradation and therefore can't work properly in low voltage systems. We illustrate in Figure 3 the 14-transistor 1-bit full adder cell proposed in [4] as a reference latter in Section 5. In [3], Lee and Sobelman alleviated the problem of threshold voltage and a non-zero standby power consumption in 14-transistor full adder proposed in [4], and presented a new low-voltage full adder as illustrated in Figure 4.

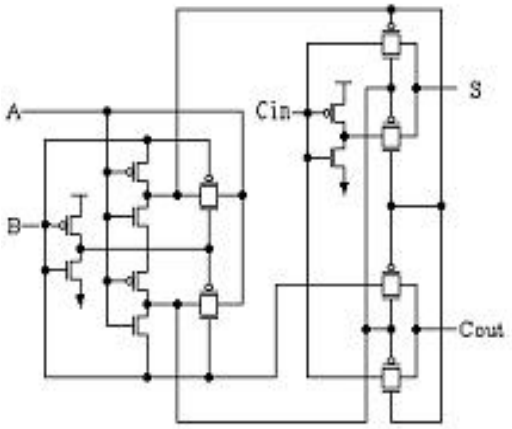

Figure 1: Conventional full adder

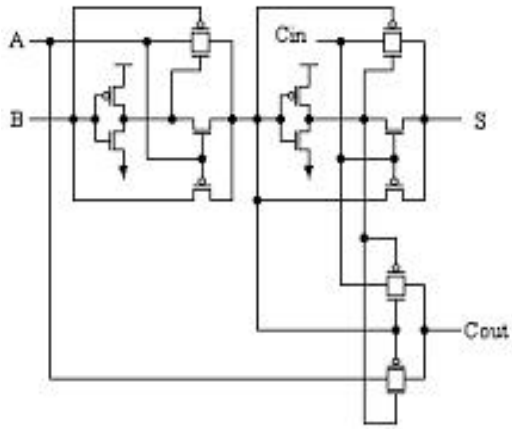

Figure 2 : Transmission full adder

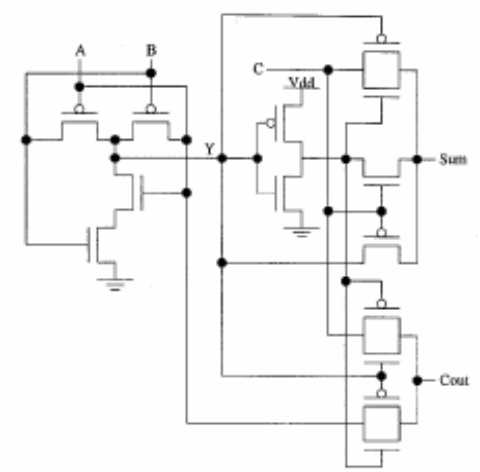

Figure 3: 14-transistor full adder in [4]

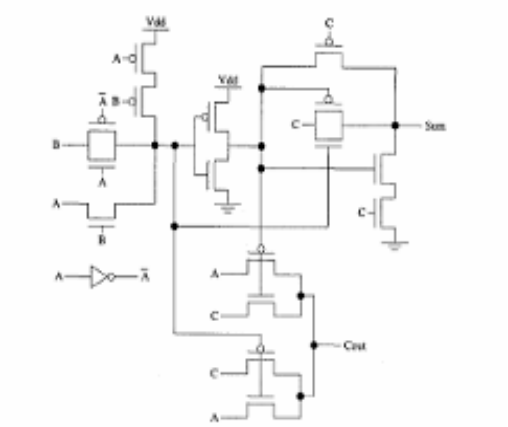

Figure 4 : 18-transistor low-voltage full adder

4 The Proposed Low-Voltage Full Adder Cell

We propose a new 18-transistor low-voltage full adder circuit as illustrated in Figure 5. The transistor number in our new design is not the fewest one (transmission full adder has only 16 transistors), but there are fewer glitches existing in our new design as compared with the 16-transistor transmission full adder because XOR and XNOR gates are generated simultaneously. Due to fewer glitches in our design, the power can be saved and it has a superior speed enhancement at the same time. The conventional full adder cell also generates XOR and XNOR results simultaneously, but its output stage that generates Sum and Cout is too complex. Because the number of inverters in our new cell is only one, which saves one inverter as compared with the other low-voltage full adder cells, the switching activity in our design is lower and the direct path from supply voltage to ground is less. As a result, both dynamic power and short-circuit power can be reduced; and moreover, the speed in the full adder can be increased since the inverter in the critical path has been removed.

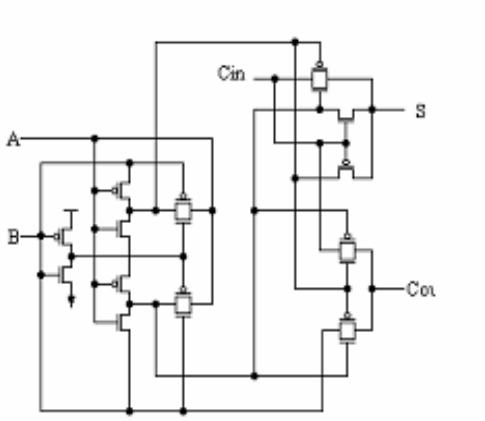

Figure 5 : The new 18-transistor low-voltage full adder

Based on simulation results, our 1-bit new full adder design not only consumes the lowest power, but it also operates nearly fastest (nearly the same speed as 18-transistor full adder in [3]) as V_{DD} varies from 3.3V to 2V in TSMC 0.35um technology, and consequently the proposed new cell has a minimal power-delay product (PDP). Besides, the new proposed cell is shown to consume a minimal power as adopted in a 4*4 bit carry-save array adder, and a 4*4 bit pipelined carry-save array adder.

5 Simulation Results

Simulation results are performed by HSPICE based on TSMC 0.35um CMOS process with supply voltage from 3.3V to 2V. In simulations, all transistors size in the full adder cell are set to the same as W=3um, L=0.35um in PMOS and W=1um, L=0.35um in NMOS, respectively. The operation frequency is at about 100MHz.

Figure 6 illustrates the waveforms of 16-transistor full adder in [5] operated at 2V. Due to threshold voltage losses in some internal nodes, the 16-transistor full adder cell can't operate properly at a 2V low supply voltage. Figure 7 shows the waveforms of the proposed 18-transistor low-voltage full adder, which performs very well at a 2V low supply voltage because all nodes in the cell possess a full voltage swing. In Table 1, Table 2, Table

3, and Table 4, we establish some models according to different loadings for the performance in both power and speed in the conventional full adder [1], the transmission full adder [2], and the low-voltage full adder [3], and the proposed new low-voltage full adder, respectively. And then, we extract the data of power and speed from the established model with loading from 0.05p to 0.2p (In synchronous systems, the loading of register in the output of full adder is usually smaller than 0.1p) to evaluate the PDP as shown in Table 5. As a result, the proposed new design consumes the lowest power and it has a minimal PDP as compared with other low-voltage adder cells. At V_{DD}= 2V, our new design performs an improvement of 13.16%, 2.73%, and 20.75% in power consumption, respectively; meanwhile, our new design has the minimal PDP value, with an improvement of 11.84%, 19.05%, and 14.16%, respectively. The compared results in power and PDP as the supply voltage varies from 3.3V to 2V is shown in Figure 8.

Finally, we adopted the new proposed 1-bit full adder cell in a 4*4 bit carry-save array adder, and a 4*4 bit pipelined carry-save array adder in Figure 9, respectively. Based on the same clock frequency about 100MHz, our proposed cell consumes a minimal power as compared with other low-voltage adder cells

Figure 6: Simulated waveforms of 16-t full adder [5] at V_{DD}=2V (wrong results)

As shown in Table 6 for V_{DD}=2V, our proposed cell performs well, and it only consumes 0.732mW in a 4*4 bit carry-save array adder and 0.718mW in a 4*4 bit pipelined carry-save array adder including the clock driver and registers.

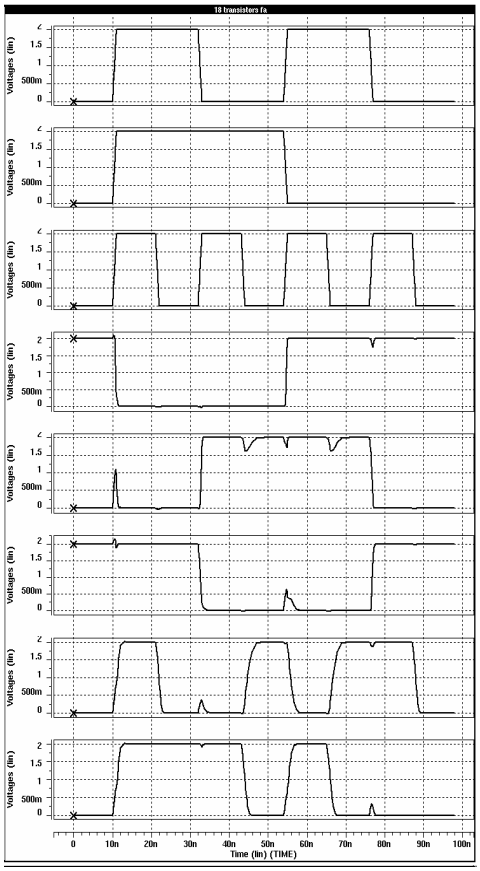

Figure 7: Simulated waveforms of proposed 18-t new low-voltage full adder at V_{DD}=2V

Table 1: Simulation results of conventional full adder

20t fa in 3.3V	Loading	0.05p	0.1P	0.15p	0.2p	0.25p	0.3p
proposed in [1]	Power (uw)	45.5	66.3	89.7	114	140	166
	Delay (ns)	0.09	0.16	0.22	0.27	0.32	0.37
20t fa in 2V	Loading	0.05p	0.1P	0.15p	0.2p	0.25p	0.3p
proposed in [1]	Power (uw)	14.4	23.1	32.4	41.9	51.7	61.5
	Delay (ns)	0.17	0.29	0.42	0.55	0.74	0.83

Table 2: Simulation results of transmission full adder

16t fa in 3.3V	Loading	0.05p	0.1P	0.15p	0.2p	0.25p	0.3p
proposed in [2]	Power (uw)	32.5	53.5	77	102	128	154
	Delay (ns)	0.1	0.16	0.22	0.27	0.33	0.4
16t fa in 2V	Loading	0.05p	0.1P	0.15p	0.2p	0.25p	0.3p
proposed in [2]	Power (uw)	11.7	20.4	29.9	39.5	49.4	59.2
	Delay (ns)	0.18	0.32	0.48	0.69	0.82	0.92

Table 3: Simulation results of low-voltage full adder[3]

18tlfa in 3.3V	Loading	0.05p	0.1P	0.15p	0.2p	0.25p	0.3p
proposed in [3]	Power (uw)	44.6	66.3	90.6	116	142	169
	Delay (ns)	0.1	0.16	0.22	0.27	0.31	0.36
18tlfa in 2V	Loading	0.05p	0.1P	0.15p	0.2p	0.25p	0.3p
proposed in [3]	Power (uw)	15.4	24.7	34.6	44.6	54.5	64.6
	Delay (ns)	0.18	0.29	0.4	0.5	0.6	0.68

Table 4: Simulation results of proposed 18-t new low- voltage full adder

new fa in 3.3V	Loading	0.05p	0.1P	0.15p	0.2p	0.25p	0.3p
	Power (uw)	31	51.7	74.8	99.7	125	152
	Delay (ns)	0.09	0.16	0.22	0.27	0.32	0.38
new fa in 2V	Loading	0.05p	0.1P	0.15p	0.2p	0.25p	0.3p
	Power (uw)	11.3	19.9	29	38.6	49.1	58.1
	Delay (ns)	0.17	0.29	0.42	0.57	0.8	0.93

Table 5: Normalized performance comparison

		Conv. 20t FA	Trans. 16t FA	18t FA in [3]	18t new FA
In 3.3V	Power	1.2278	1.0303	1.2344	1
	Delay	1.0014	1.0163	1.0041	1
	PDP	1.2295	1.0471	1.2395	1
In 2V	Power	1.1316	1.0273	1.2075	1
	Delay	0.9883	1.1589	0.9454	1
	PDP	1.1184	1.1905	1.1416	1

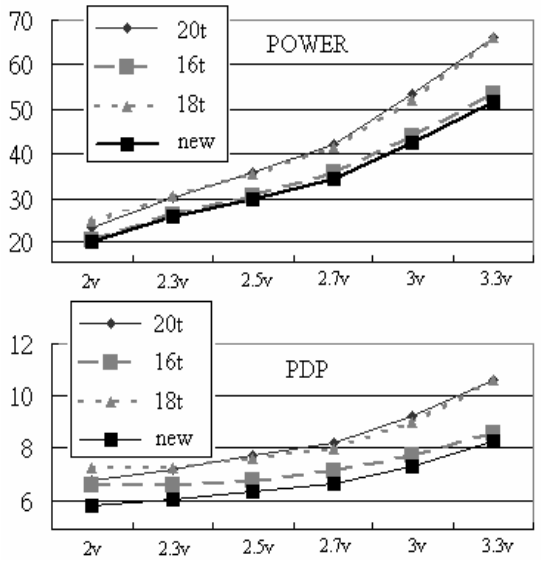

Figure 8: Compared results of power and PDP as V_{DD} from 3.3V to 2V

Table 6: Power consumption in 4*4 bit Carry save adder and 4*4 bit pipelined carry-save adder

Power (mw)	3.3v	normal	2v	normal
4bccfa	2.462	1.082	0.789	1.078
4b16tfa	2.287	1.005	0.744	1.016
4b18tlfa	2.703	1.188	0.82	1.12
4b18tfa	2.275	1	0.732	1
4bpipeccfa	2.985	1.253	0.764	1.064
4bpipe16tfa	2.507	1.052	0.738	1.028
4bpipe18tlfa	3.118	1.309	0.768	1.07
4bpipe18tfa	2.382	1	0.718	1

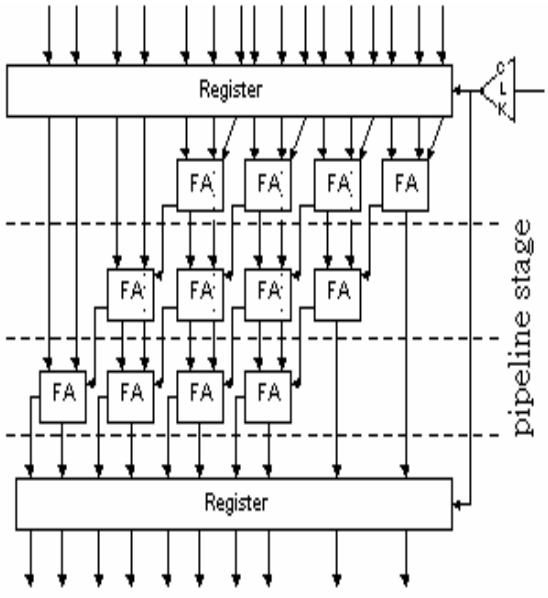

Figure 9 : 4*4 bit carry-save adder and pipelined carry-save adder (with pipeline stage)

6 Conclusions

In this paper, a new low-voltage high-performance CMOS 1-bit full adder circuit is proposed. The proposed cell can provide a full voltage swing at a low supply voltage. Based on simulation results performed by HSPICE in TSMC 0.35um SPTM CMOS process with 2V supply voltage, the new low-voltage design consumes a minimal power and has a minimal PDP with an improvement of 11.84%, 19.05%, and 14.16% than the conventional full adder [1], the transmission full adder [2], and the low-voltage full adder [3], respectively. As we

adopted the new proposed full adder cell in both a 4*4 bit carry-save array adder, and a 4*4 bit pipelined carry-save array adder, it performs well at 2V supply voltage with a minimal power consumption of only 0.732mW and 0.718mW, respectively, as compared with other adder cells.

Acknowledgment

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