A New CMOS Image Sensor with Pixel-Shared Design and Split-Path Readout Circuit

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Abstract: - In this paper, a new CMOS active pixel sensor (APS) of 128X128 resolution is proposed for high quantum efficiency. The presented CMOS image sensor can operate at the power supply of 3.3V, and use both a new pixel-shared structure and split-path readout direction. This new method has the advantage that the number of transistors in each pixel is reduced to increase the fill factor by enlarging the photo-sensing area; on the other hand, it also raises the speed of readout, and is twice as fast as that of the traditional single direction readout. Besides, we use a delta-difference sampling (DDS) for the readout circuit to suppress the Fixed Pattern Noise (FPN). The complete CMOS image sensor is implemented based on TSMC 0.35μm 1P4M CMOS technology.

Key-Words: - Active Pixel, Image Sensor , Fill Factor, Readout, Fixed Pattern Noise

1 Introduction

The image system technology has been applied in various fields including camera, medical, examination, astronomy, and other strategic equipment. Photo-sensor plays an important role in OEIC (OptoElectronic Inte -grated Circuit). Nowadays semiconductor still camera system using CCD image sensors offer an excellent resolution, but they need high voltage about 12V~15V for maintaining high charge transfer efficiency (CTE). CMOS active pixel sensor (APS) is well known for its possibility of integration with peripheral circuits, low voltage operation, standard CMOS process, random access and low cost as compared to CCD [1-11].

Photo-detectors are very important building blocks in CMOS imagers. The image quality of such systems is mainly determined by the performance of individual pixel in which the acquisition of the image is realized. A good sensor design is one of the important keys in the realization of a successful CMOS imager. For this reason, it is very important to pay more attention to the design of the CMOS pixel.

In this paper, a new image sensor pixel structure is proposed to reduce the complexity of each pixel to only two transistors. On the other hand, we use the manner of pixel-shared split-path readout on the active pixel design.

2 Pixel Structure and Circuit Diagram

2.1 Photo-detector

In the proposed CMOS APS, the P-N junction diode technology is used as the photo-detector (PD), as shown in Fig. 1. The PD1 and PD2, which are operated under reverse biased, are used as the photo-sensing devices. When the radiated photons are absorbed, the excited photo-current flows through the reverse-biased junction diode. The photo-current is proportional to the intensity of light.

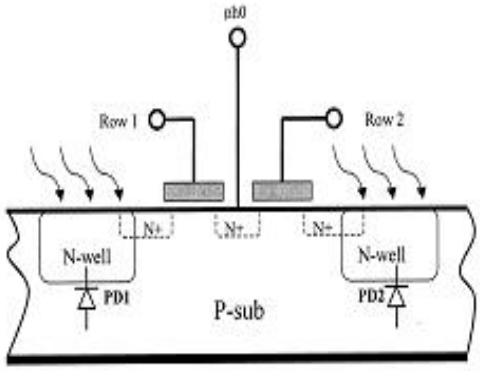

Fig. 1 Cross section of the proposed pixel-shared structure

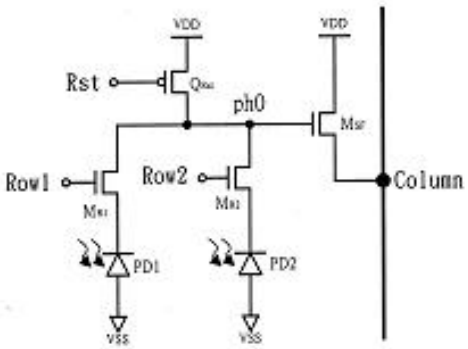

Fig. 2 Proposed pixel-shared design

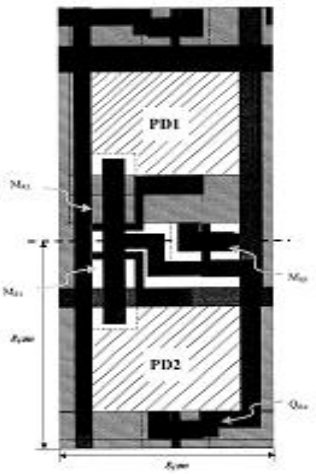

Fig. 3 Layout of pixel-shared circuit (2 pixels)

2.2 Sensor Structure

Fig. 2 is the proposed schematic pixel structure. In this structure, an active pixel sensor with a common readout method is used so that each pixel only contains two transistors. Due to the reduction of the transistor count, the size of each pixel is 8×8 μm^2 as shown in Fig. 3, and the fill factor can be increased to 49% to enhance the quantum efficiency.

Besides, the transistor Q_{rst} should be a PMOS component, since as the working voltage is reduced, if the transistor Q_{rst} is made by an NMOS component, due to the body effect, the voltage on node ph0 will be less than VDD with the value of Vt. Then, transistor MSF can not work properly for low supply voltage.

Therefore, we choose the transistor Q_{rst} as a PMOS device, the body effect will be avoided, then the circuit is more easily to be operated under the lower voltage condition. Fig. 4 shows the timing diagram of the shared readout image sensor. First, *Reset* is changed to 0V, Q_{rst} turned on, and Row1 is changed to VDD at the same time, MR1 turned on, so that node ph0 is reset to VDD.

Then, Reset is changed to VDD, Q_{rst} turned off. The voltage of node ph0 will be dropped for the photo-current produced by the PD1. After a time interval, Row1 is changed to 0V, MR1 turned off, and the voltage of ph0 will be amplified by MSF to transfer to Column. PD2 is operated in the same way.

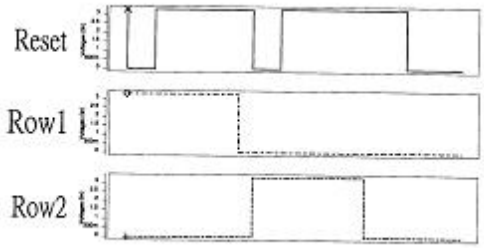

Fig. 4 Timing diagram of controlling shared readout pixel

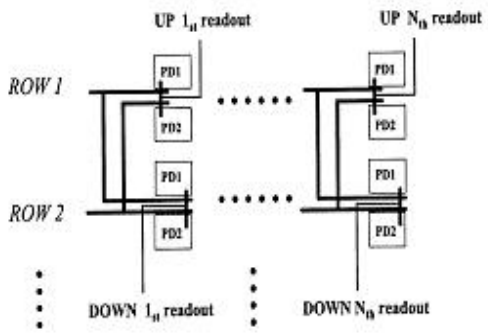

Fig. 5 Structure of split-path readout

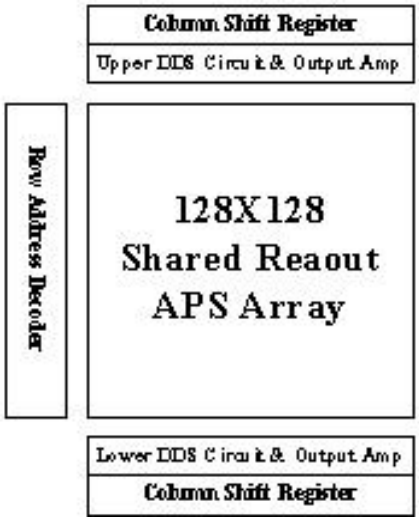

Fig. 6 Complete block diagram of the sensor array.

Fig.5 schematically illustrates an imaging sensing device compromising the active pixel sensors, wherein for brevity, only the photodiodes, PD1 and PD2, arranged in a 2-dimentional array of rows and columns are depicted. The block diagram of the sensor is shown in Fig. 6. The complete image sensor includes row address decoders, and upper 、 lower delta-difference sampling circuits (DDS) and output amplifiers, upper、lower column shift registers. In this way, the image sensor has the capability of random addressable process. By using the manner of split-path readout, the speed of readout is twice as fast as that of the traditional single direction readout.

2.3 Delta-Difference Sampling Stage

Delta-difference sampling (DDS) can decrease the effect of the reset noise by computing the difference between the output voltage after reset and integration [4]. The circuit of DDS which consists of a crowbar switch (DDS) and two-column selection switches on either side (M3 and M5) are added to selectively short the two sample-and-reference capacitors MC1 and MC2 formed by PMOSFET as shown in Fig. 7. The timing diagram is shown in the same Figure. By subtracting the image signal V_{ims} and the reference level Vref, the fixed pattern noise (FPN) dominated by column-to-column due to the column parallel readout structure can be suppressed to improve the image quality. Moreover, by shorting the two sample-and-reference capacitors in the column, the offset due to threshold voltage variations is removed [4].

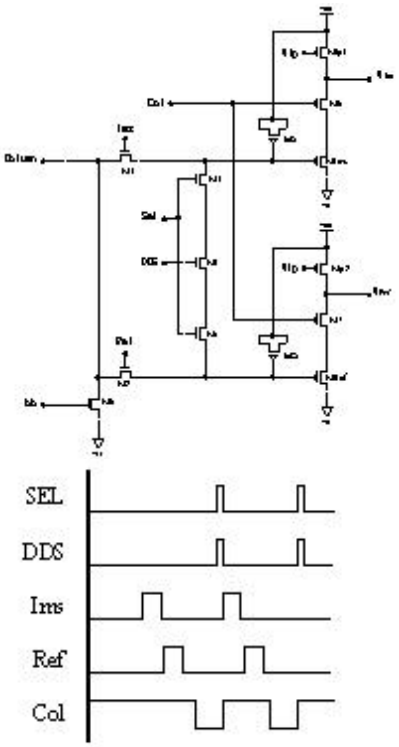

Fig. 7 DDS circuit and the corresponding control signals [4]

3 Measurements and Simulation Results

The 128×128 CMOS image sensor is designed based on TSMC 0.35μm 1P4M CMOS technology. The current response of photo-diode formed by Nwell-Psub is measured by HP4156A, and the measurement results are shown in Figs. 8 and 9, respectively. Fig. 8 shows the photo-current under the injecting light of 490nm、580nm and 620nm wave length. Fig. 9 shows the photo-current under the injecting of 350mcd、550mcd、750mcd and 950mcd light intensity.

Table 1 compares the fill-factor of the proposed design with some selected prior art CMOS imagers. The transistor count of our proposed pixel structure is only two. Therefore, a high fill factor of 49% is obtained.

Table 1 Fill-factor comparison for various CMOS pixels

Pixel design	CMOS Technology	Pixel size (μm^2)	Resolution	Count of transistors in each pixel	Fill factor
this work	**0.35 μ m**	**64**	**128X128**	**2**	**49%**
[5]	1.2 μ m	576	128X128	4	25%
[6]	0.5 μ m	56	2048X2048	3	25%
[7]	0.8 μ m	117	800k	3	26%
[8]	0.18 μ m	88	352X288	3	15%
[9]	0.35 μ m	86	512X384	4	24%
[10]	0.5 μ m	100	1024X1024	3	45%(*QE)

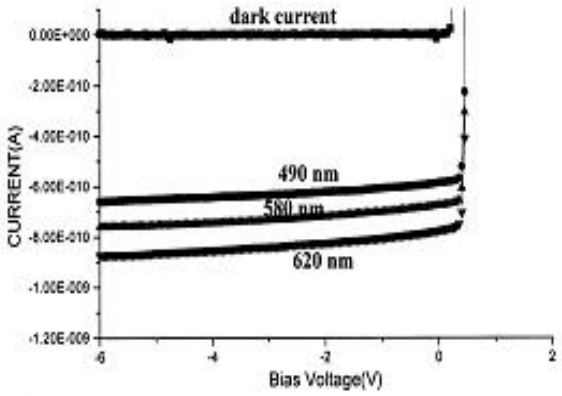

Fig. 8 Photocurrent measurements under The injecting light of 490nm、580nm and 620nm wave length.

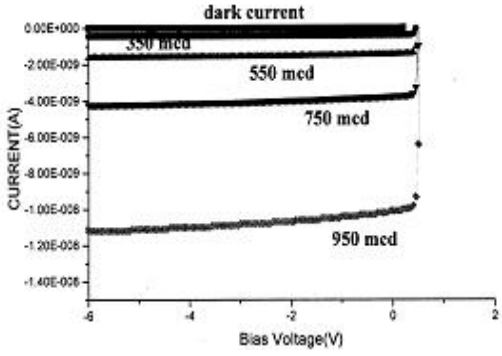

Fig. 9 Photocurrent measurements under the injecting of 350mcd、550mcd、750mcd and 950mcd light intensity.

This consequence will lead to higher quantum efficiency and better dynamic range. Simulation results of the designed CMOS image sensor, as depicted in Fig. 10, show the voltage of Vims and Vref for input Photo-current from 2nA to 12nA. Judging from simulation results, the power consumption is 52mW for a single 128 pixel-array at 3.3V power supply, and the frame readout rate can achieve 300 frames per second. The overall simulation results are summarized in Table 2. The whole chip layout of the complete CMOS image sensor is shown in Fig. 11.

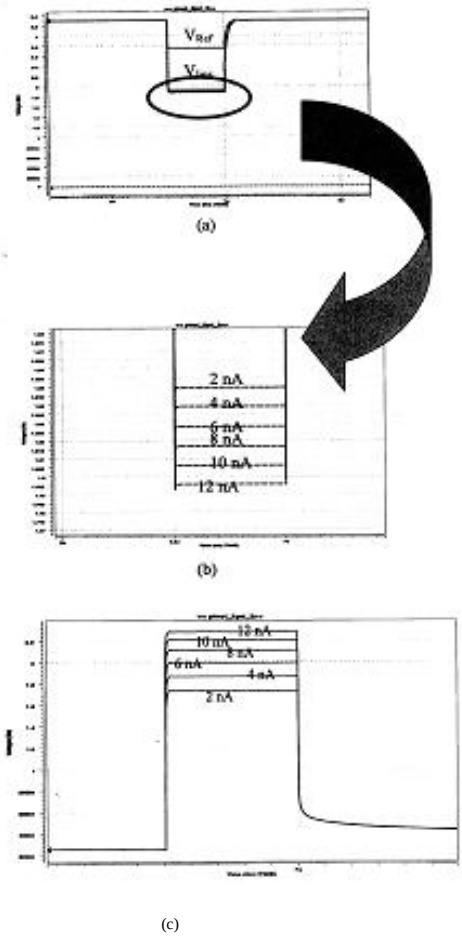

Fig. 10 Simulation results of the CMOS APS image sensor

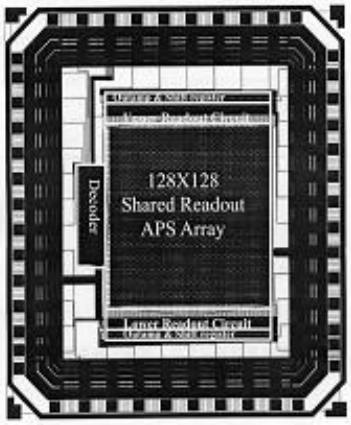

Fig. 11 Chip layout of the CMOS image sensor

Table 2 Chip summary

128X128 Active Pixel Sensor	
Process technology	0.35 μm SPQM
Photodetector	N-well/P-sub Photodiode
Pixel type	Active
Array size	128 x 128
Pixel size	8 x 8 μm^2
Chip size(include pads)	2400 x 2800 μm^2
Power supply	3.3V
Power consumption	52mW*
Fill factor	49%
Maximum frame rate	300 frames/per second
Dark response	~10pA
DDS	Yes

* A single 128 pixel-array at 3.3V power supply

4 Conclusion

In this paper, a split-path readout 128X128 CMOS APS image sensor has been designed and analyzed. By using the proposed readout manner, twice readout speed can be achieved. On the pixel design, a new pixel-shared structure with a common readout has been proposed and verified. Due to this new structure, a high fill-factor of 49% has been achieved in a standard 0.35μm CMOS technology. This high fill-factor makes this pixel structure very suitable to meet high performance CMOS image applications.

Acknowledgment

This work was supported in part by the National Science Council of TAIWAN, ROC under contracts NSC 89 – 2213 – E – 182 – 044 and NSC 92-2220-E-182-002.

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