# Low cost Digital Oscilloscope

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**ABSTRACT**
In this paper a digital oscilloscope implementation is described. An FPGA (Field Programmable Gate Array) is used in order to signal capture, processing and visualization. The goal of this design is provide a cheap and reliable solution to electronics and informatics students to represent analog signals. In our proposal commercial components are used (FPGAs Spartan II, 80 MHz DAC ...) and the visualization only need an VGA compatible screen. We could obtain electric signals plots for around a hundred of Euros.

**KEY WORDS**
FPGA, oscilloscope, signal processing

## 1 Introduction

The electronics, it is an area in which besides a few extensive theoretical knowledges, in the practice we need diverse devices of instrumentation, since he can be a polimeter, a oscilloscope or a signal generator. But of all of them the Oscilloscope stands out, especially, since it is the only one that provides a graphical and intuitive way of showing the relative information a sign. The principal disadvantage is the price. In general it is prohibitive, except for companies or organizations. An oscilloscope like that we have in the laboratories of Electronics of the UMH overcomes 1500 Euros.

### 1.1 Motivation and Aims

The main aim is to manage to fulfils a simple, functional, small oscilloscope, capable of sampling to sufficient frequency and with the sufficient precision for the needed in our qualifications. All this thinking that the cost of the same one is approximately 100 Euros.

## 2 The Digital oscilloscope

Opposite to the classic analogical oscilloscope the oscilloscope Digital [4] is imposed increasingly up to such a point that already practically the analogical ones are not in use. The principal reason of this phenomenon is the extraordinary evolution of the Digital Electronics. Every time the manufacturers of Digital chips manage to realise smaller chips, with major number of transistors, capable of working every time to more speed and to minor cost.

The basic functioning of the digital oscilloscope we can see it in the figure 1. It has, as any equipment of instrumentation, of a stage of Conditioning sign. The ADC (Analog to Digital Converter) is in charged of sampling the signal and of the quantification of this value. This part of the oscilloscope is specially critical, since depending on the sampling rate and the precision level of the converter (levels of quantification), it will define the principal characteristics of the oscilloscope. Once sampled the values are stored in a digital memory for later processing and visualization. The Digitals oscilloscope , thanks to the digital logic, can realise complex calculations on the information stored in the memory. This one is a great advantage of the Digital oscilloscopes opposite to the Analogical ones; the

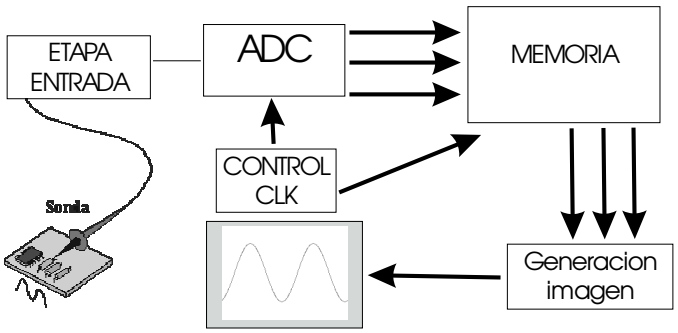


Figure 1. Digital oscilloscope schematics

processing of the captured data. Nevertheless, the principal virtue opposite to the classic oscilloscope appears at the moment of visualising not repetitive or random signals. The classic oscilloscopes base on periodic income to generate signs in tooth of saw, indispensable for the correct visualization. On the other hand in the foxgloves this does not happen. What provides the aptitude to visualise any type of entry so much, periodic as random.

## 3 Digital Logic

In this paragraph we will explain the tools used for the implementation of the Digital Logic necessary for the manufacture of our oscilloscope.

### 3.1 SoC: System on Chip

For our logical design since(as,like) we see in the figure 1, need to implement a memory(report), generator of image VGA and hardware in charge of the control and of the trigger. When we stop to think the components that we need to implement all these modules we would realise immediately the complexity of the project.

For this motive we have decided to implement the whole digital logic inside a FPGA. So we obtain:

- the whole logic Implements in one only chip (SoC).
- Can design our modules to measure, without us having to restrict to the existing ones on the market. We are the persons in charge of the functioning of each one and can implement them such and since(as,like) let's need.
- flexible, scalable and modifiable Design. Only in spite of rescheduling the FPGA we can change any aspect of our design, so much correct mistakes as the design to extend.
- To reduce Costs. It turns out to be a more economic the disbursement of the only FPGA than that of many components that do the same function.
- Major Productivity. The design is simpler and rapid on our chip that the design with devices of different manufacturers and with characteristics that surely are not exactly the wished ones.
- Reduction of the size. The motherboard, where all the necessary chips are will be more limited.

### 3.2 What is a FPGA?

An FPGA is, as its name say, a Field Programmable Gate Array. Let's see of that this array of gates consists.

An FPGA is organised in:

- CLBs (Configurable Logic Block ): An array of cells regularly arranged on the chip, these CLBs are programmable.
- IOBs (Input Output Block): It is the programmable connection with the pines of entry exit arranged about the chip.
- PSM (Programmable Switch Matrix): Blocks of interconnection, which under programming the CLBs allow to connect between yes or with IOBs.

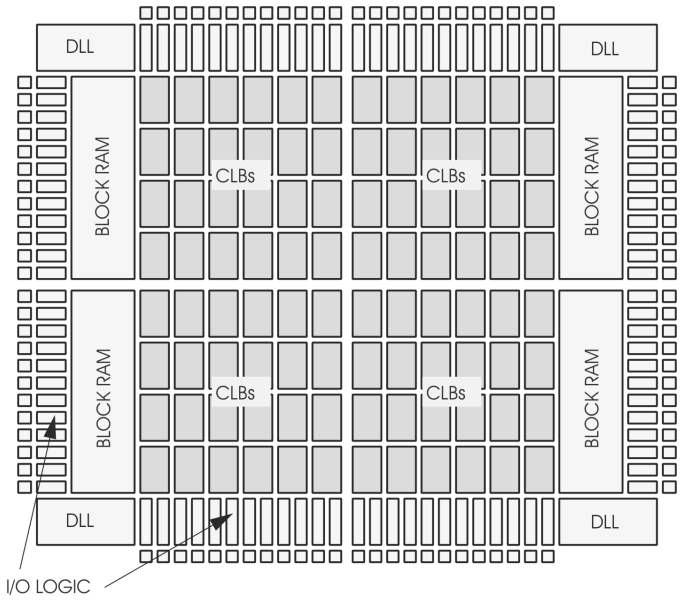


Figure 2. Internal composition of an FPGA: CLBs and IOBs

Every CLB is composed by 2 programmable cells called Slices. Every Slice is capable of containing any logical function of 5 variables. By means of the suitable programming of these CLB's and Slices there is achieved that the FPGA realises the wished functions.

The main characteristics of a FPGA are: the speed to the one that can work and the number of Slices that it possesses, since this one is the one that is going to limit the size of the design that I can implement in it.

### 3.3 Design Tools

We work with a FPGA Xilinx's Spartan II, have used the software Xilinx ISE 5.1[7] with that we synthesise the code programmed in VHDL[2] [5]. VHDL is a language of description of Hardware (HDL) very extended in the area of the programming of Programmable Logic Devices (PLDs). To the being a language HDL, it allows to us to create modular elements, giving the possibility of interconnecting them and re-using so often like need. For the simulation of the code VHDL there has been in use the software Active-HDL of Aldec [1]. With that the design has been purified up to obtaining an ideal result. The last one I pass once simulated the project, it is synthesising it for our FPGA. For it Xilinx's software takes charge realizing different stages:

1. Synthesis: the file is generated *netlist* from the code VHDL. *netlist* is a description of the design to level RTL.

2. Implementation: In this phase the previous file is implemented for the FPGA or logical selected device. It distinguishes the design forming adequately the CLBs, IOBs and PSMs.

3. Generation of *bit stream*. *bit stream* is the programmable file in the FPGA. It includes the necessary orders to make to know to the FPGA the configuration calculated in the previous phase.

## 4 Oscilloscope Implementation

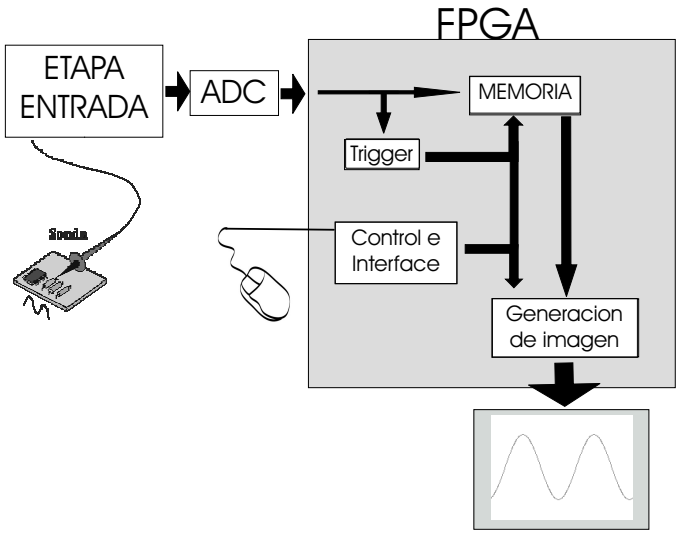


Figure 3. Digital oscilloscope blocks diagram

After evaluating the needs of the project and the different alternatives of implementation, there has been distinguished the structure of an oscilloscope showed in the figure 1 taking advantage of the advantages that the FPGA's can offer us and of the design SoC.

The scheme of our oscilloscope is the showed one in the figure 3. In it, it is possible to observe, the analog stage of acquisition and conditioning, and on the other hand the digital electronics that has been implemented in a FPGA.

### 4.1 Used material

For the development of the design of the oscilloscope Digital we have used the following elements

- Converter ADS831-E [6]. This one is a converter that works for successive approximations, provides to the exit eight bits, with binary codification or in complement to two, according to the needs. It is commercialised by the company Burr-Brown belonging to Texas Instrument, in an encased SOIC.
- Active filter low step implemented with the THS4061.
- Tension constrainer of entry with the utilization of Zener diodes.
- Tension fastener using two operational amplifiers 741[3].
- Selector of scales, using resistances of different values, THS4061 and one analogical multiplexer (AD8174) of great bandwidth.
- Xess XSA-100. Plate of development commercialised by Xess in which we have of:
  - Xilinx Spartan II FPGA of 100 thousand logical equivalent gates.
  - Interface VGA. VGA has connector and of converter DAC of 2 bits for colour (6 bits = 64 colours) by means of considered resistances.
  - Connector PS/2. By means of which it is possible to connect a keyboard or mouse (in our case a mouse).
  - programmable Clock up to(even) 100MHz.
  - Other components that have not been necessary to use: 16 Mbyte SDRAM, 256 KByte Flash, 7-segment LED.
- Monitor VGA of a conventional PC for the visualization.

### 4.2 Signal Processing

An oscilloscope is an instrument of visualization of signals. It can show any type of signal, already be seismic, beatings of the heart, electromagnetic waves etc ... always and when he has been provided with a suitable transducer. The measurements that an oscilloscope has to do have to be very precise and it is here where the system of acquisition

of information has great importance, since any mistake initially of the system would provoke a result that would be far much from the reality.

Our system conditioner of signal allows to select between coupling CC and CA. Filtering or not the continuous component of the input. Equally, it attenuates or amplifies the signal of entry by means of a selector on a large scale.

For the implementation of the stage of acquisition of information we need:

1. A filter to prevent it from producing Aliasing as what the signal of entry does not have to have component frequency over 2*fs. Theoretically the maximum bandwidth in which we can move comes determined by the ADS831-E (analog to digital converter) that, for Nyquist's criterion, the maximum fix us to 40 MHz.

2. A set of circuits that fix the tension level to the range accepted by the analog to digital converter since this one must work between 1.5V and 3.5V.

3. An analog to digital converter. The converter that we have used (ADS831-E), was chosen principally by the great bandwidth that it possesses and especially for his reasonable price.

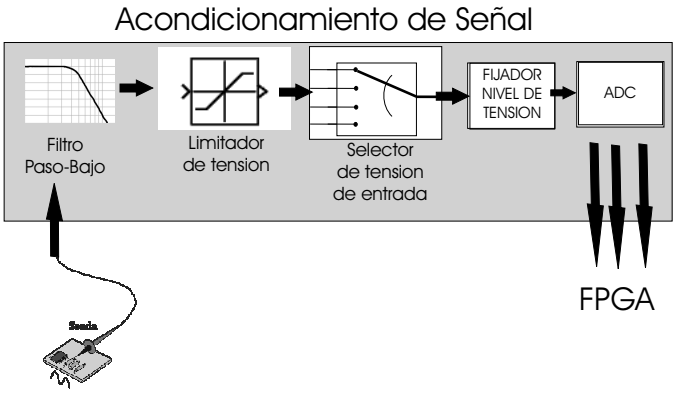


Figure 4. Signal conditioning

## 4.3 Digital Memory

The memory of our oscilloscope is one of the most critical points of the project. This memory has to be capable of writing in it the data who comes form the converter and, simultaneously, to read them for his visualization.

The memory has to be capable of guarding so many points as horizontal pixels have our screen VGA (640x480). Bearing in mind that our A/D converter has a word of 8 bits it will be enough to us with a memory of:

$640x8bits = 5120bits = 640bytes$

The implementation of the same one has realised by means of the tool *Xilinx CORE Generator* [8] that we have been generated by a memory of double port synthesised and optimised by Xilinx for his FPGAs.

We have programmed a module that manages the reading and writing of the same one. The writing fulfils consecutively from the address 0 up to 640 when the control of the trigger indicates it to us. This does that for our VGA it(he) is so simple to read all the information that it contains whenever we draw one of 480 vertical lines that has our screen.

## 4.4 Visualization

Such as we have explained previously the principal aim of the project is obtain an oscilloscope to low cost. For this motive we have thought that the best option is that the visualization does to itself by means of a monitor VGA because:

- To cheapen costs. If we do not integrate a screen in the system the price diminishes drastically.

- Screens very widespread VGA. The PCs for example use screens compatible with VGA. Our oscilloscope will be able to be visualised in any of these screens.

- Easy implementation. Thanks to the power of the FPGAs the implementation of a module that generates the signals VGA is relatively simple.

The VGA signals can divide into two groups:

- Of synchronism. Horizontal and vertical synchronism. They indicate to the screen the frequency to which they have to realise the refreshment of every vertical line or of every image.

- RGB. They indicate, by means of 3 analogical signals, the intensity of the component of Red, Green and Blue of every pixel. To generate it there is in use an ADC of 2 bits for colour based on a network of resistances considered, which provides to us a whole of 64 colours.

# 5 Results

We have managed to implement a digital oscilloscope of low cost, to visualise the signals there is used a screen of computer and a mouse to control the complete functioning of the oscilloscope (trigger, type of coupling, you climb etc ...). The circuit might be implemented in a plate of 10*10 cm. For what is a perfectly portable system to any place.

## 5.1 Other commercial devices

On the market different alternatives exist at the moment of be doing by an oscilloscope. A digital oscilloscope is about them 1500€ but it yes with a few characteristics very over our possibilities (fs=1Ghz, BW=60Mhz). There exists also

oscilloscopes of storage (DSO) based on PC much more economic (some 500€) that connect to him(it) by means of parallel port or USB. Characteristics (fs=250Mhz, FFT, AD 8 bits, memory=1k) his principal disadvantage is that a computer is indispensable. Our oscilloscope is much more modest fs=25Mhz, 8 bits of resolution, 640 bytes of memory (extend able to 40kbits). In addition it does not need a PC to work only a screen which turns it in the most flexible and portable. With a cost near of 100€ it is an alternative more than interesting to what the market offers.

## 5.2 Future work

Taking advantage of the reconfigurability of the FPGA it is tried in a future to implement in the same circuit:

- To include the second channel of acquisition. (It needs to modify the hardware and the software)
- Increase of memory of storage. (Used FPGA has of 40kbits).
- Accused of information: To include technologies of divided equally and detection of harmonic.
- Analyzer of spectra.
- Generator of signals. (Including a DAC in the circuit).

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