SYMBOLIC NOISE ANALYSIS FOR MOST CIRCUITS USING NULLORS

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ABSTRACT

A novel technique oriented to compute Noise Figure (NF) for MOS Transistor (MOST) circuits, is presented. The proposed method uses the features of symbolic analysis. In order to improve the computation time, a pure-nodal-analysis (PNA) method is applied by modeling all elements using the nullor. Two illustrative examples are given where the NF is computed using the proposed method and compared with HSPICE simulations, the results demonstrates the suitability of the proposed method.

1. INTRODUCTION

Numerical circuit-simulators have been very useful to compute the figures of merit such as: noise [1, 2], distortion [3], and stability [4], in order to improve a design. However, symbolic computing is making significant impact in analog design, since a symbolic-expression helps to gain insight about the behavior of a circuit. In this manner, a CAD-oriented method focused on the symbolic computation of NF for MOST circuits, using the nullor concept [5, 6], is described. The nullor is used to model the behavior of a MOST, and all non-NA-compatible elements [3, 7], in order to avoid the handling of stamps. That way, it is shown that by using the PNA method, both the computation time and the handling of symbolic expressions being improved. It is worth to mention that the proposed model for a MOST includes the effect of the most significant noise-sources [8], the technology dependence and the biasing region [9].

The concepts of noise and NF are described in section 2, where it is assumed that noise sources are uncorrelated, as it is used in most of the circuit simulators. Section 3 is devoted to consider the relevant noise sources of a MOST. The proposed method is described in section 4. Several examples are given in section 5, where the proposed method is compared with the simulation results using HSPICE. Finally, the conclusions are listed in section 6.

[*]Sánchez-López holds a scholarship at INAOE from CONACyT-MEXICO.

2. NOISE AND NOISE FIGURE

Noise can be defined as any interference unrelated to the signal of interest [1, 2]. Noise is characterized by a probability density function (PDF), and a power spectral density (PSD). The PSD of a signal $x(t)$ is denoted by $S_x(f)$, and it shows how much power the signal carries in a unit bandwidth around frequency f, which is defined as the average normalized noise power over a 1Hz bandwidth, and it is a positive real valued function. The most commonly accepted definition for NF is given by equation (1), where SNR_{in} and SNR_{out} are the signal-to-noise ratios measured at the input and the output, respectively.

$$NF = \left. \frac{SNR_{in}}{SNR_{out}} \right|_{T=300^{o}K} \tag{1}$$

NF is a measure of the degradation of the SNR as the signal passes through a system [7]. For a noiseless circuit $SNR_{in} = SNR_{out}$. Therefore, regardless of the gain, NF equals to the unity. However, in real systems the inner noise degrades the SNR, yielding NF>1. According to Fig. 1, NF for circuits working in voltage-mode becomes [7]:

$$NF = \frac{V_{n,out}^2}{A_v^2 N_{RS}} \tag{2}$$

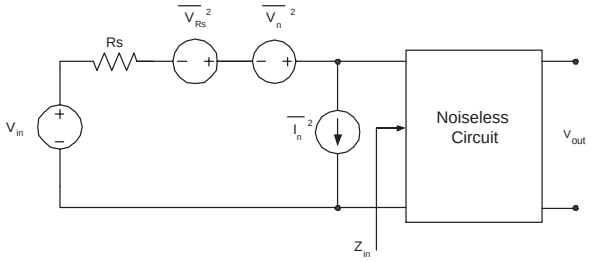

Figure 1: Circuit representation to compute NF

For current-mode circuits NF becomes:

$$NF = \frac{I_{n,out}^2}{A_i^2 N_{RS}} \tag{3}$$

where $V^2_{n,out}$ = voltage of the total output-noise, $I^2_{n,out}$ = current of the total output-noise, A_v = voltage gain, A_i = current gain, and N_{RS} = noise of the resistance of a source.

3. TRANSISTOR NOISE SOURCES

The three most important types of noise in analog circuits are the shot, thermal and flicker noise [1, 2].

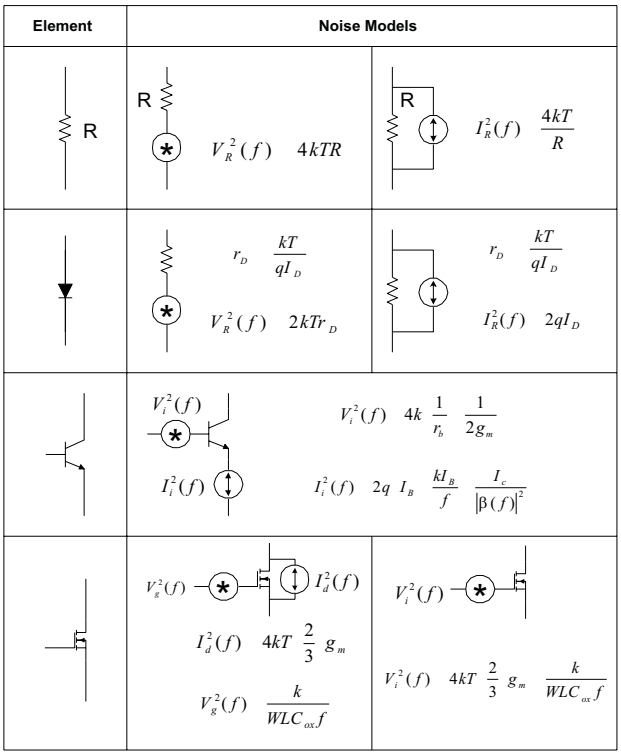

Figure 2: Circuit elements and its noise circuit models

Hspice Models	Flicker Noise	Thermal Noise
NLEV = 0	$S_{ID} = \frac{K_F I_{IDS}^{AF}}{C_{ox} L_{eff}^2 f}$	$S_{channel} = \frac{8kTg_m}{3}$
NLEV = 1	$S_{ID} = \frac{K_F I_{IDS}^{AF}}{C_{ox} W_{eff} L_{eff} f}$	(Also for NLEV = 2)
NLEV = 2,3	$S_{ID} = \frac{K_F g_m^2}{C_{ox} W_{eff} L_{eff} f^{AF}}$	$S_{channel} = \frac{8kT}{3} B(v_{gs} - v_{TH}) \frac{1+a+a^2}{1+a} GDSNOI$ $a = 1 - \frac{v_{ds}}{v_{dsat}}$ Lineal $a = 0$ Saturacion
BSIM3v3	Manual BSIM3v3 Chapter 8, http://www.device.eecs.berkeley.edu/~bsim3/get.html	

Figure 3: Noise models implemented in HSPICE

In HSPICE a MOST is modeled with four noise current-generators [8, 9]. Two of these represent the thermal noise associated with the parasitic drain and source series resistances. The other two are modeled as current sources from drain to source. One of them represents white shot noise and the other flicker noise. All these noise sources are characterized in the saturation region by their PSD. However, in MOSTs the shot noise is very small. The flicker noise is present in all active devices and in some passive elements. Besides we are interested in compute NF of a MOST, the noise models for resistors, junction diodes, BJTs and MOSTs are shown in Fig. 2. Fig. 3 shows the models implemented in HSPICE according to the level of simulation and technology dependence. The proposed noise-models of the MOST as a three and four terminals device are shown in Fig. 4 and Fig. 5.

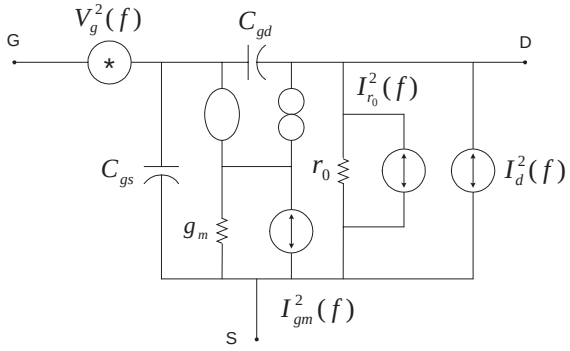

Figure 4: Noise model of a MOST with three terminals

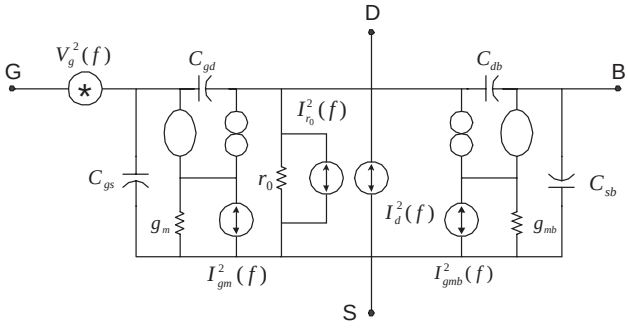

Figure 5: Noise model of a MOST with four terminals

4. COMPUTING THE NF

The first step of the proposed technique is the formulation of a data-structure from a net-list in an HSPICE format. Second, the program transforms the file *.cir into a nullor-based circuit, where the noise sources associated to a MOST are added according to either Fig. 4 or Fig. 5. Third, the

program computes the small-signal circuit equivalent from which the formulation of equation (4) is done.

$$i = Y_{NA} v \tag{4}$$

where i=vector of independent current sources, Y_{NA}=linear admittance matrix, and v=node voltage-variables.

Using the nullor properties[5, 6], equation (4) is reduced in one order for each nullor, leading to equation (5), from which the solution of $V^2_{n,out}$, $I^2_{n,out}$, A_v, and A_i can be computed by handling Ohm's law, in order to satisfy (2) and (3).

$$i = Y_{PNA} v \tag{5}$$

The proposed technique can be summarized as shown by the f lowchart depicted in Fig. 6.

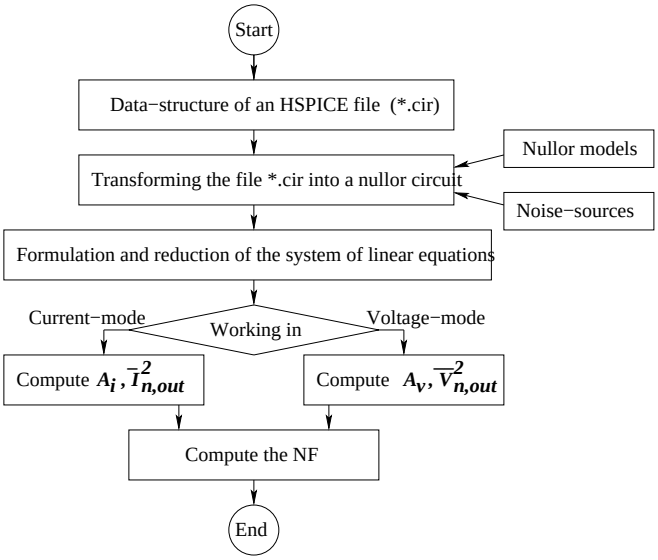

Figure 6: Flow-chart of the proposed method

5. EXAMPLES

In order to demonstrate the suitability of the proposed technique, two illustrative examples have been selected.

5.1. The cascode current mirror

The f irst example is a cascode current mirror, which is shown in Fig. 7. Its corresponding nullor circuit equivalent is shown in Fig. 8. The NF of this circuit, computed by using the proposed method is given by equation (6). A numerical comparison between equation (6) and HSPICE is shown in Fig. 9.

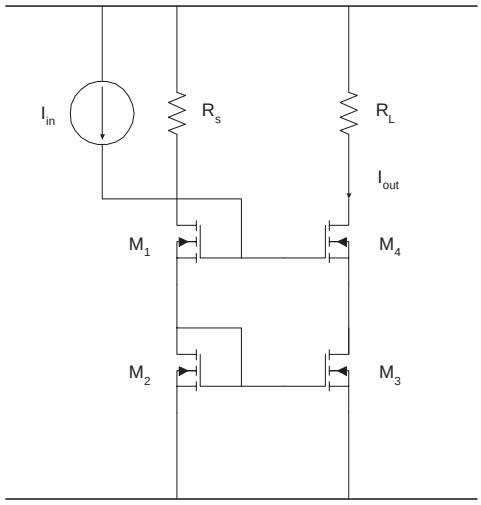

Figure 7: Cascode current mirror

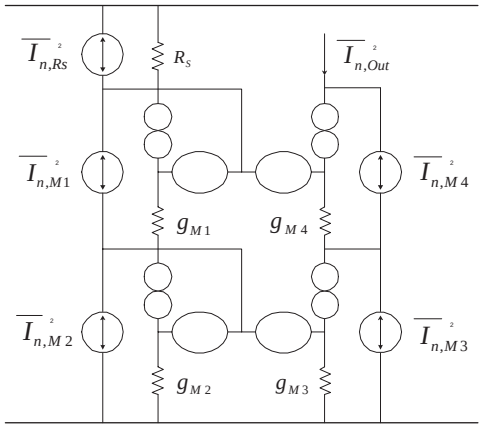

Figure 8: Nullor circuit equivalent of Fig. 7.

$$\begin{aligned} NF = 1 &+ \tfrac{2}{3}\tfrac{g_{m2}}{R_s g_{m1}^2} + \tfrac{1}{4}\tfrac{K_F I_{D2}^{AF}}{R_s g_{m1}^2 kTC_{ox} L_{eff}^2 f} + \\ &\tfrac{2}{3} R_s g_{m2} + \tfrac{1}{4}\tfrac{R_s K_F I_{D2}^{AF}}{kTC_{ox} L_{eff}^2 f} + \tfrac{R_s g_{m2}^2}{g_{m3}^2 R_L} + \tfrac{2}{3}\tfrac{R_s g_{m2}^2}{g_{m3}} \\ &+ \tfrac{1}{4}\tfrac{R_s g_{m2}^2 K_F I_{D3}^{AF}}{g_{m3}^2 kTC_{ox} L_{eff}^2 f} + \tfrac{g_{m2}^2}{R_s g_{m1}^2 g_{m3}^2 R_L} + \\ &\tfrac{1}{4}\tfrac{g_{m2}^2 K_F I_{D3}^{AF}}{R_s g_{m1}^2 g_{m3}^2 kTC_{ox} L_{eff}^2 f} + \tfrac{1}{R_s g_{m3}^2 R_L} + \tfrac{2}{3}\tfrac{1}{R_s g_{m3}} \\ &+ \tfrac{1}{4}\tfrac{K_F I_{D3}^{AF}}{R_s g_{m3}^2 kTC_{ox} L_{eff}^2 f} + \tfrac{2}{3}\tfrac{1}{R_s g_{m1}} \\ &+ \tfrac{1}{4}\tfrac{K_F I_{D1}^{AF}}{R_s g_{m1}^2 kTC_{ox} L_{eff}^2 f} + \tfrac{2}{3}\tfrac{g_{m2}^2}{R_s g_{m1}^2 g_{m3}} \end{aligned} \tag{6}$$

5.2. A feedback amplif ier

The second example is a feedback amplif ier, which is shown in Fig. 10. Basically, the circuit consist of a common-source amplif ier which uses an active device as a feedback element. Its nullor circuit equivalent is shown in Fig. 11. The

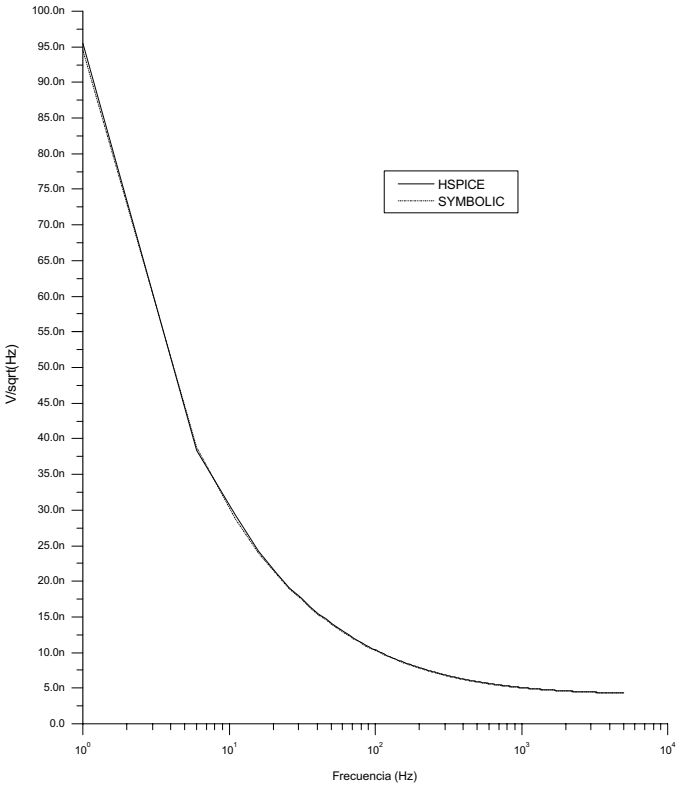

Figure 9: Numerical comparison using the proposed method and HSPICE, for the cascode current mirror.

NF of this circuit, computed by using the proposed method is given by equation (7). A numerical comparison between equation (7) and HSPICE is shown in Fig. 12.

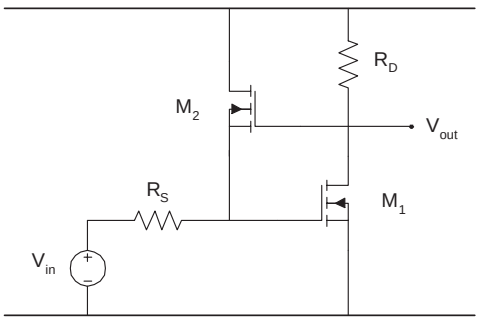

Figure 10: Feedback amplif ier.

$$NF = 1 + \frac{R_s g_{m2}^2}{g_{m1}^2 R_D} + \frac{2}{3}\frac{R_s g_{m2}^2}{g_{m1}} + \frac{1}{4}\frac{R_s g_{m2}^2 K_F I_{D1}^{AF}}{g_{m1}^2 kTC_{ox} L_{eff}^2 f} + \frac{1}{R_s g_{m1}^2 R_D} + \frac{2}{3}\frac{1}{R_s g_{m1}} + \frac{1}{4}\frac{K_F I_{D1}^{AF}}{R_s g_{m1}^2 kTC_{ox} L_{eff}^2 f} + \frac{2}{3} R_s g_{m2} + \frac{1}{4}\frac{R_s K_F I_{D2}^{AF}}{kTC_{ox} L_{eff}^2 f} \quad (7)$$

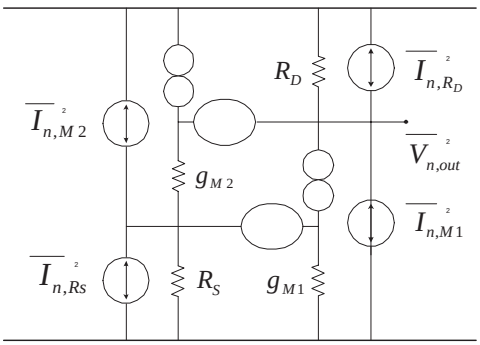

Figure 11: Nullor circuit equivalent of Fig. 11.

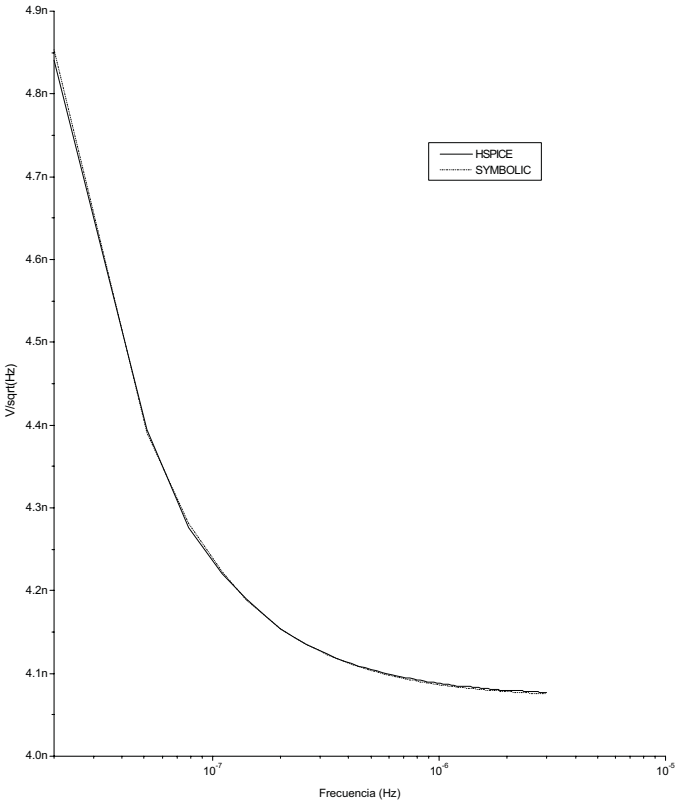

Figure 12: Numerical comparison using the proposed method and HSPICE, for the feedback amplif ier.

5.3. Noise Analysis in Translinear Circuits

For MOSTs biased in weak-inversion, as the example given in Fig. 13 [10], the NF can also be computed with the proposed method. The resulting NF of the normalized gaussian function is given in Fig. 14

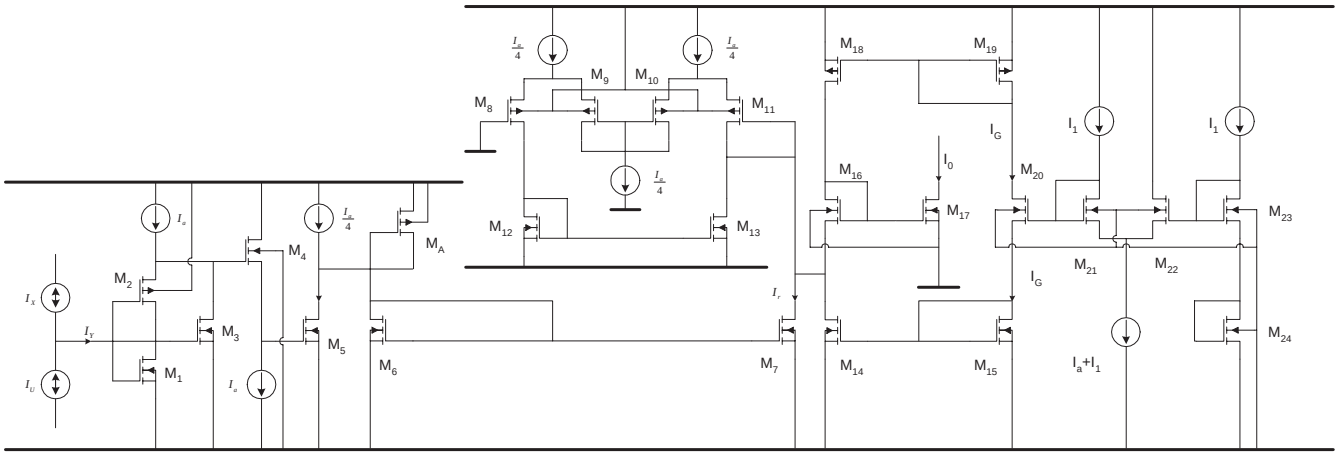

Figure 13: CMOS normalized gaussian-function 13.

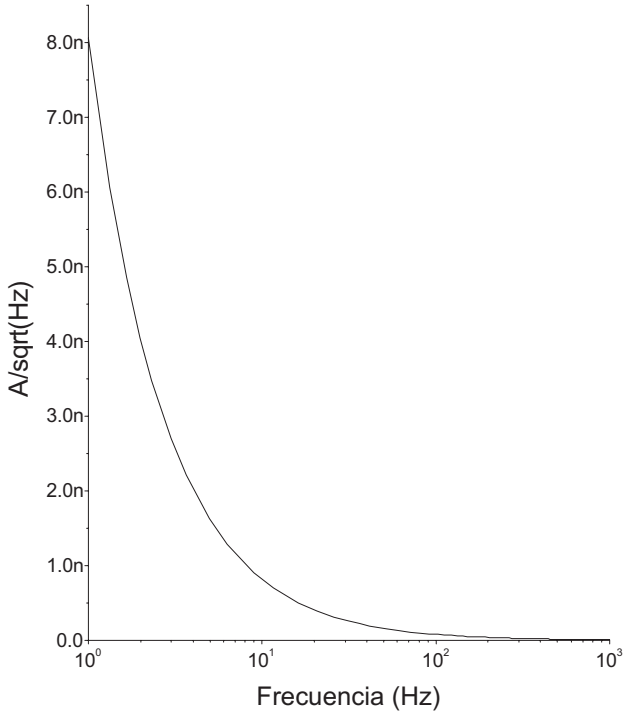

Figure 14: Nullor circuit equivalent of Fig. 11.

6. CONCLUSION

A novel method focused on the symbolic computation of NF for MOST circuits has been described. The method uses the features of the PNA technique by modeling all analog circuits using the nullor element, in order to avoid the use of stamps. The proposed technique has been implemented using MAPLE^{TM}. A comparison between the simulation results using HSPICE and the proposed method, lead us to conclude on the suitability of the proposed technique.

7. REFERENCES

[1] A. Van Der-Ziel, *Noise, Characterization, Measurement*, Prentice-Hall 1970.

[2] C. D. Motchenbacher and J. A. Connelly, *Low-Noise Electronic System Design*, John Wiley Inc., 1994.

[3] L.O. Chua, P.M. Lin, *Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques*, Englewood Cliffs, NJ, Prentice-Hall, 1975.

[4] P.R. Gray and R.G. Meyer, *Analysis and Design of Analog Integrated Circuits*, New York, Wiley, 1984.

[5] B.D.H. Tellegen, *La recherche pour una série complète d'éléments de circuit ideaux non-lineáires*, Rend. del Seminario Matematico e Fisico di Milano, 1954, 25, pp. 134-144.

[6] H.J.Carlin, *Singular network elements*, IEEE TCAS-11, pp. 67-72, 1964.

[7] Tlelo-Cuautle E., Cid-Monjaráz Jaime, *Computing symbolic transfer functions from SPICE files using nullors*, Advances in Systems Theory, Mathematical Methods and Applications, A series of reference books, pp. 74-79, ISBN: 960-8052-61-0, WSEAS PRESS, 2002.

[8] Behzad Razavi, *RF Microelectronics*, Prentice-Hall, 1998.

[9] W. Liu et al, *BSIM3v3 Manual*, Dep. Elec. Eng. Comp. Sciences, Univ. California, Berkeley, 1999.

[10] Carlos Sánchez-López, Alejandro Diaz-Sánchez, Esteban Tlelo-Cuautle, *Generating gaussian functions using low-voltage MOS-Translinear circuits*, WSEAS Transactions on Systems, Issue 2, vol. 1, April 2002. ISSN 1109-2777.