A 1.35 GHz CMOS WIDEBAND FREQUENCY SYNTHESIZER

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Abstract: - The design and simulation of a 1.35 GHz fully integrated CMOS frequency synthesizer for a double band receiver is presented. The proposed synthesizer is based in a wide-band PLL topology with a high reference frequency. This approach allows obtaining low phase noise, fast switching time, a low divider ratio and a reduction in the total chip area. Besides, the use of a novel charge-pump circuit with partial positive feedback and current reuse allows a further reduction in both chip area and power consumption, making the proposed structure suitable for high frequency and low-voltage phase-locked loops.

Key-Words: - Frequency synthesizers, ring oscillators, mixed-mode circuits, wireless integrated circuits.

1. Introduction

Phase noise, silicon area and switching-time are the most important parameters for an integrated frequency synthesizer. When a PLL is utilized, all these parameters can simultaneously be satisfied increasing both the loop bandwidth and the reference frequency. Unfortunately, for integer-N architectures this can not be realized because the reference frequency must be equal to the channel bandwidth [1]. Furthermore, for stability reasons, the loop bandwidth must be selected equal to one tenth or less of the reference frequency. Fractional-N architectures allow to overcome those limitations, by changing the division ratio, achieving a larger loop bandwidth and alleviating the requirements for the voltage-controlled oscillator (VCO). However, the fractional division generates spurious tones at the output of the frequency synthesizer, leading to complicated compensation schemes like sigma-delta or dithering modulation. Recently, dual-loop topologies have taken advantage of large bandwidth and high reference frequency, achieving low-phase noise and relatively reduced area. However, any of the previous approaches have completely exploited the potential of these features, wasting the possibility of producing a good quality output signal, although a low Q voltage controlled oscillator be utilized, a set of very attractive features when a complete integration in low cost, standard CMOS process is pursued.

This paper is focused on the design and simulation of a 1.35 GHz CMOS quadrature oscillator for the 900 MHz & 1.8 GHz bands. The proposed synthesizer is based in a wideband PLL topology with a high reference frequency, resulting in a low phase noise output, although a noisier VCO is used. Furthermore, fast switching time, a low modulus divider and low power consumption are satisfied by using this approach. Additionally, the use of a novel charge-pump topology with positive feedback and current reuse, allows a further reduction both in chip area and power consumption.

2. The Double Band CMOS Receiver

Multi-standard and different operation band capabilities, are some of the technological trends pursued in modern integrated receivers. That has been motivated by two primordial factors: the availability of new frequency bands beyond the 1.8 GHz range, and the proliferation of new wireless standards like GSM or CDMA. Both factors have allowed a higher flexibility and a noticeable increasing in the overall capacity for mobile communication systems. However, in order to satisfy those features, it is necessary to apply a very efficient frequency planning and choose carefully the blocks that can be reused, allowing a reduction in both the total chip area and the off-chip components. This last has leading to the development of new transceiver architectures or in some cases, the return to old systems whose integration in CMOS technologies can be realized now. Following the described trends, the frequency synthesizer is designed for the dual band system shown in figure 1. It corresponds to a Weaver modified architecture [2], which avoids the need of an image reject band filter, a desirable feature for monolithic integration. In this work, the oscillator is located in the middle of the two desired bands (1.35 GHz for the 900 MHz and 1.8 GHz bands). Additionally, the synthesizer has quadrature outputs with low phase imbalance, in order to achieve a good image rejection ratio for the whole system.

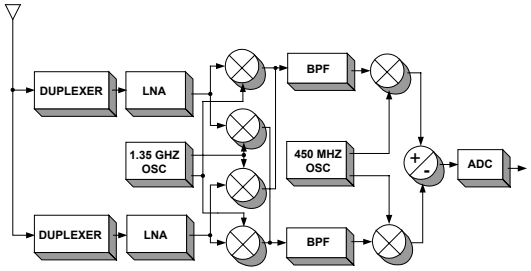

Figure 1. A dual-band CMOS receiver.

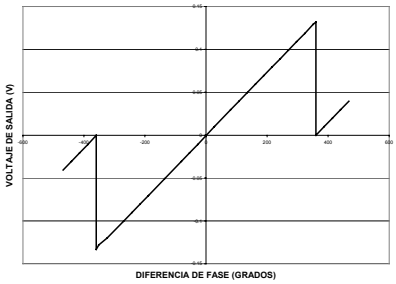

Figure 4. PFD phase-voltage characteristic.

3. Basic Building Blocks

Figure 2 shows the proposed synthesizer. It is based in an integer-N architecture, with a reference frequency of 75 MHz and a 3.5 MHz loop bandwidth. The output frequency of the synthesizer can be expressed as:

$$f_O = N * f_{REF} \quad (1)$$

where: N is the divider ratio. With this reference frequency, the modulus divider ratio is simplified to 18, reducing both noise, area and power contributions from this block.

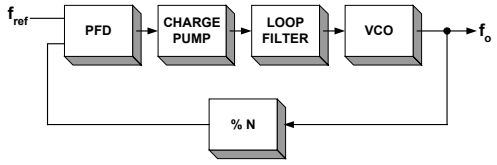

Figure 2. Integer Frequency synthesizer architecture.

3.1 Phase Frequency Detector (PFD)

The utilized phase frequency detector is shown in figure 3. It consists in two type D-FLIP FLOPS and an AND gate. A delay element is introduced to eliminate the dead zone problem in the phase-voltage PFD transfer characteristic. However, if this delay is quite large, the level of the output spurs is increased, and thus leading to a tradeoff between dead-zone and spurs level. The PFD was designed in static CMOS logic. The transfer characteristic for the designed PFD is shown in figure 4. From this, it can be seen that no dead zone problem is generated.

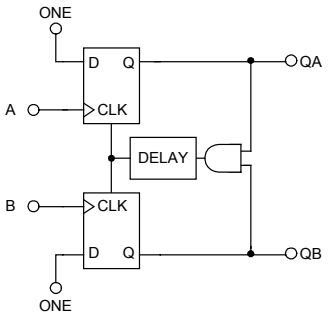

Figure 3. PFD without dead zone..

3.2 The Positive Feedback and Current Reuse Charge-Pump.

A charge pump is composed by two switched current sources driving a capacitor. This circuit is used to convert the output signal of the PFD into a control voltage for the LO. In recent works, some current-steering topologies have been proposed in order to provide fast switching time and low charge-injection errors[3,4]. However, these topologies present several drawbacks, like a static current consumption, which penalize the total power consumption of the structure. In order to solve that issue, a novel charge-pump topology is proposed. Shown in figure 5, the proposed circuit makes use of positive feedback for increase the switching speed and current reuse for reduce the power consumption. By using two basic cells, the complete structure results highly robust and symmetrical. Besides to eliminate the static power consumption and provide a faster switching speed, the chip area remains almost the same, since we have only moved the position of one current source, as shown in figure 6. A fully description of this topology can be found in [5].

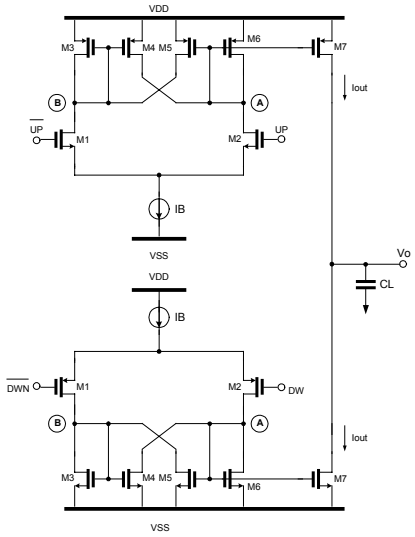

Figure 5. The proposed partial positive feedback and current reuse charge pump circuit.

The amount of positive feedback is given by:

$$\alpha = (W/L)_5/(W/L)_6 \quad (2)$$

The switching speed of the circuit depends of the parasitic capacitance associated to node A and the current source IB. The capacitance on node A is given by:

$$C_A \approx Cgs_3 + Cgs_4 + Cgs_7 + Cdb_2 + Cdb_5 + Cdb_7 \quad (3)$$

From equation (2), it can be deducted that the maximum value for α must be 1 or the circuit becomes a latch. A practical value for this is 0.75. The switching point of the input differential amplifier is given by:

$$V_{SW} = \sqrt{2}(V_{GS1} - V_{T1}) = \sqrt{2}V_{DSAT1} = \sqrt{\frac{4IB}{Kn(W/L)_1}} \quad (4)$$

In this way, a trade-off between switching point and capacitance must be realized. Furthermore, for low-voltage operation VDD must satisfy:

$$V_{DD} \geq V_{GS3} + V_{DSAT2} + V_{DSATIB} \quad (5)$$

An important issue in the design of charge-pump circuits, is the current imbalance due to both current and time mismatch, which produces single sidebands at the synthesizer output. To solve this, differential charge pump inputs are driven by a Shoji's delay balanced chain. Composed of two delay lines with two and three inverters respectively, this circuit minimizes the time imbalance mismatch

3.3 Loop Filter

The utilized loop filter is composed of a second order passive integrator with phase lag (fig.7). Although increasing the order allows a better filtering and lower component values, in this case this is not necessary because they are intrinsically reduced by the wide PLL bandwidth. Thus, the total chip area is drastically reduced, making feasible its complete integration.

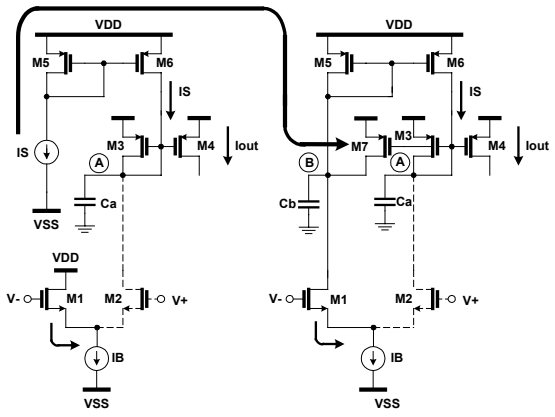

Figure 6. An interpretation of the proposed technique.

The component values for the loop filter are summarized in table 1.

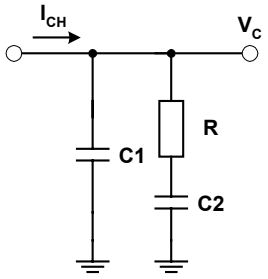

Figure 7. Second order passive loop filter.

Table 1. Loop filter element values.

ELEMENT	VALUE
R1	30.5 KΩ
C1	3.9 pF
C2	0.3 pF

3.4 Frequency Divider

The design of the frequency divider entails different issues in order to obtain satisfactory results. Low power consumption, high operation frequency and low switching noise, are the main features that must be satisfied for this block. Therefore the correct selection for a logic style results cleaver. SCL logic combined with an adequate design methodology allows to satisfy all this parameters. The frequency divider is composed of a divide by two circuit followed by two divide by three circuits, giving the desired modulus. The basic cell for each divider is the SCL latch circuit shown in figure 8. The bias current for each cell is given by:

$$IB = n\Delta V f_{CLK} C_L \quad (7)$$

where ΔV is the output swing voltage, f_{CLK} is the operation frequency and C_L the load capacitance.

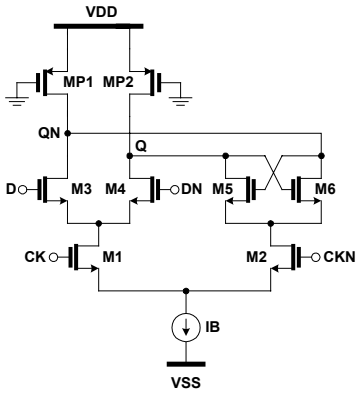

Figure 8. Basic SCL latch circuit.

The transistor sizing is determined by:

$$(W/L)_n = \frac{2mIB}{KnV_{DSATn}{}^2} \quad (8)$$

$$(W/L)_P = \frac{1}{R_L K_P (V_{BIAS} - V_{TP})} \quad (9)$$

where m is a correction factor which takes into account the layout capacitance, and R_L is the load resistance. It is interesting to note that following the described approach, the theoretical results are in good agreement with the simulation results.

3.5 Voltage Controlled Oscillator

The VCO is a four stages fully integrated ring oscillator, which generates inherently good quadrature outputs, besides the possibility of incorporate a phase imbalance correction circuitry. The core for each stage is the Maneatis cell [6], which provides good power supply rejection, linear tuning range and moderate phase noise. With a total power consumption of 25 mW, a phase noise of –100 dbc/Hz at 600 KHz offset from the 1.35 GHz carrier was obtained through simulations.

4. Simulation Results

The proposed wideband synthesizer was simulated in H-SPICE, with AMS 0.35 μm CMOS parameters. Figure 9, shows the simulated VCO control voltage for the worst case. From this figure, it can be seen that the locking time is 6 μs, which is significantly lesser than the time slot for GSM and DCS-1800 systems. A smaller overshoot can be obtained by increasing the phase margin of the loop, at expenses of a large locking. Finally, figure 10 shows the simulated phase noise, which is –112 dbc/Hz @ 600 KHz frequency offset.

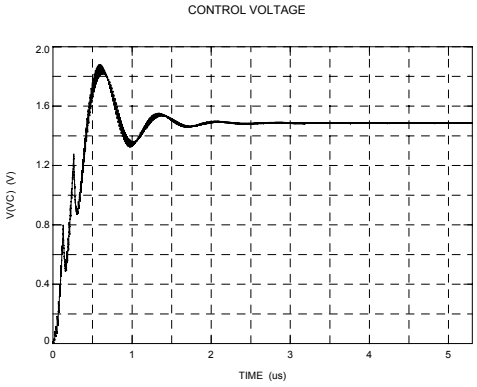

Figure 10. Transient response of the synthesizer.

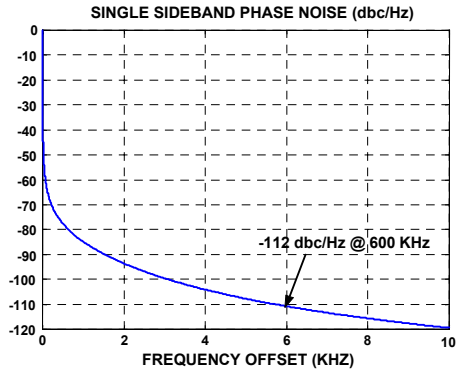

Figure 10. Phase noise for the synthesizer.

5. Conclusions

A 1.35 GHz, wideband CMOS frequency synthesizer for a dual band receiver is presented. With a reference frequency of 75 MHz and a loop bandwidth of 3.5 MHz, the proposed topology reduces the output noise by a significantly amount, taking advantage of these important features and thus been fully compatible with standard CMOS technologies. Besides, the use of a novel charge pump topology with partial positive feedback and current reuse allows to reach a higher switching speed and a lower power consumption, outperforming previously reported structures.

Acknowledgements

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