A Second Generation Low-Voltage Current Conveyor

Juan Lopez-Hernandez, Jose Alejandro Diaz-Mendez and Alejandro Diaz-Sanchez
Integrated Circuits Design Group
Instituto Nacional de Astrofísica Óptica y Electrónica
Luis Enrique Erro #1, Sta. Ma. Tonantzintla, Puebla
MÉXICO
jlopezh@susu.inaoep.mx, ajdiaz@inaoep.mx, adiaszsan@inaoep.mx

Abstract: - A Low-Voltage/Low-Power rail-to-rail Second Generation Current Conveyor is presented. The CCII is implemented using two techniques: MOS Transistors in weak inversion, which allows the use of small I_b, and Floating Gates, to obtain an extended dynamic range. The concept of Partial Positive Feedback is used for implementing the required OTA.

Keywords. - Current mode, Floating gates, Translinear circuits, Positive feedback.

1. Introduction

Low-power low-voltage integrated circuits are of great interest for many applications that use batteries as power supply. Because the need of digital systems to operate below 1.5V, mixed-mode designers have implemented many solutions to obtain good performance in the analog section. Several techniques have been reported recently [1], which can be used to solve the problem. In the present work, two analog low-voltage techniques have been used: MOS-translinear topologies in weak inversion, and floating gates structures.

MOS-translinear is a technique, which allows designing circuits capable of good performance with lower power supplies. The mayor advantage of that technique is the maximum transconductance obtained by MOS transistors operating in weak inversion. Moreover, since they are operating in the subthreshold region, they require lower voltages for biasing. Thus, reduced supply voltages can be used. One of the problems presented by MOS transistors in the subthreshold region is the low speed achieved from systems, mainly due to the low drain-currents used in those applications.

Floating Gates (FG) is another novel technique, which allows us to set the operating point of transistors as a sum of a set of input voltages. By using this technique, we only need to bias one or more of the floating gates at the transistor gate, level to set the transistor in the wished region. Since the voltage at the input is weighted by the floating capacitor size, a small V_{th} can be obtained by applying this technique.

In the present work both described techniques are used to implement a full CMOS rail-to-rail second generation current conveyor (CCII). In the second section, a brief review of the basic concepts of current conveyors is depicted. Section three describes the design of the rail-to-rail current conveyors using MOS-translinear circuits and some simulated results. Finally, the conclusions of the present work are discussed in section 4.

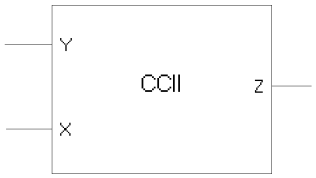

Figure 1. CCII as a black box.

2 Rail to Rail CCII

A CCII is a device that can be see as a black box, as is shown in Figure 1. Which should fulfill the following input/output characteristics:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \qquad (2.1)$$

It can be seen from equation 2.1, that the CCII should have very high impedance in the terminal Y, very low impedance in the terminal X, and make a copy of the current that passes from the X-terminal to the Z-terminal. In low-voltage circuits, those requirements are not easy to obtain. Despite circuit-source levels can be lowered notably, noise levels remain in the same range.

For that reason, the voltage follower at terminals X and Y must have a rail-to-rail operation range.
Since obtaining low impedance at X-terminal is the most difficult requirement in the design, in many applications the value of this impedance is of a small but finite value. In what concerns to obtain the replies of currents at terminals X and Z, it is not a problem, and it is only necessary to obtain a good isolation of this currents.

3 Rail to Rail CCII

The structure of the analyzed CCII is presented in figure 2 [2]. So far, a technique that has taken relevance in the design of low-voltage circuits has been operating the MOSFET in the weak inversion region. The advantage of this technique is that it allows carrying out designs with very low voltage levels. This is due to transistor only requires voltage, slightly lower than V_{th}, since all the transistors hardly have formed the conduction channel [1].

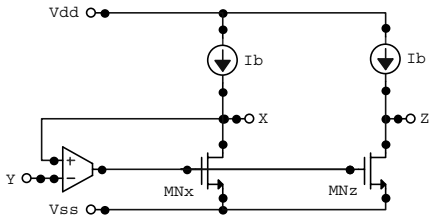

Figure 2. Proposed CCII.

The OTA used to implement the current conveyor is based on this technique. In addition, the use of the Partial Positive Feedback (PPF) is introduced to increase the DC gain of the OTA. This concept is thoroughly treated in [3]. Figure 3 shows the schematic diagram of the OTA. Transistors MNx and MNz were chosen to drive up to 10 µA. The circuit was designed to operate with ±0.6 V. Simulated results are shown in Figures 4-7.

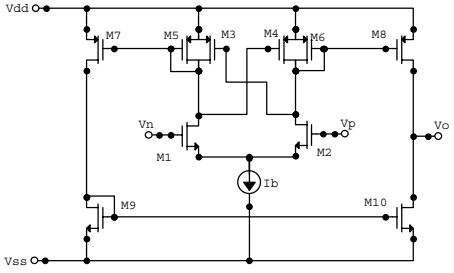

Figure 3. OTA with PPF.

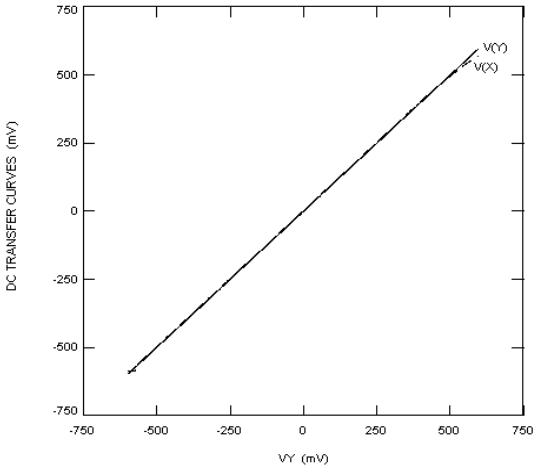

Figure 4. V_y-V_x Response with ±0.6 V (DC).

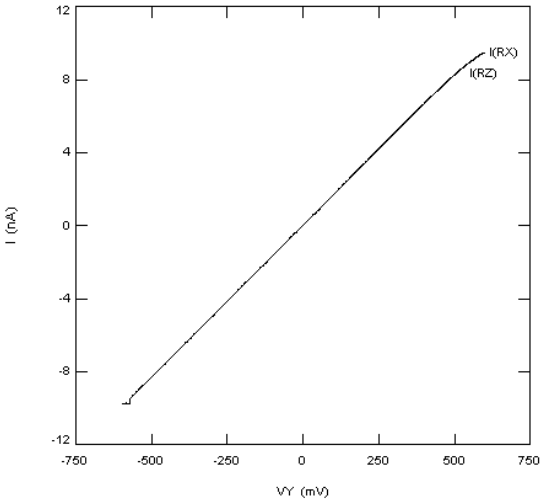

Figure 5. I_x-I_z response with ±0.6 V (DC).

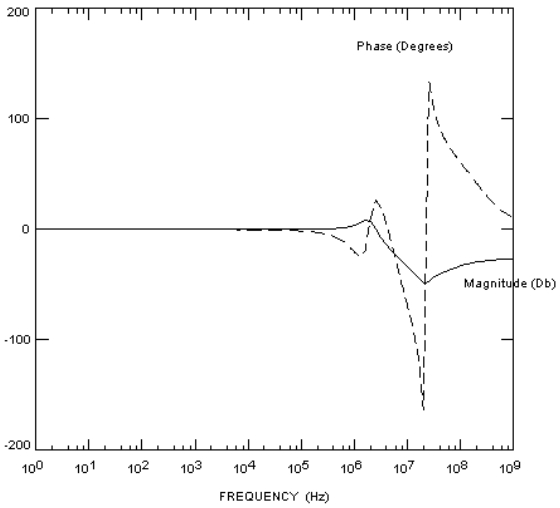

Figure 6. V_x/V_y response with ±0.6 V (AC).

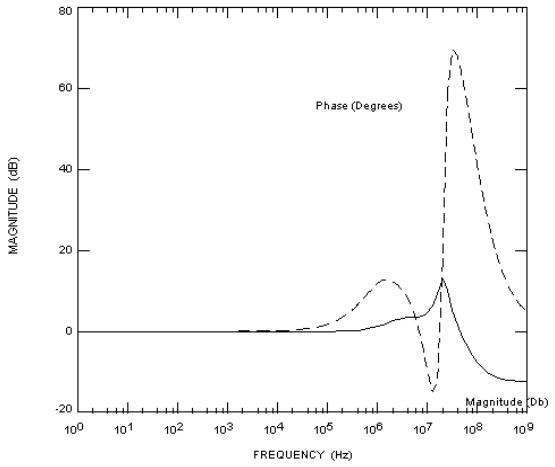

Figure 7. I_z/I_x response with ±0.6 V (AC).

3.1 CCII modified using FG

The necessity to operate the circuits with even lower voltage levels than those previously shown, has motivated the development of several techniques, such as the use of floating-gate (FG) structures. There are several ways of taking advantage of the FG. One of them is to reduce the V_{th} of the transistor or to predetermine the point of operation of the same one. In figure 8, FG is used to diminishing the differential pair's V_{th}, and lowers the bias requirements of the input to create the drain-source channel.

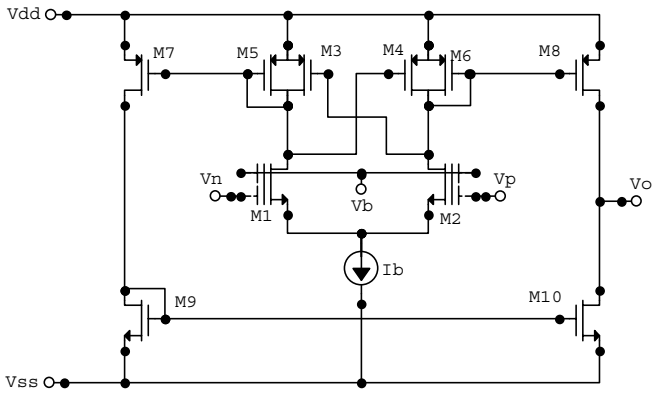

Figure 8. OTA with Floating Gates.

It can be seen how only one of the gates should be polarized in the differential pair's transistors to obtain the wanted results. The simulation results obtained with those modifications are shown in figures 9-12 for supply voltages of ± 0.6V, while figures 13 and 14 show the DC response using supply voltages of ±0.35 V.

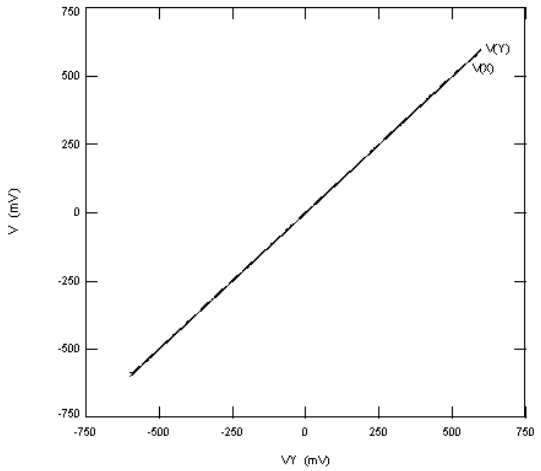

Figure 9. V_y-V_x response with ±0.6 V and FG (DC).

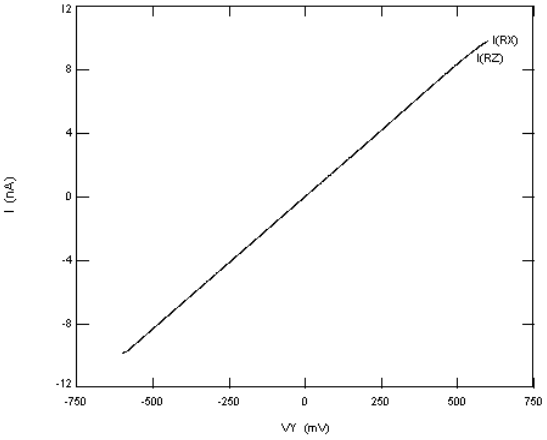

Figure 10. I_x-I_z response with ±0.6 V and FG (DC).

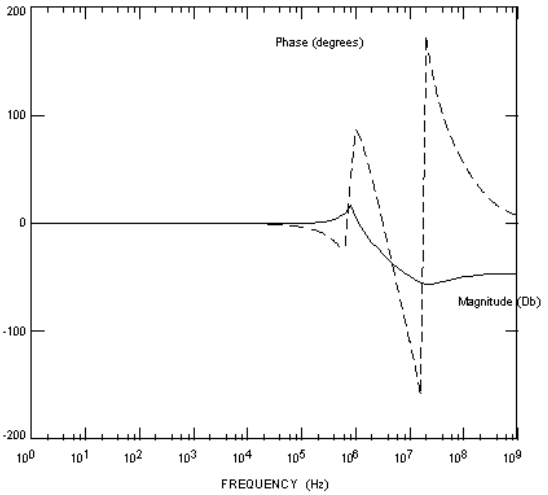

Figure 11. V_x/V_y response with ±0.6 V and FG (AC).

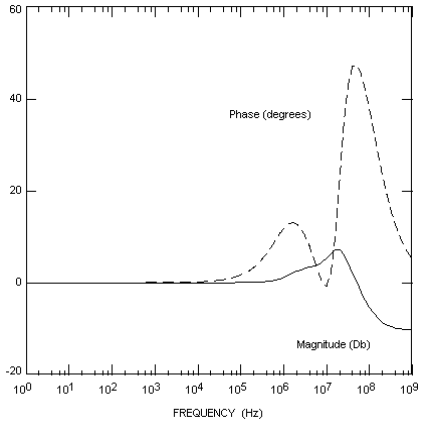

Figure 12. I_z/I_x response with ±0.6 V and FG (AC).

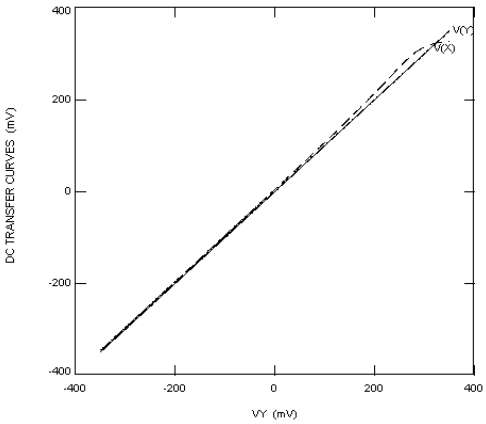

Figure 13. V_y-V_x response with ±0.35 V and FG (DC).

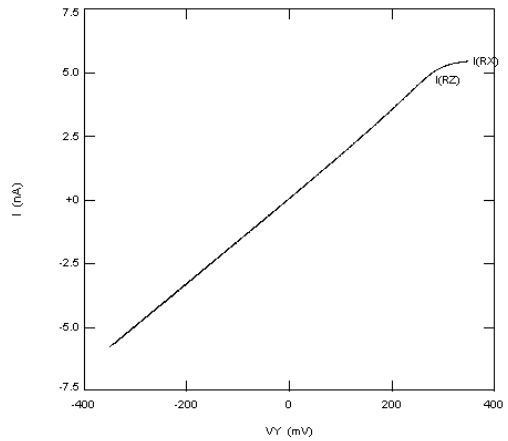

Figure 14. I_x-I_z response with ±0.35 V an FG (DC).

Table1) Sizes using translinear circuits

CCII in Sub-Umbral, I_{bias}=5.6µA	
Transistor	W/L (µm)
M1-M2 (OTA)	12/4.8
M3-M4 (OTA)	7.68/9.6
M5-M10 (OTA)	9.6/9.6
MNx-MNz	76.8/4.8

Table 2) Sizes using floating gates

CCII in Sub-Umbral con FG, I_{bias}=5.6µA	
Transistor	W/L (µm)
M1-M2 (OTA)	12/4.8
M3-M4 (OTA)	7.68/9.6
M5-M10 (OTA)	9.6/9.6
MNx-MNz	76.8/4.8
Capacitores para Floating Gates (Farads)	
C1	40f
C2	88f

4 Conclusions

The design of a low-voltage CCII, using MOS-translinear circuits and floating gate structures, was presented. The use of the MOS-translinear technique allowed improving the performance of the circuit and obtaining a rail-to-rail operation. The voltage and current follower behavior were as expected for a supply voltage of ±0.6 V and a bandwidth of 100 KHz. The circuit was also operated with a source of ±0.35 V. Using the floating-gate structures, an improve bandwidth in the current copiers was observed, but the obtained decreased. The obtained resistance in the X-terminal is of some hundreds of ohms, but increasing the current capacity, which increases the power consumption, can diminish it, this solution isn't reliable when power consumption is critical. Table 1 and 2 shows the sizes used in the design.

5. References

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