On-Chip ESD Protection Design for Ics

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Abstract: This tutorial paper reviews the state of knowledge of on-chip ESD (electrostatic discharging) protection circuit design for integrated circuits. The discussion covers critical issues in ESD design, such as, ESD test models, ESD failure mechanism, ESD protection structures, ESD device modeling, ESD simulation, ESD layout issues, and ESD influences on circuit functionality, etc. This review serves to provide industrial IC designers with a thorough and heady reference in dealing with ESD protection design.

Key Words: ESD protection, electrostatic discharging, failure analysis, ESD modeling, I/O, HBM, CDM, MM, IEC, TLP.

1 Introduction

One of the most pervasive reliability problems facing the IC industry is ESD (electrostatic discharging) failure. It is reported up to 35% of total IC field failures are ESD induced with an estimated annual cost to the IC industry running to several billion dollars [1, 2]. Dedicated on-chip ESD protection structures are commonly used to protect IC parts from being damaged by ESD stresses [3-5]. Active research on ESD fundamentals and protection has been going on for over two decades. While significant progresses have been made in the field of ESD protection, many important issues remain unresolved, for example, latent ESD failure mechanism, accurate ESD device modeling and predictive ESD CAD design verification, to name a few. Further, as IC technologies continue to advance in a stunning pace, new problems continuously emerge in ESD design for very deep sub-micron (VDSM) IC applications. It is therefore believed that ESD protection design will become a major IC design challenge down the road of semiconductor IC technology advancement [6]. It is hence imperative for IC designers to acquire adequate knowledge on ESD protection design and to maintain at the front page of the new development in the field. This tutorial paper is meant to serve such a critical need among IC designers.

2 ESD Test Models

ESD is an extremely fast discharging phenomenon occurring when two charged objects are brought into proximity and electrostatic charges transfer in between [4]. The resulting high current (up to a few tens of Amps) and high voltage (up to several tens of KV) may damage or degrade IC parts. ESD events can be simulated by different ESD test models categorized by its origins, upon which on-chip ESD protection circuits are tested and rated.

2.1 HBM Model

Human body model (*HBM*) [7, 8] simulates ESD events that occur when a charged human body contacts an electronic device directly. HBM circuit model is shown in *Fig. 1*, where a C (=100pF) is charged up and then discharges through an R (=1500Ω) & L (≈7.5μH) network to the device under test (DUT). *Fig. 2* shows its discharging current waveform. HBM is the current industry standard.

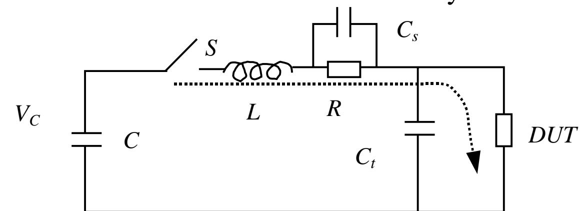

Fig. 1 A HBM ESD model circuit.

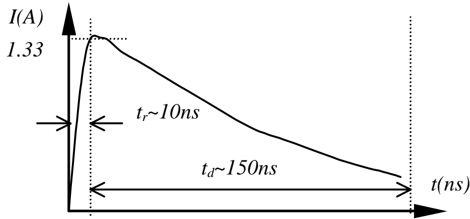

Fig. 2 A typical HBM ESD discharging waveform.

2.2 MM Model

Machine model (*MM*) [9, 10] describes an ESD pulsing event where charged machinery discharges when touching IC parts during testing. MM circuit model is similar to HBM model with different parameters: C=200pF, R=0Ω & L≈2.5µH, leading to an oscillatory discharging waveform (*Fig. 3*) with higher peak current (I_{peak} ~7A) and shorter rise time (t_r~*ns*).

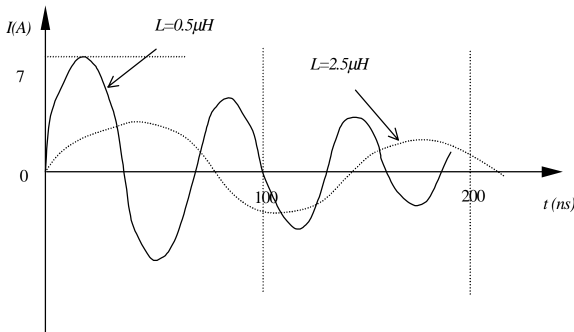

Fig. 3 A typical MM ESD discharging waveform.

2.3 CDM Model

Charged device model (*CDM*) [11-13] simulates self-induced discharging of devices where un-grounded electronic parts are charged up during manufacturing or assembly and then discharge through a ground-pin. *Figs. 4 & 5* show its circuit model and typical discharge waveform, respectively, featuring very short t_r (~1*ns*) and very high I_{peak}.

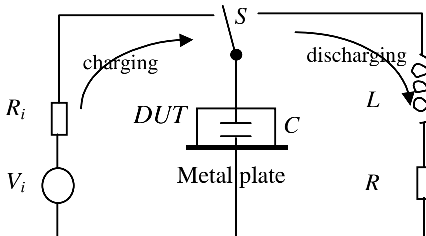

Fig. 4 A CDM ESD model circuit.

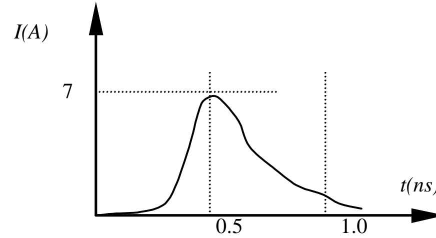

Fig. 5 A typical CDM ESD discharging waveform.

2.4 IEC Model

IEC (International Electrotechnical Commission) model [14] circuit is illustrated in *Fig. 6* with typical current waveform shown in *Fig. 7*, delivering extremely low t_r (≤ 1*ns*) and high I_{peak} due to very low R and zero-L.

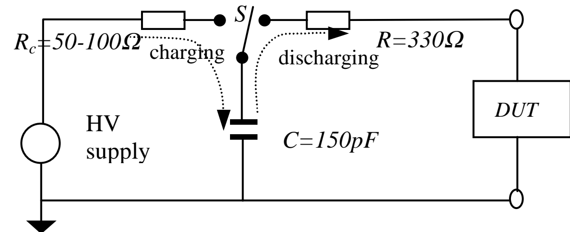

Fig. 6 A typical IEC ESD model circuit.

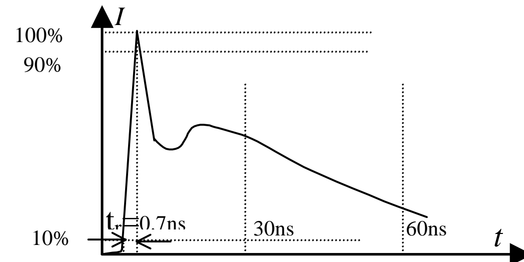

Fig. 7 A typical IEC ESD discharging waveform.

2.5 ESD Zapping

The differences among the above ESD models stem from their circuit parameters as summarized in *Table 1*. ESD protection performance is classified by stressing tests where IC chips are stressed by ESD zapping testers, using the above ESD testing models, step-wisely until damage occurs. All the above ESD test models are *destructive* that provides no insights into the failure mechanisms needed to optimize ESD design performance.

2.6 TLP Model

The *TLP* model (transmission line pulse) [15], unlike the above black-box type models, is *non-destructive*

and can probe instantaneous *I-V* curve of a DUT under ESD stress. TLP model circuit is shown in *Fig. 8* where a transmission line is charged up and then discharges into a DUT to simulate ESD stressing. TLP model is critical to ESD simulation.

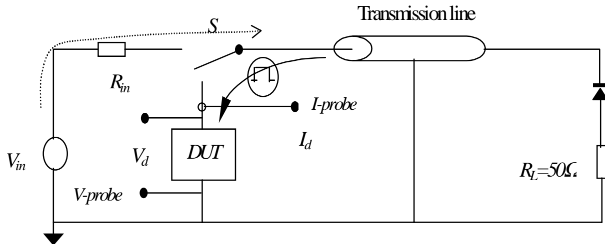

Fig. 8 A typical TLP model circuit.

Table 1 Parametric summary of ESD models

ESD Models	R (Ω)	L (μH)	C (pF)
HBM	1500	7.5	100
MM	0	2.5	200
CDM	0 - 25	0.005 – 0.1	1 - 100
IEC	330	0	150

3 ESD Protection Device Physics

On-chip ESD protection units, being either single devices or sub-circuits, are commonly used to protect IC chips by being placed at each I/O and V_{DD} pins. The principle of ESD protection is twofold: to provide a low-impedance discharging path to shunt ESD currents and to clamp pin-voltage to a safe level to avoid dielectric breakdown. The two typical ESD I-V characteristics, as illustrated in *Fig. 9*, are simple turn-on and I-V snapback, with the latter being more attractive due to its high current handling capacity. A successful ESD protection design must properly define such critical parameters as, triggering point, (V_{t1} & I_{t1}), snapback holding voltage, (V_h, I_h) and thermal breakdown, (V_{t2} & I_{t2}), etc. Typical single ESD protection devices and device physics are discussed as following:

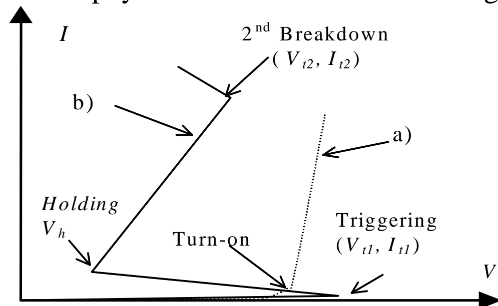

Fig. 9: Typical ESD I~V characteristics: a) simple turn-on; b) snapback.

3.1 Diode ESD device

Diodes, reverse-connected to I/O pins as shown in *Fig. 10*, are widely used in early days as ESD protection solutions. Its operation follows the simple turn-on scheme as depicted in *Fig. 9* (a). Zener diodes are often used in this scheme [4, 5]. This is a simple solution that can be simulated by SPICE. One main disadvantage is the fixed diode forward turn-on voltage that limits its applications in varying-V_{DD} cases. Multiple diode strings (forward or reverse) may address the problem [16-18], however, the on-resistance add-up reduces their current handling capacity.

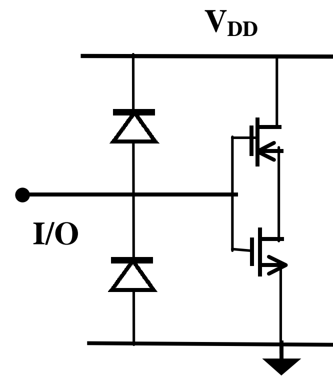

Fig. 10 A typical diode ESD protection scheme.

3.2 NMOS ESD device

Fig. 11 illustrates a well-known ggNMOS (grounded gate) ESD structure where the drain (D) is connected to an I/O pad. When a positive ESD pulse appears at the I/O pin, the D/Body junction is reverse biased until breakdown occurs. The generated hole current flows to Ground via the B (body) terminal that builds up a positive B/S junction voltage since B and S (source) are shortened. It eventually turns on the parasitic lateral NPN transistor, which forms a low-impedance discharging path to shunt the ESD current, therefore protect ICs from being ESD-damaged. For a negative ESD transient, a parasitic diode takes the charge. The advantage of ggNMOS protection is its active protection mechanism that can be optimized via physical design. The main disadvantages include non-SPICE-compatible snapback I~V, relative high holding point, low area efficiency, substantial parasitic effects, and multiple-finger structure susceptible to non-uniform turn-on. An improved version, gCNMOS (gate-coupling), will be discussed in Section 4. A field-oxide NMOS

(FD-NMOS) version, using FOX as the gate [19-22], was also in use in the past.

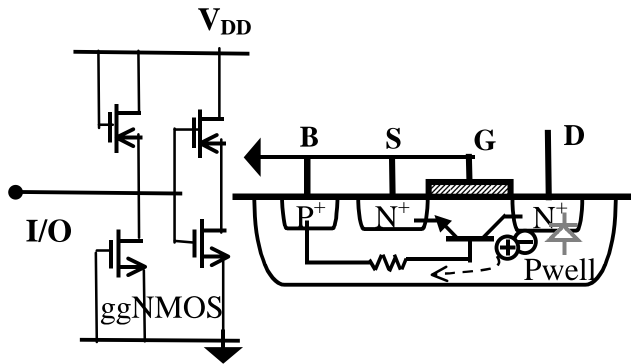

Fig. 11 A ggNMOS ESD protection structure.

3.3 SCR ESD Device

A SCR structure may serve as an excellent ESD protection device due to its deep snapback I~V characteristic [4, 5, 23-25]. *Figs 12 & 13* illustrate a typical SCR cross-section and equivalent circuit. As an ESD pulse appears at the anode (A) *w.r.t* cathode (K), it breaks-down the BC junction of vertical PNN Q1. The hole current flows through parasitic substrate-R, builds up V_{BE} of lateral NPN Q2, turns it on that triggers off the SCR. A low-R active path is then formed to discharge ESD current while its low holding voltage clamps I/O pad to a safe level to avoid any ESD damages. A SCR is a very area-efficient ESD protection structure because of its high current handling capacity. However, cautions are needed to avoid possible latch-up effect. For example, its holding current must be designed higher than others on a chip; proper isolation using double guard rings and placement are critical to avoid early triggering. Another disadvantage of SCR is that it relies on parasitic diode for ESD discharging in the opposite direction, which disqualifies it for many higher voltage mixed-signal ICs.

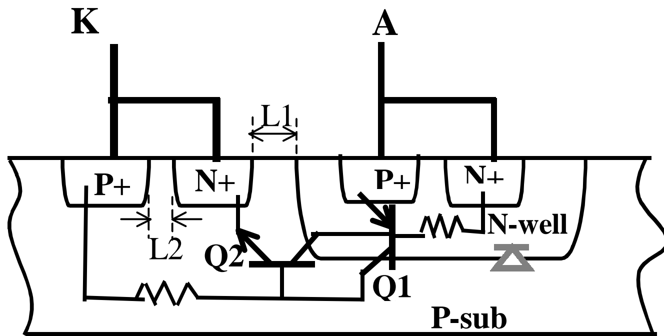

Fig. 12 A X-section of a SCR ESD structure.

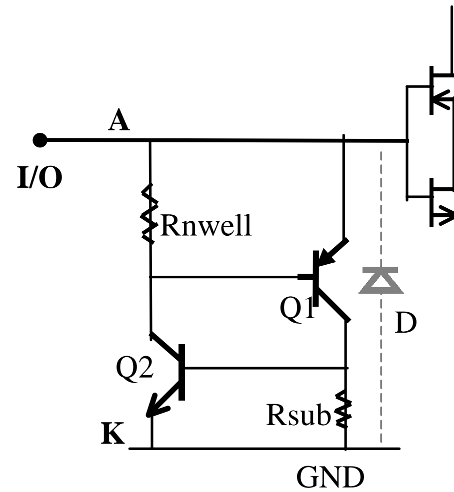

Fig. 13 A schematic for the SCR ESD structure.

4 ESD Protection Circuit Solutions

ESD protection circuits are designed for input, output and power bus based upon their special needs. An ideal ESD structure should feature low-R, low-holding non-destructive path to shunt ESD pulses of all modes, preferably in active device mode for SPICE modeling, as well as negligible leakage in off-state. To achieve full-chip ESD protection, ESD units are placed at all bonding pads and form active paths from each pin to any other pins. Until 1990s, most ESD protection is single-device based. IC technology advancements in recent years made more robust but complex ESD protection networks attractive and possible.

4.1 Input ESD Protection

4.1.1 A Primary-Secondary ESD Solution

A classic primary-secondary ESD protection scheme [4, 5, 26] is illustrated in *Fig. 14* where a primary ESD structure (P_{ESD}) is used to take the brunt of ESD transients; a secondary ESD unit (S_{ESD}) serves to ensure CMOS gate voltage clamping as well as to assist the turn-on of the primary that usually has higher triggering point; and an isolation resistor limits the current to inside circuits. A ggNMOS serves as a good secondary. The primary, which can be realized by a FD-NMOS, SCR, or diode strings [26-28], must be able handle large current, has very low holding voltage and small size. The isolation–R should be large enough to ensure current-limiting without affecting IC speed performance. Low-parasitic poly-Si resistors may be used for low ESD case while diffusion-R with heads in n-well has better thermal behavior for high ESD rating. Better

ESD performance can be achieved by optimizing layout; for example, current uniformity can be realized by rounding corners to avoid localized heating.

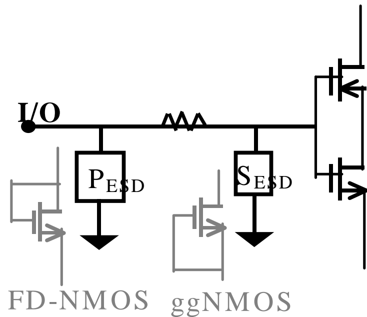

Fig. 14 A classic primary-secondary ESD scheme.

4.1.2 gCNMOS

To achieve robust ESD protection (>2KV HBM), a large size ggNMOS is used in multiple-finger format. However, a linear relationship between ESD performance and the number of NMOS fingers cannot obtained readily because one NMOS finger is usually damaged first due to non-uniform turn-on and current-heat distribution across fingers. This happens if the trigger voltage (V_{t1}) is greater than that of the second breakdown voltage (V_{t2}), referring to *Fig. 9*, where one on-finger takes all ESD current and burns out before any other finger may be turned on. Conceptually, a design of $V_{t1} < V_{t2}$ will resolve the problem, which can be realized either by inserting a ballast-R at the drain of each finger, or, using a gate-coupling NMOS (gCNMOS) structure [4] as shown in *Fig. 15*. In principle, a coupling capacitor lifts the gate voltage (V_G) of NMOS to boost the substrate current that in turn accelerates the V_{BE} building-up of lateral NPN, hence reduces its V_{t1}. A very careful design is needed in selecting the values for C and R to avoid over-stressing NMOS Gox while reducing V_{t1} [29, 30].

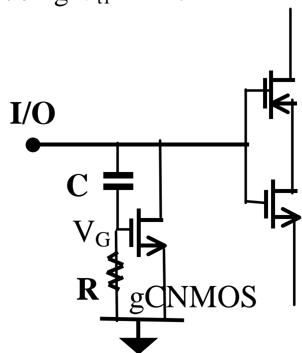

Fig. 15 A gCNMOS schematic.

4.1.3 Low-V_{t1} SCR

Conceptually, a SCR in *Fig. 12* can be used at input pins; however, it is normally not a suitable option because of its high V_{t1}. Its low-V_{t1} versions work in many cases [24, 25]. *Fig. 16a* shows one low-V_{t1} SCR where a floating N^+-layer is inserted across the n-well boundary to reduce its avalanche breakdown voltage, hence lower V_{t1} (~ 20V). *Fig. 16b* illustrates an even lower V_{t1} SCR where a ggNMOS is placed over the n-well boundary to further reduce the V_{t1} to 10-15V.

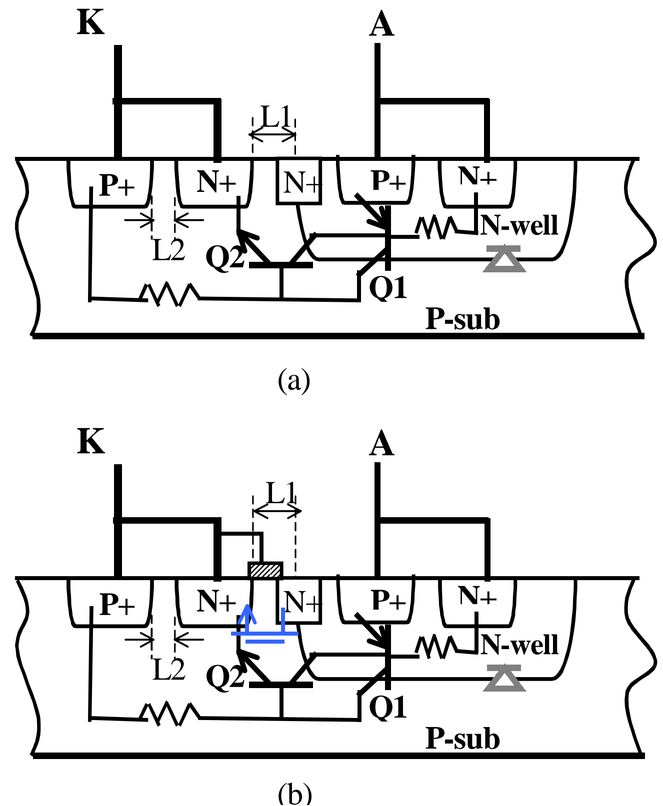

Fig. 16 LVSCR structures using N+ insertion and NMOS.

4.1.4 Compact Multiple-Direction ESD

As IC technologies advance into VDSM region, area-efficiency becomes the number one concern in ESD design to simultaneously achieve superior ESD robustness and low ESD parasitic effects on circuit performance. Two novel compact ESD designs were reported in this category. Conventionally, a complete ESD protection scheme requires multiple-devices for ESD pulses of all modes, i.e., I/O-to- V_{DD} positively and negatively (PD & ND) and I/O-to-GND positively and negatively (PS & NS), as well as V_{DD}-to-GND (DS), all for active discharging, as illustrated in *Fig. 17a*. While this scheme provides

full ESD protection, it consumes too much Si and produces substantial parasitic effect on circuit performance. A dual-direction ESD protection structure with its cross-section shown in *Fig. 18*, operating in a dual-SCR fashion, can be used to solve this problem as illustrated in *Fig. 17b*. An improved, three-terminal all-in-one ESD structure is

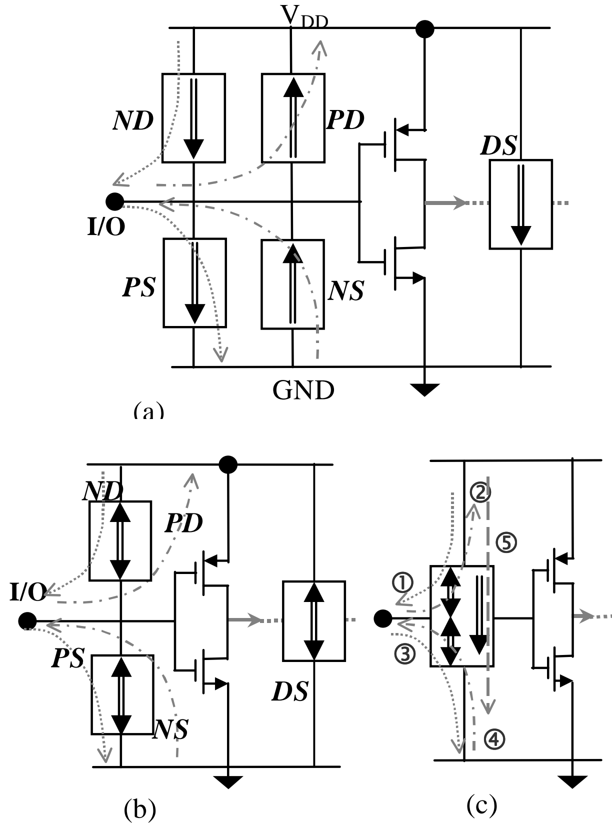

Fig. 17 Complete ESD protection schemes in traditional way (a), and using new dual-direction (b) and all-in-one (c) ESD structures.

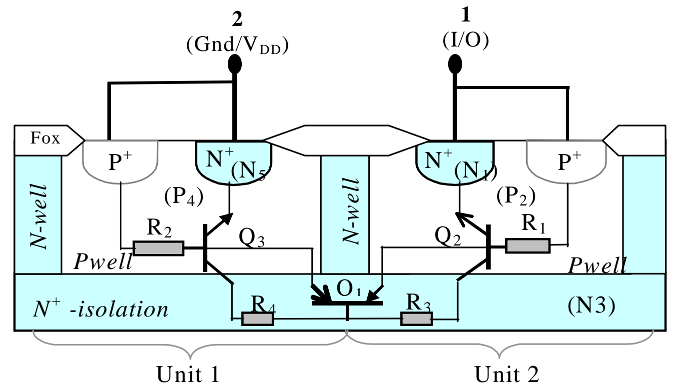

Fig. 18 A novel dual-direction ESD structure [31].

depicted in *Fig. 19*, which basically consists of two dual-direction structures. With its three terminals connected to I/O, GND and V_{DD}, one single such structure can provide complete ESD protection in all directions, including power bus clamping, as illustrated in *Fig. 17c*. The main advantage of these structures is their high area efficiency, extremely desired by mixed-signal and RF ICs. Bonding pad-oriented designs can also be realized to further improve the performance. Careful ESD simulation is crucial to ensuring proper functionality in designs. Further discussion will be given in Sections 8 & 9.

4.1.5 Trigger-Assisting for SCR

ESD structures in *Figs. 18 & 19* feature tunable V_{DD} by layer selection. For further reduction in V_{DD}, a trigger-assisting current source, shown in *Fig. 20* for the all-in-one structure, was used to provide current flowing through the lateral-R to accelerate the turn-on of vertical NPN, hence reduces V_{t1}. A Zener diode is an easy option for such an I-course [33].

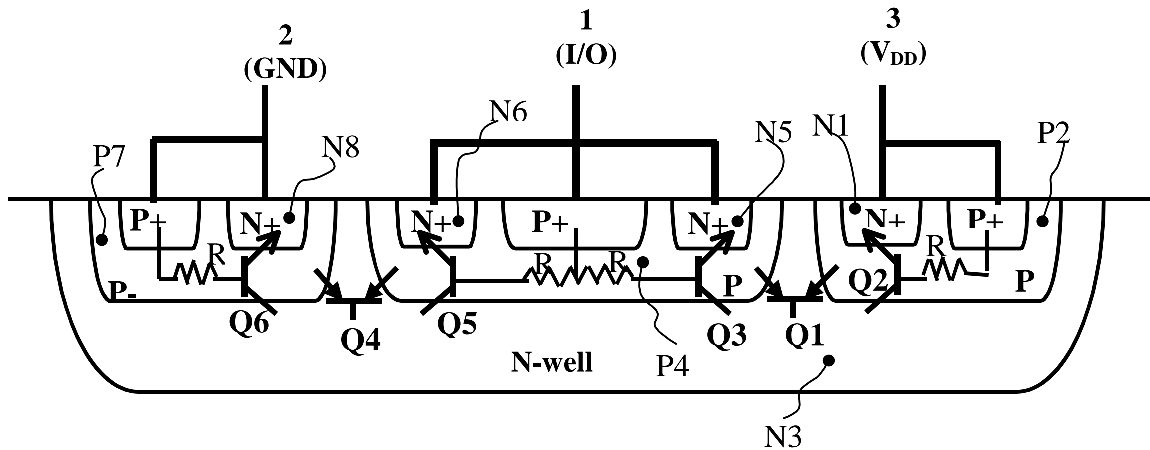

Fig. 19 A compact all-in-one ESD protection structure [32].

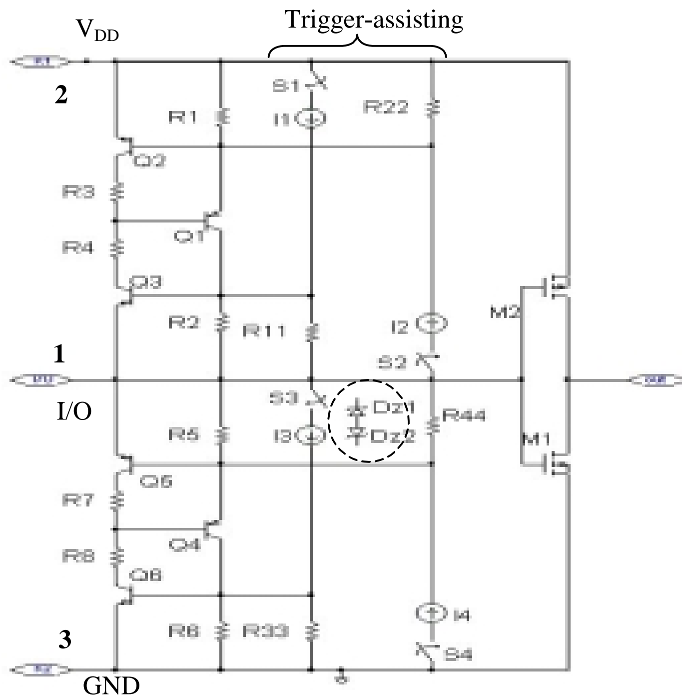

Fig. 20 A low- V_{t1} all-in-one ESD protection circuit [33].

4.2 Output ESD Protection

Most of the ESD protection structures described for the input pins can be used for output pads [4, 5]. The voltage clamping requirement is relatively relaxed for output pins because most are not directly connected to CMOS gates. On the other hand, since many output stages are buffers with high current driving capability, those large output buffer transistors are often modified to provide ESD protection. A main benefit of this technique is eliminating extra ESD structures, though a trade-off between the buffer and ESD performance has to be balanced.

4.3 Power Clamps

A power clamping structure is commonly used to protect ICs against power bus ESD surges. Multiple-finger gCNMOS and SCR type structures are good candidates for power clamps. Power clamps are normally placed at four corners on a chip, or upon device density, connected between V_{DD} and GND, or between different V_{DD}'s if multiple power buses exist. Another proven power clamp is based on a forward diode string as illustrated in *Fig. 21*. Since diodes are realized by PNP's, Darlington multiplication effect takes place in operation. Under high current condition, the β of PNP becomes very small and diode modeling can be used. To avoid the substantial leakage due to Darlington effect, a snubbing-R is used to supply current directly to the emitter of Q5 to break up the Darlington multiplication [5, 17, 18].

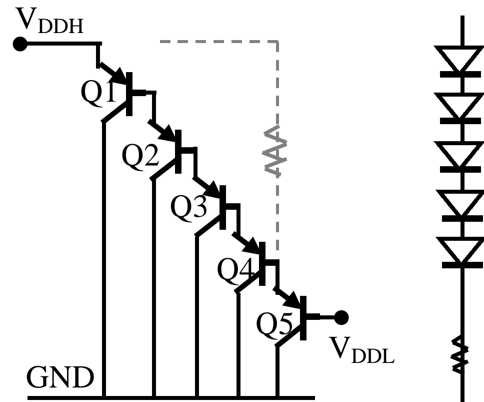

Fig. 21 A five-diode string power clamp.

Yet another big-NMOS based power clamp is shown in *Fig. 22* where the large NMOS is turned on by inverters under ESD pulses [34]. The advantage of this scheme is its SPICE compatibility.

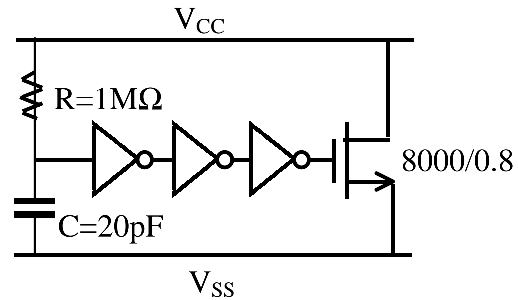

Fig. 22 A Big-NMOS clamp.

4.4 Whole-Chip Protection

A whole-chip ESD planning is critical to complete ESD protection. The rule is to ensure a low-R active discharging path from each pad to any other pads on a chip. *Fig. 23* illustrates one whole-chip ESD protection scheme that guarantees discharging channels between any two pins. The individual ESD structure may be any of those discussed previously, for example, a simple diode in forward mode. One has to estimates the worst case discharging resistance for the longest path (Pin 1 to Pin 2). If there are dual-direction ESD structures available, the schematic can be simplified substantially. A second approach is shown in *Fig. 24* where a global ESD bus is placed on a chip and dual-direction ESD

devices are used. The ESD bus may be connected to the substrate for better heat dissipation.

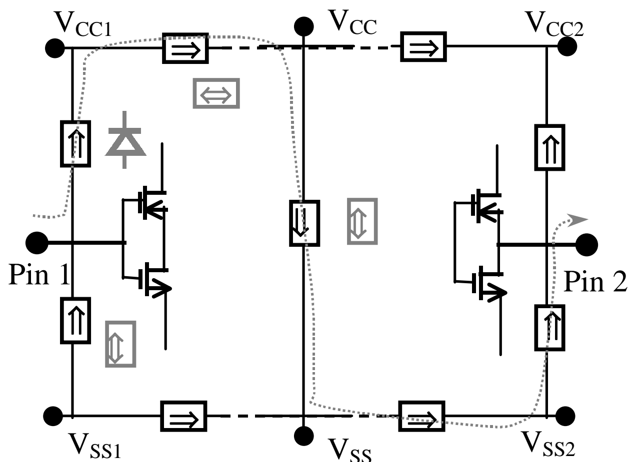

Fig. 23 Whole-chip ESD protection scheme 1.

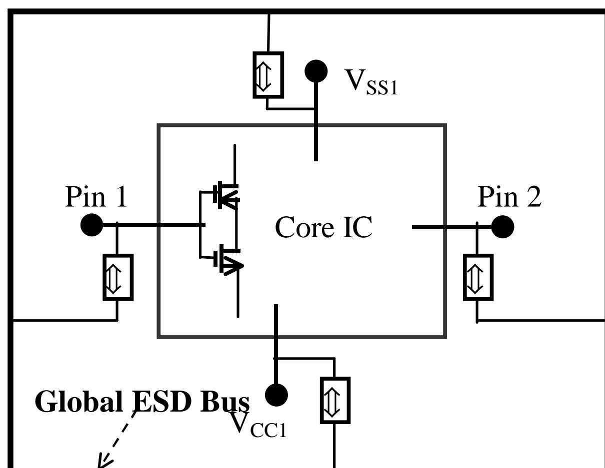

Fig. 24 Whole-chip ESD protection scheme 2.

4.5 ESD for Mixed-Signal & RF ICs

ESD protection design is more challenging in mixed-signal and RF IC applications. For mixed-signal ICs, since different circuit blocks on a chip have different specifications and most likely use different local power supplies, ranging from 1.8V to 50V plus, one has to select different ESD structures to fulfill local needs [31-33]. An all-fit ESD unit does not exist most of the time. Challenges in RF and VDSM IC ESD design mainly stem from the substantial interactions between ESD networks and core IC circuits. The most critical requirement for ESD here is small size and negligible ESD-induced parasitic effects, which will be discussed in Sec. 9.

5 ESD Failure Analysis

ESD damages are either permanent or latent in nature. Permanent ESD failures are associated with material damages due to localized heating in Si and/or metal interconnects or field stress induced dielectric rapture in CMOS gate. Latent ESD failures cause circuit performance degradation and lifetime problem; however, detail mechanism is still under investigation. ESD failure analysis (FA) is extremely important for designers to improve ESD designs. FA tools include SEM, TEM, photoemission microscopy, e-testing, etc. FA research found many unique ESD failure signatures for different ESD structures in different technologies. The following are a few typical examples. *Fig. 25* shows a typical ESD damage at an NMOS drain diffusion edge. *Fig. 26* shows ESD damage in an NMOS gate oxide. *Fig. 27* shows ESD damage occurring in one finger of a NMOS finger structure due to non-uniform turn-on.

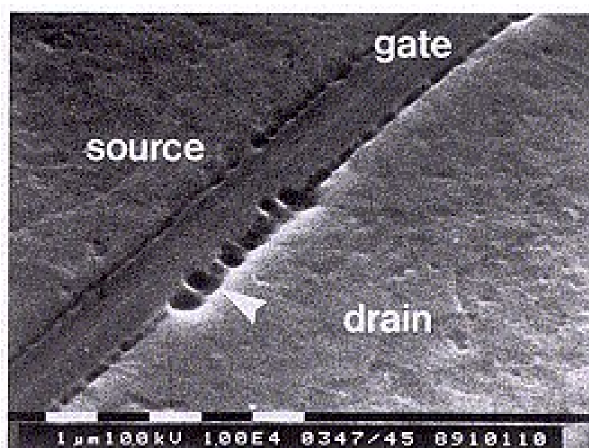

Fig. 25 ESD damage occurs at NMOS drain diffusion [35].

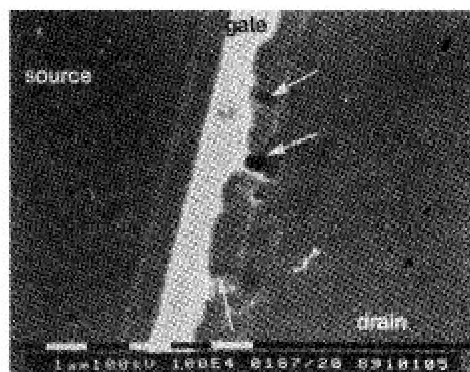

Fig. 26 ESD damage occurs at NMOS gate [35].

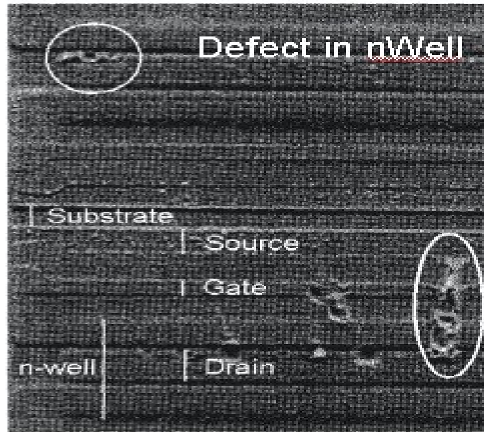

Fig. 27 ESD damage occurs at NMOS finger [36].

6 Layout and Technology Issues

ESD protection design is extremely geometry-sensitive that makes layout a critical factor. Many ESD designs, predicted working by simulation, fail pre-maturely due to careless layout, while thoughtful layout may boost ESD performance significantly.

Fig. 28 illustrates an optimized multiple-finger ggNMOS structure following a BSGD-DGSBSGD-DGSB pattern for better ESD performance [30]. Careful design on current flow path is important in avoiding I-crowding-induced early-failure (*Fig. 28b*). All corners should be smoothed (rounded) to avoid localized heating. Large diffusion-heads for resistors are suggested to avoid resistor overheating. Square cell structures are reported to boost ESD performance [60]. Some novel ESD structures may also allow bonding pad-oriented layout (surrounding or underneath pad) that saves Si areas substantially, as demonstrated in *Fig. 29*. If permitted, as many as possible contacts and vias should be used. The width of ESD metal lines is normally suggested to be 20 μm or as wide as possible. However, the wide ESD metal induced RC parasitic effect is becoming an issue in high-speed dense design [38]. Electro-thermal ESD simulation should be conducted to select just-adequate ESD metal lines for full-chip design optimization [39, 40]. In NMOS ESD structures, accepted rules suggest using large drain-contact-to-gate-spacing (DCGS ~ 5μm) and minimum source-contact-to-gate-spacing (SCGS) for optimized ESD performance. This rule generally works for technologies down to 0.25μm. However, studies indicate the minimum SCGS rule may lead to pre-mature ESD failure in sub-0.25μm technologies because the heat generated at the drain junction spreads into S-contact regions and causes thermal damages in source contacts and metal [40, 41].

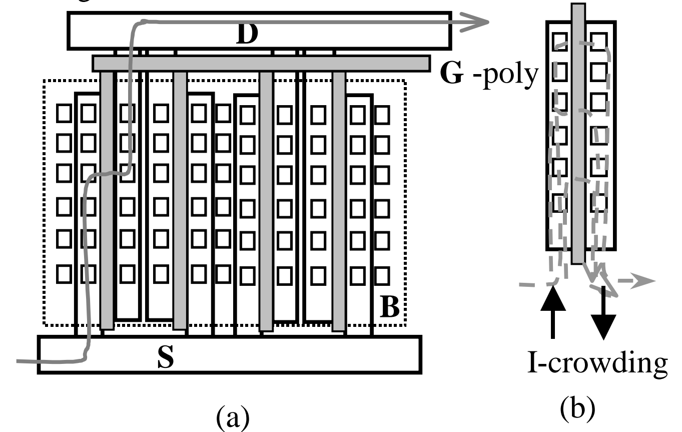

Fig. 28 A good NMOS finger structure layout.

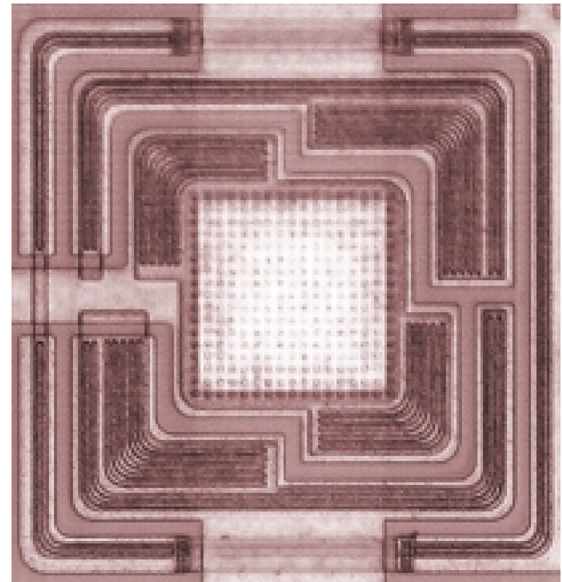
Fig. 29 A bonding pad oriented novel ESD structure [37].

IC technology advancements may affect ESD performance positively or negatively. On the negative part, new techniques, such as, LDD and salicidation, degrade ESD performance significantly, which calls for extra ESD-fixing steps in processes [4]. For example, ESD implant and salicide-blocking techniques are commonly used for such purpose. On the other hand, new copper interconnect technology can relaxes ESD concern in metal interconnection. It is therefore possible to use narrower ESD metal lines in Cu technologies [41]. Other emerging technologies,

such as SOI [61] and SiGe, also require more studies and special considerations in ESD protection design.

7 ESD Failure Modeling

Analytical models, thermal and electro-thermal, have been proposed to describe ESD device failure phenomena. A thermal model assumes the ESD failure onset associated with a critical temperature that is correlated with the power delivered to the device under stress while assuming temperature-independent electrical parameters. A power-to-failure versus time-to-failure formula was found based upon heat equation solution of an assumed localized parallelepiped heat source, as illustrated in *Fig. 30* [42-45]. Electro-thermal models [46-49] correlate device electrical parameters with temperatures based upon a coupled set of semiconductor device equations and heat distribution equation. The failure criteria are related to the device second breakdown with I_{t2} (*Fig. 9*), being the indicator. More research is under way to better understand ESD device failure mechanisms, particularly for the latent ESD failures.

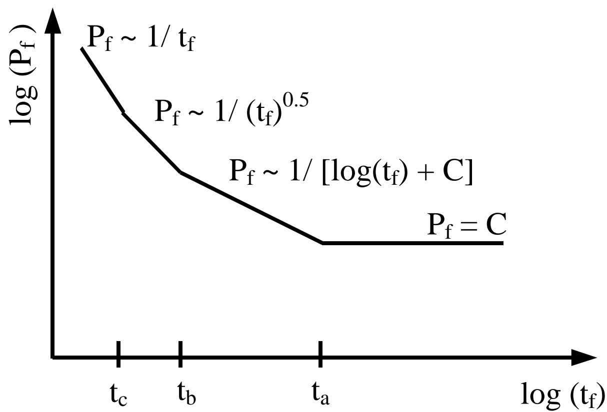

Fig. 30 A ESD device failure model.

8 ESD Design by Simulation

ESD protection design traditionally follows a trial-and-error approach due to difficulties in failure modeling and CAD tools. To date, experience-based ESD design methods still play a main role as ESD simulation techniques advance. ESD simulation methods can be classified as device and circuit levels. On one hand, ESD design prediction requires numerical simulation at device level to address the electrothermal behaviors. Efforts have been made in this area by many investigators [48-54]. On the other hand, circuit level ESD simulation is preferred by ordinary IC designers to include ESD design into whole chip design work. However, since most advanced ESD structures rely on non-SPICE-compatible snapback characteristics, while accurate high-current ESD device modeling is still not really available yet, circuit-level ESD simulation does not show much successes in practical design. A few electrothermal ESD simulators were developed, using a thermal-electronic analogy network model and snapback device models, for circuit level simulation [53, 55-57]. One main problem there is the assumption made in defining a localized parallelepiped heat source under ESD stresses. A mixed-mode TCAD-based ESD design-simulation methodology was reported recently that involves multiple-level coupling effects in simulation, *i.e.*, process-device-circuit-electro-thermal [29]. This new ESD simulation approach has been used successfully in many practical ESD design cases [30-33, 37-41]. For example, *Fig. 31* shows transient ESD simulation results for a multiple finger NMOS ESD structure where the simulation helped to reduce the V_{t1} from ggNMOS to gCNMOS to achieve uniform turn-on across fingers [30]. *Fig. 32* is another design example where a high V_{t1} (~20V) of a dual-direction ESD structure (*Fig. 18*) was reduced to ~9V using a trigger-assisting sub-circuit [31, 58]. Mixed-mode ESD simulation played a key role in these designs. It is important realize that calibration is critical for ESD simulation to achieve design prediction.

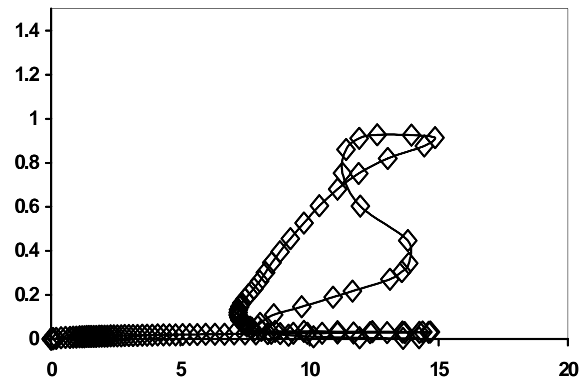

Fig. 31 (a) Simulation of a ggNMOS shows V_{t1} ~ 14.7V.

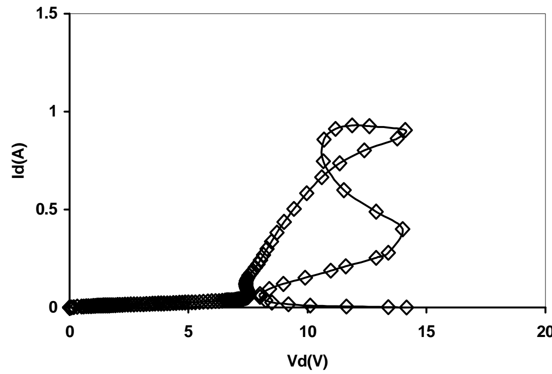

Fig. 31 (b) gCNMOS shows low V_{t1} (~7.5V).

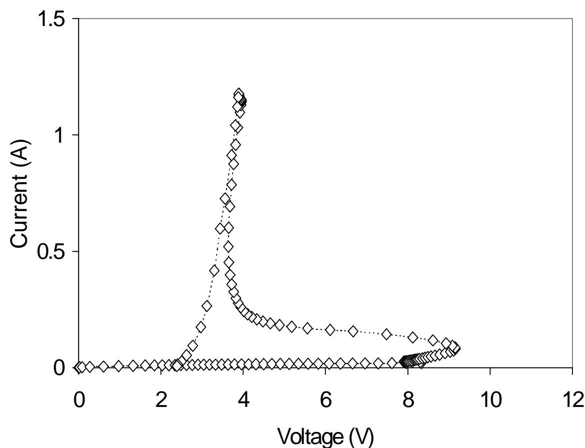

Fig. 32 Simulation shows lower V_{t1} of an ESD structure.

9 ESD-Circuit Interactions

Another extremely important, however largely overlooked, aspect in modern ESD design is the complex ESD-circuit interaction. On one hand, parasitic devices inside the circuit being protected may cause early ESD failure of a chip even though stand-alone ESD structures work well. On the other hand, the inevitable parasitic effects from the ESD protection units can influence circuit performance dramatically. Typical ESD-to-circuit impacts include ESD-induced RC delay and extra noises. These interactions become intolerable to RF ICs and other VDSM chips. It is therefore desirable to explore novel compact ESD protection solution for advanced IC chips. For example, one study [38] showed up to 30% performance degradation of a high-speed Op Amp circuit in 0.18 μm technology when using conventional NMOS ESD protection, while using compact ESD structure can recover such performance degradation by 80% as indicated in *Table 2*. Another study [59] demonstrated that using a big NMOS ESD structure increased the noise figure of a high-performance LNA by 4.5%, which was reduced to a mere 0.6% when an improved ESD protection structure was adopted, as shown in *Table 3*, without suffering ESD performance.

Table 2 an Op Amp circuit degradation due to C_{ESD} loads

Parameters	Original	ESD1	ESD2	ESD3
f_T (MHz)	126.3	-31.75%	-11.16%	-6.1%
		➥ +64.85% ↑		
		➥	+80.86%	↑
f_{-3dB} (KHz)	40.6	-7.4%	-2%	-2%
		➥ +83.78% ↑		
		➥	+83.78%	↑
Slew rate (V/us)	115.7	-30.34%	-7%	-5.5%
		➥ +76.93% ↑		
		➥	+81.87%	↑
t_{set} (nS, 1%)	9.38	-39.55%	-9.59%	-8%
		➥ +75.98% ↑		
		➥	+79.77%	↑

Table 3 An LNA noise figures vs different ESD devices

ESD Structures	LNA NF (dB)
None	1.54
ESDa (GGNMOS)	1.61
ESDb (dual-direction)	1.55

10 Future Work

It is extremely important to realize that ESD protection design takes a system approach to address the complex multiple-level coupling issues. It is equally critical to recognize that ESD protection design is not portable even within the same technology. Mixed-mode ESD simulation, though still not perfect and time consuming, should be used in advanced ESD protection design. To achieve full ESD design prediction, much research efforts are expected in such areas as, accurate high-current ESD device modeling, geometry-sensitive ESD device modeling, 3D ESD simulation, as well as whole chip level ESD design synthesis, simulation and verification.

11 Summary

In summary, this review discusses the state of knowledge of on-chip ESD protection circuit design for ICs. The discussion covers critical issues in ESD design, such as, ESD test models, ESD failure

mechanism, ESD protection structures, ESD device modeling, ESD simulation, ESD layout issues, and ESD influences on circuit functionality, etc. This review serves to provide practical IC designers with a thorough and heady reference in handling the complex ESD protection design tasks.

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