

# Phase Noise and Tuning Speed Optimization of a 5-500 MHz Hybrid DDS-PLL Synthesizer with milli Hertz Resolution

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*Abstract:* Recent research on frequency synthesis concentrates mainly on specific wireless applications requiring high-purity gigahertz carriers in a narrow frequency band, with moderate resolution and tuning speed. A low power consumption is often a must for mobility, thus a PLL solution is indicated. The main benefits of direct digital synthesis (DDS), very wide band operation with millihertz resolution, are more useful for instrumentation, where the higher power consumption is less problematic. A hybrid DDS-PLL approach can preserve most of the DDS benefits, and counter the DDS frequency limitation. This paper emphasizes on phase noise and tuning speed optimization of such an architecture. The implemented synthesizer shows a 5-500 MHz output frequency range with millihertz resolution. The single sideband phase noise at 1 kHz offset measures less than  $-80$  dBc/Hz over the full frequency range.

*Key-Words:* Phase Noise, Phase Locked Loop, Direct Digital Synthesis

## 1 Introduction

The four most important topology-determining specifications for designing frequency synthesizers are: output bandwidth (i.e. relative bandwidth), output frequency and resolution, output set up speed, and signal quality [1]. The latter can be split up into narrowband quality, i.e. phase noise and close-in spurs, and wideband quality or spectral purity which is determined by harmonic content, wideband spurs and overall noise floor.

It is clear that the design specifications of a synthesizer depend on its application, and will determine the choice of topology. The design method discussed in this paper deals with stringent demands on all four aspects of performance. The presented topology, although ideal to meet the first three requirements, is generally not considered to be suited for optimal signal quality. It will be shown however that rigorous system modeling can result in excellent performance on all four fronts.

## 2 A Measurement System Signal Source

Measurement equipment has always been a subject of research in the INTEC-design lab [2].

For vector network and signal analysis, a low-cost frequency synthesizer was needed, covering a two decade output range (5-500 MHz), with a

frequency resolution under 0.1 Hz. To reach the desired instrument measurement speed, a full range change in synthesizer output frequency must be completed in less than 1 ms. Finally, both good spectral purity and phase noise performance (goal  $<-80$  dBc/Hz@1kHz) improve measurement quality and expand the synthesizers application range. These specifications had to be achieved while keeping low cost and minimal complexity in mind.

## 3 Synthesizer Design

Both frequency range and resolution have a heavy impact on synthesizer architecture. The combined use of PLL technology and direct digital synthesis as shown on Fig.1, takes away the fundamental relationship between frequency resolution and phase detector (PD) input frequency (tuning speed) in a single loop PLL [3][4]. The use of a DDS chip as reference clock to a PLL loop partially decouples the dynamic behavior and noise performance of the synthesizer from output resolution and frequency span. This makes fine tuning combined with fast locking possible without the introduction of complex structures such as nested PLL loops.

A second advantage of this topology is the fact that it simplifies loop design itself. Critical PLL loop parameters and more specifically the divider ratio, remain constant for all output frequencies. This means that no extra compensation for loop gain

variation is required and that loop characteristics do not change significantly over the full frequency range, resulting in uniform noise performance and dynamic behavior.

This together with the fact that a 2-decade frequency span cannot be attained with a single VCO, resulted in the hybrid down-converting scheme of Fig.1.

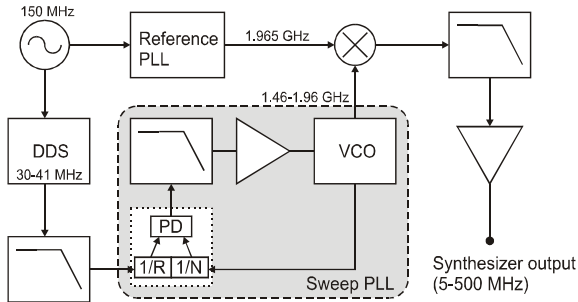


Fig.1: Synthesizer architecture

A high performance 150 MHz crystal oscillator was built and used as master clock for both reference PLL loop and DDS chip (cf. Fig.1). Its phase noise is lower than the HP8560E measurement limit, or less than  $-105\text{dBc/Hz}$  @1kHz. The reference loop provides a fixed frequency signal at 1965 MHz to the active mixer for down conversion. A filtered 30-41 MHz DDS output signal is used as reference clock for the sweep PLL. The VCO, and thus the sweep PLL itself, outputs signals ranging from 1.4 GHz to 2 GHz. Mixing both signals and applying the necessary filtering results in an output range of 5 to 500MHz.

### 3.1 Frequency Resolution

It is obvious that the synthesizer resolution is determined by the sweep PLL resolution. The DDS chip used as reference for that loop is the Analog Devices AD9852 DDS, with a 48-bit frequency register. It is driven by the 150 MHz master clock. The PLL N/R ratio (cf. Fig.1) is determined only by the VCO and DDS output range and in this case equal to 48. All the above results in a synthesizer frequency resolution of:

$$\Delta f_{out} = \frac{f_{MASTER}}{2^{48}} \cdot \frac{N}{R} = 26\mu\text{Hz} \quad (\ll 1 \text{ mHz}) \quad (1)$$

In this architecture optimal values for N and R are determined by the required dynamic behavior and noise performance, and not by frequency resolution.

### 3.2 Phase Noise and Speed Analysis

The synthesizer setup speed is solely determined by the sweep PLL locking speed. The overall phase noise performance is influenced by the mixer and output amplifier, but is primarily dominated by the PLL loop phase noise contribution. Therefore an in depth discussion of the sweep PLL will illustrate the mechanisms involved in both speed and phase noise performance.

Before moving over to the actual calculations, some quantitative remarks are made to provide more insight. It is clear, that wide loop bandwidth allows fast variations in the VCO control voltage and thus faster locking. On the other hand, the loop bandwidth determines the width of the region around the reference signal that will be tracked by the PLL. This means that reference clock spurs that lay within the PLL loop bandwidth from the carrier, can be observed at the PLL output. DDS chips are notorious for their spurious content (typical of digital signal generation), so extra care must be taken when using them as PLL references. Finally loop bandwidth has its impact on noise performance.

The dynamic behavior of the synthesizer was studied with transient simulation. First order time domain models of the loop components were created out of datasheet information and measurements. Special care was taken to model important time domain effects like phase detector behavior, amplifier small signal bandwidth, slew-rate and limiting.

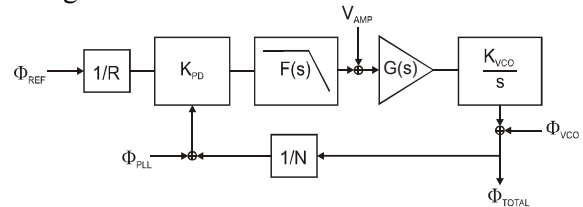


Fig.2: PLL loop noise sources

Noise analysis was based on classical frequency domain simulation of the PLL loop (cf. Fig.2) [5]. The loop parameters are: phase detector gain ( $K_{PD}$ , A/rad), VCO tuning sensitivity ( $K_{VCO}$ , rad/V), filter ( $F(s)$ ) and amplifier ( $G(s)$ ) characteristic and finally N and R divider ratios. The phase noise is modeled as phase deviation caused by FM modulation of the carrier. SSB phase noise f Hz apart from the carrier can then be expressed as:

$$L(f)[dB] = 10 \cdot \log \left( \frac{\phi_{RMS}^2(f)}{2} \right) \quad (2)$$

(note that all noise related parameters are expressed in RMS values throughout this paper).

Fig.2 shows the four main noise sources in the loop. These are:

- $\phi_{REF}(f)$ : Reference oscillator phase noise injected into the loop.
- $\phi_{VCO}(f)$ : VCO phase noise.
- $\phi_{PLL}(f)$ : PLL chip noise.
- $V_{AMP}(f)$ : Amplifier input referred RMS voltage noise contribution.

The amplifier noise contribution is a combination of opamp voltage noise, opamp current noise and equivalent source resistance input noise. The latter can be derived from the source impedance that is offered to the amplifier input by the loop filter. Note that the amplifier noise is highly frequency dependant, especially for low frequencies (flicker noise).

It is easily seen that the total PLL output phase noise is equal to:

$$L(f)[dB] = 10 \cdot \log \left( \frac{\sum_{NoiseSources} \phi_{LOOP\_CONTRIBUTION}^2(f)}{2} \right) \quad (3)$$

The separate contributions of reference oscillator, VCO, PLL and amplifier are respectively:

$$\phi_{LOOP\_REF}^2(f) = \left| \left( \frac{N/R}{1 + 1/G_{OL}(j \cdot 2 \cdot \pi \cdot f)} \right)^2 \cdot \phi_{REF}^2(f) \right| \quad (4)$$

$$\phi_{LOOP\_VCO}^2(f) = \left| \left( \frac{1}{1 + G_{OL}(j \cdot 2 \cdot \pi \cdot f)} \right)^2 \cdot \phi_{VCO}^2(f) \right| \quad (5)$$

$$\phi_{LOOP\_PLL}^2(f) = \left| \left( \frac{N}{1 + 1/G_{OL}(j \cdot 2 \cdot \pi \cdot f)} \right)^2 \cdot \phi_{PLL}^2(f) \right| \quad (6)$$

$$\phi_{LOOP\_AMP}^2(f) = \left| \left( \frac{N}{1 + 1/G_{OL}(j \cdot 2 \cdot \pi \cdot f)} \right)^2 \cdot \left( \frac{1}{K_{PD} \cdot F(j \cdot 2 \cdot \pi \cdot f)} \right)^2 \cdot V_{AMP}^2(f) \right| \quad (7)$$

With open loop gain  $G_{OL}(s)$  defined as:

$$G_{OL}(s) = K_{PD} \cdot F(s) \cdot G(s) \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N} \quad (8)$$

### 3.3 Optimized Phase Noise Performance

The phase noise performance of the PLL loop was optimized using the listed formulas. The locking

speed (5–500 MHz) was limited to 1 ms. As expected, the simulations showed that extra care had to be taken in designing the PLL reference clock. For that reason a high performing DDS like the AD9852 was used and extra effort was put into the design of the master clock.

Furthermore, the calculations indicated that the loop amplifier impact on noise performance could not be neglected, thus a very low-noise opamp was used (the amplifier is necessary in the loop to scale the maximum PLL output to the VCO tuning voltage range). Finally, the VCO phase noise specifications seemed to influence the overall phase noise performance less than was expected.

The phase noise performance of the final PLL is listed in Table 1, and can be seen on Fig.3 and Fig.4. With the chosen loop parameters, the contributions of the different noise sources are comparable (Fig.3). Herein lays the explanation of the difference between calculated and measured data: the modeling errors on all noise sources are accumulated. Furthermore, the relative errors become rather large because of the low absolute noise level. To illustrate this the PLL reference clock was replaced with a HP8648B signal generator. The phase noise built up in the system was now primarily caused by the reference clock and much larger, resulting in an even closer match between simulation and measurements. The results are listed in Table 2.

<i>phase noise (dBc/Hz) @</i>	<i>simulated</i>	<i>measured</i>
1 kHz	-90	-91
10 kHz	-93	-90
100 kHz	-96	-99
1 MHz	-125	-121

Table 1: Optimized PLL phase noise performance

<i>phase noise (dBc/Hz) @</i>	<i>simulated</i>	<i>measured</i>
1 kHz	-60	-60
10 kHz	-73	-74
100 kHz	-91	-94
1 MHz	-124	-121

Table 2: PLL phase noise performance with signal generator as reference

Transient modeling is less difficult and results in a near perfect match between simulation and reality, both show a locking time of 670 $\mu$ s (cf. Fig.5 and Fig.6).

### 3.4 Spurious Sidebands

It was mentioned before that spurious content typical to DDS is reflected in the synthesizer output signal. Next to spurious generated by e.g. a digital

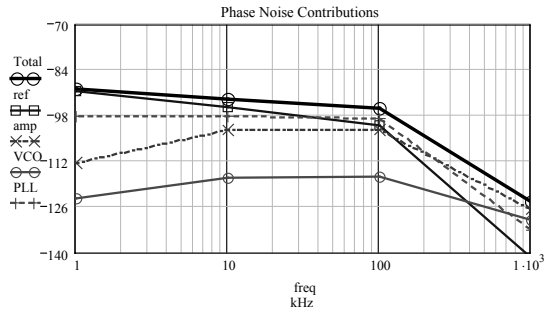


Fig.3: Simulated impact of different noise contributors on overall phase noise performance

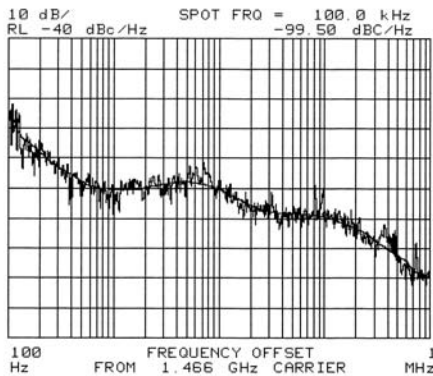


Fig.4: Measured phase noise of sweep PLL output

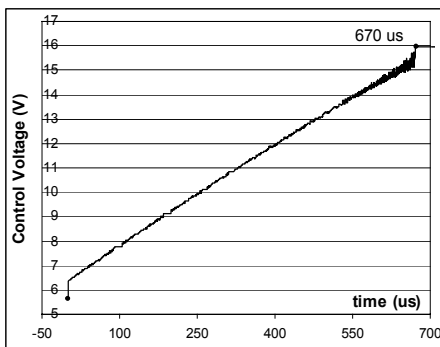


Fig.5: Simulated VCO control voltage (Switching from 5 to 500 MHz)

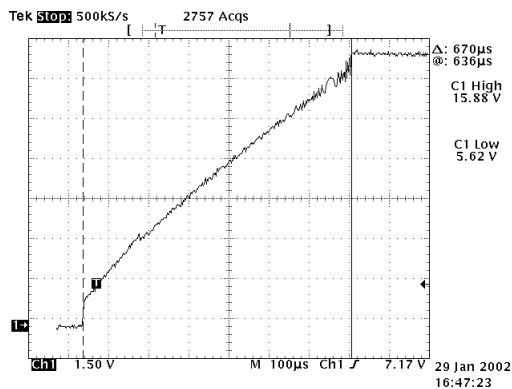


Fig.6: Measured VCO control voltage (Switching from 5 to 500 MHz)

PLL chip, this spectral pollution is inherent to the architecture and imposes a hard limit on spur performance. Because of the nature of the application, this design mainly focused on phase noise performance and tuning speed, however some remarks should be made.

DDS spurs that lay within sweep PLL bandwidth of the carrier are amplified by  $20 \cdot \log(N/R)$  within the PLL loop. This indicates a third criterion for DDS chip selection next to phase noise and frequency resolution. The chosen DDS (AD9852) exhibits excellent spurious performance, within 250kHz bandwidth all spurs are  $-84$  dB below the carrier, resulting in an overall synthesizer spurious performance better than  $-84 + 20 \cdot \log(48)$  or  $-50$  dBc (cf. Fig.7).

If spurious sidebands are of high concern, one solution is to upconvert the DDS output and use dividers to shift the frequency down again. This will give a spurious reduction of  $20 \cdot \log(\text{divider ratio})$ .

### 3.5 Overall Performance

The phase noise performance of both mixer inputs is reflected at the mixer output. Therefore equal effort was put into the design of the two PLL loops. This resulted in similar noise spectra for the reference signal and the sweep signal. As expected, both mixer and amplifier impact on overall synthesizer signal quality was limited. The measured specifications of the final synthesizer design are summarized in Table 3.

Frequency range	5-500	MHz
Frequency resolution	$\ll 1$	mHz
Output Power	7	dBm
Gain flatness	$\pm 1$	dB
Phase Noise @1 kHz	$< -80$	dBc/Hz
Phase Noise @100 kHz	$< -95$	dBc/Hz
Max. Span setup speed (5-500MHz)	670	$\mu$ s

Table 3: Summarized frequency synthesizer specifications

## 4 Conclusion

Phase noise and tuning speed optimization of a two decade frequency synthesizer was presented. A synthesizer with 5-500 MHz range and millihertz resolution was built based on the phase noise calculations described in this paper. A close match between predicted and measured results proves that

Careful modeling can lead to a good overall performance with relatively simple architectures.

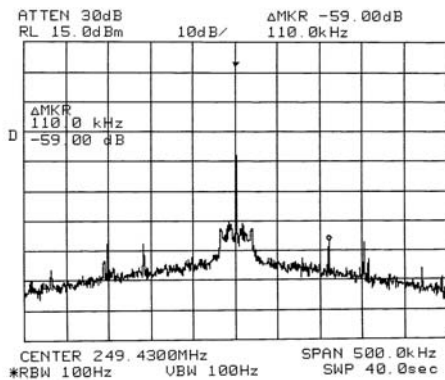


Fig.7: Example of spurious sidebands at synthesizer output (highest spur  $-59\text{dBc}@110\text{kHz}$ )

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