Synchronism Architecture Implementation for High Quality Audio Processing and Transmission

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Abstract: Transmission of high quality audio over telecom networks requires specific synchronization schemes. It is necessary to maintain a high grade of fidelity over several signal parameters. Particularly important is to achieve a effective synchronization between source and destination. Deviation in sampling frequencies implies distortions, especially noticeable in high quality audio. In the case of transmission over a standard telecom network, is possible is to extract the network synchronism and reuse it to generate the sampling frequency and processor clock at both ends. The contribution of this paper is the description of an implemented design for a generic architecture allowing locking network clock and necessary synchronism for audio processing at both ends of the communication network. Illustrated design is applicable to multi-codec and multi-channel architectures where global common synchronization is required.

Key-Words: Audio DSP, Audio compression, Sampling frequency, PLL, Audio transmission, Synchronism.

1 Introduction

There are several applications that require the transmission of digitalized compressed audio signals in the environment of local or wide area networks. Examples of these applications are multimedia transmission, audio/video conferences, HiFi sound distribution, etc [1]. An intensive digital processing can be present between the original analog sound and the final signal recovering. Clock references of source and destination could have divergences (Jitter, wander,..) and when long distances is an additional requirement, synchronism becomes a hazard. Small variations over the sampling frequency imply very noticeable signal impairment. To maintain the quality parameters of these very susceptible signals is necessary to take special care in all blocks of design. This paper describes the implementation of an hardware architecture over the synchronism part that provides a very precise recovery of original sampling frequency and allows mirror synchronization of processors. Additionally, the architecture provides this advantage over the main high quality audio signals sampling frequencies: 32, 44.1 and 48 Khz. Figures are provided for a 2 Mbps standard ITU-G.703 [2] example telecom network.

2 Audio transmission scenario

Figure 1 illustrates the reference scenario of an audio transmission system using the proposed architecture.

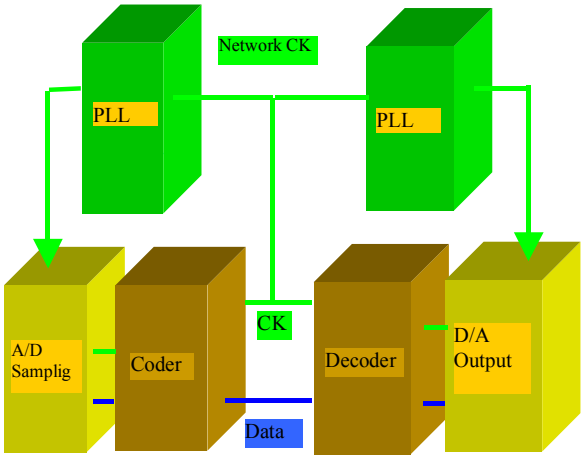

Fig. 1. Network reference

Usually networks have a reference clock that could be a generic external common one or could be internally generated by a master transmitter. The digital network could impact in the quality of the digital signal basically in two ways: time distortion (Jitter or wander) and noise or amplitude distortion, both produce, in worst case, errors that can be measured by the Bit Error Rate (BER). Recovering an analog signal after digital transmission means

additional sources of distortions. When the extracted sampling frequency is not an exact reproduction of the original one, distortion impairments could becomes audible. We propose in this paper a configuration based in a mirrored PLL that generates the transmitter sampling frequency and extract in the receiver a precise reproduction, taking in both ends the network clock as main reference. Additionally, this reference synchronism will allow generation of DSP processors clock and alignment in multi-codec architectures.

3 Coder

Considering the existence of a external reference clock for the network does not imply any loss of generality in our proposal. Following this hypothesis the mechanism for extracting references in transmitter and receiver part could be very similar.
Fig. 2 represents a zoom inside synchronization part of the coder. DSP processor receives digital samples from de A/D converter via Serial Synchronous Interface (SSI) with a clock extracted from network. Processor sends digital data to network by Serial Communication Interface (SCI) at the rhythm of clocks obtained from same source (network reference). Block diagram reveals the presence of a Phase/Frequency Lock Loop (PLL) that allows generation of needed clocks.

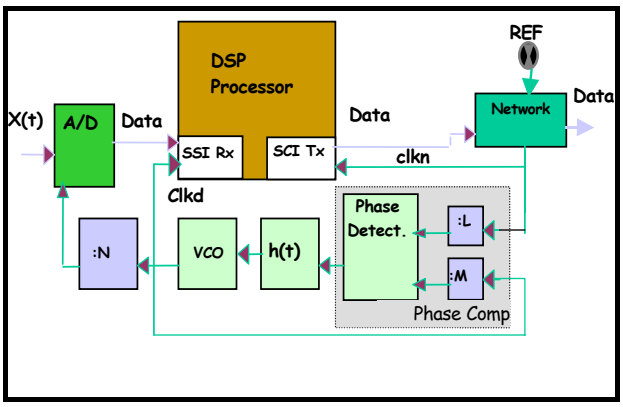

Fig.2. Coder synchronism

4 PLL Circuit

This circuit generates the reference clocks for the A/D converter and the writing/reading clocks for SSI and SCI mentioned in previous paragraph. All of them are locked to the network clock frequency (2 Mhz ITU-G.703 [2] in our example). The diagram in figure 3 shows the structure of the design.

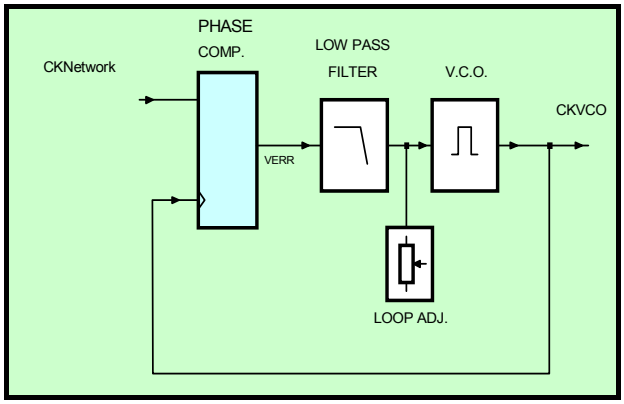

Fig.3. PLL Block diagram

The circuit showed in figure 3 has PLL architecture with phase comparator, including clock dividers, low pass filter and voltage controlled oscillator (VCO). It allows the frequency locking between the reference clock and the synthesized one.
A 2 Mhz network extracted clock goes into the phase comparison. The synthesized clock is CKVCO, which after division will be the master one for A/D conversion. It has to be divided before the phase comparison in order to obtain the same frequency than the reference clock. The implemented circuit supports the frequency division and phase comparison for all the possible master frequencies by setting a group of switches. Table 1 shows different configurations according selected sampling frequency.

Table 1.- Master frequency selection

SAMPLING FREQ.	CKVCO FREQ.	COMPARISON FREQ.
32 KHz	12.288MHz	512 KHz
48 KHz	12.288MHz	512 KHz
44.1 KHz	16.934MHz	6.4 KHz

Phase comparison is made at the comparison frequency by an exclusive OR logic function between divisions of CKnetwork and CKVCO clocks. It generates a digital signal (VERR) with double frequency than the comparison one and duty cycle variable with the frequency deviation. At nominal frequency, the duty cycle has to be 50 %, which can be adjusted with a potentiometer (Loop Adj.).
VERR signal is filtered to obtain the direct voltage that controls the VCO function. A R-C filter obtains the average voltage of the VERR signal (variable with the duty cycle) and an active low pass filter controls the loop stability.
The VCO circuit is an integrated VCXO device (Voltage Controlled Crystal Oscillator) with the nominal frequency required for the application and a locking range of +/- 100 PPM.

5 Phase comparison implementation

To allow compatibility of the circuit layout in all synthesized frequencies, it has been considered the frequency division and comparison architecture shown in figure 4. The phase comparison is implemented at an exclusive OR logic function between the CKREF2AD signal and the division of the CKVCO signal.

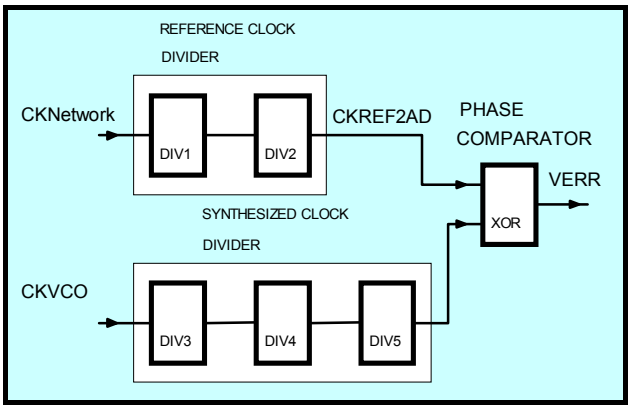

Fig.4. Phase comparison architecture

This distribution allows a reduction in the number of the required devices and, also guarantees the compatibility with most standards D/A and A/D synchronism architecture, which have to consider the generation of a digital serial interface clock. Table 2 shows the division factors for all possible sampling frequencies. Hypothesis of 2 Mhz network clock does not mean any lost of generality. Usually, higher capacity networks have clocks that are multiples of this basic 2 Mhz frequency, and that implies a simple factor addition to given in table 2. These dividers are implemented over programmable logic devices. Design require special care of layout in order to avoid signal noise or interference [3]

Table 2.- Division Factors

SAMPLING FREQUENCY	DIV1	DIV2	DIV3	DIV4	DIV5
32 KHz	4	1	3	8	1
48 KHz	4	1	3	8	1
44.1 KHz	4	80	3	18	49

From tables 1 and 2 and figure 4 we can assume that different configurations for the possible sampling frequencies may be set automatically except the case of 44.1 Khz, that needs a change of VCO crystal.

6 Tests and Results

The proposed design has been used for the implementation of a DSP processor board based on a Motorola 56002 DSP [4][5] and a Crystal A/D and D/A[6] converter among other necessary circuits to complete an audio processing architecture development. The full system design is based on three boards: Coder, Decoder and Transmitter-Receiver interface [7]. The system has been tested in two steps: a set of objective tests and some statistical subjective tests. Tests on audio processing systems using compression algorithms require subjective tests [8].

Tests environment use the configurations following recommendations described in ITU-T J.52 [9] and ITU-R BS.1284 [10]. Objective tests has been done introducing jitter over 2 Mhz transmission clock and measuring the impact over the resulting source and extracted sampling frequencies at the encoder and decoder sides. Variations of ±100 ppm, that is the standard tolerance of the network clock, impact on the resulting frequency that follows the network clock deviations.

Previous results indicate that the behavior of the PLL circuit is according prediction. However there are variations from the nominal sampling frequency values that could impact on the quality of the recovered signal. From this observation we can deduce that PLL filters setting will be very impacting over jitter and wander filtering.

We conclude that PLL tuning according expected network clock behavior (Jitter of high or low frequency) would provide best results over sampling frequency stability and fidelity. Additional tests must be done to guaranty the right response.

Tests of S/N and distortion parameters have been done transmitting a bit stream from sampling a CD quality signal at 48 and 32 Khz, using a linear algorithm without compression. Network clock has been set at different values in the range of ±100 ppm. Considering the CD quality audio signal sampled at 48 Khz with 16/18 bits of samples resolution, the obtained S/N values in the receiver side (95 dB) demonstrates the high fidelity of the system.

Additional subjective tests results arise similar values than expected according to UIT-R BS.1115 [11].

7 Future Works

Next specific research, implementation and tests will be done over similar functionality applied to packets networks. The implementation under packets networks requires buffering of samples and special control of the PLL depending of the network latency. Continuation investigations on this design will be inside a working group dealing with researches on

tele-learning applications and quality of service over LAN and WAN packets networks [12][13].

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