

# BiCMOS Current-Controlled Current Feedback Amplifier (CC-CFA) and Its Applications

MONTREE SIRIPRUCHYANUN<sup>1</sup>, CHAIYAN CHANAPROMMA<sup>2</sup>, PHAMORN SILAPAN<sup>3</sup> and WINAI JAIKLA<sup>4</sup>

<sup>1,2</sup> Department of Teacher Training in Electrical Engineering, Faculty of Technical Education, King Mongkut's University of Technology North Bangkok, Bangkok, 10800, THAILAND

<sup>3</sup> Electric and Industrial Program, Faculty of Industrial Technology, Uttaradit Rajabhat University, Muang, Uttaradit, 53000, THAILAND

<sup>4</sup> Electric and Electronic Program, Faculty of Industrial Technology, Suan Sunandha Rajabhat University, Dusit, Bangkok, 10300, THAILAND

mts@kmutnb.ac.th, chaiyanc@kmutnb.ac.th, phamorn@mail.uru.ac.th, jnai2004@yahoo.com  
<http://www.te.kmutnb.ac.th/~msn/>

*Abstract:* - This paper introduces a modified version of current feedback amplifier (CFA), called current controlled current feedback amplifier (CC-CFA), to extend usability of this active element in terms of electronic control-abilities and simpler circuit description of the element's applications. This modified element was realized by using a BiCMOS standard technology to reduce offset error phenomenon, the design configuration is systematically explained. The performances have been proven through PSPICE which is accordance with theoretical anticipations. In addition, application examples for a current-mode multiplier/divider, oscillator, grounded inductance simulator, filters, and amplifiers are included. The results are confirmed that the electrical characteristics are electronically tunable.

*Key-Words:* - CC-CFA, Current-mode, Voltage-mode, Filter, Oscillator, Inductance simulator, Multiplier

## 1 Introduction

There has been much effort to reduce the supply voltage of electronic circuits in the last decade. This is due to the demand for portable and battery-powered equipment. Since a low-voltage operating circuit becomes necessary, the current-mode technique is ideally suited for this purpose more than the voltage-mode one. Consequently, there is a growing interest in synthesizing the current-mode circuits because of more their potential advantages such as larger dynamic range, higher signal bandwidth, greater linearity, simpler circuitry and low power consumption [1-2]. Many active elements able to function in current-mode such as OTA, current feedback amplifier, current conveyor [3], current differencing buffered amplifier (CDBA) [4] and current differencing transconductance amplifier (CDTA) [5], and etc., have been introduced to response these demands.

Among the mentioned active building blocks, the current feedback amplifier (CFA) or current feedback operational amplifier (CFOA) is an interesting active component, especially suitable for a class of analog signal processing [6-8]. This device can operate in both current and voltage-modes, provides flexibility and enables a variety of

circuit designs. In addition, it can offer advantageous features such as high-slew rate, free from parasitic capacitances, wide bandwidth and simple implementation [9-11]. Presently, the CFA can be commercially found, for example AD844 of Analog Devices Inc. [7]. It can be employed to realize filters [10-13], amplifiers [14], oscillators [15-19], inductance simulators [20-21], and etc. [22-24]. Conventionally, the electrical characteristics for applications of the CFAs cannot be adjusted by electronic methods, which this means that they cannot be controlled by currents and/or voltages. Although, they can be achieved by passive element adjustments, the electronic control method is being more popular more than those by passive elements (i.e. resistors and capacitors) [25] due to it can be easily adapted to automatic or microcontroller-based controls [26]. In addition, the CFA can not be controlled by the parasitic resistance at current input port so when it is used in a circuit, it must unavoidably require some external passive components, especially the resistors. This makes it not appropriate for IC implementation due to occupying more chip area, high power dissipation and cannot be electronic controllable. If it is employed for an off-the-shelf design, the circuit

description is composed of a large number of external passive elements. Actually, the electronic control can be done in a CFA application by replacing a resistor by junction field effect transistor (JFET) employed in voltage controlled resistor (VCR) region [19]. Unfortunately, it makes circuit description more complicated. Furthermore, the conventional CFA was designed by using the BJT and a basic voltage follower, consequently, this structure has problem for the output offset errors because the BJT current mirrors in the CFA provide errors due to practically internal factors more than a current mirror based on CMOS [27]. The offset output error from the basic voltage follower also affects the accuracies of circuits/systems. The offset problem is an important factor for circuit designers to be certain in practical implementations, especially in instrumentation and measurement systems.

In this work, thus, a modified-version CFA whose parasitic resistance at current input port can be controlled by an input bias current, called current controlled current feedback amplifier (CC-CFA), will be reviewed via this article. To reduce offset phenomenon, a BiCMOS technology is suitable for realizing the proposed element. In addition, the voltage follower is also developed to reduce the offset output current and voltage. The performances of proposed BiCMOS CC-CFA are illustrated by PSPICE simulations, they show good agreement as mentioned. The example applications as a multiplier/divider, oscillator, grounded inductance simulator, filters, and amplifiers are included.

## 2 Circuit Configuration

### 2.1 Basic Concept of CFA

The CFA properties can be shown in the following equation

$$\begin{bmatrix} I_y \\ V_x \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \\ V_w \end{bmatrix} \quad (1)$$

The symbol and the equivalent circuit of the CFA are illustrated in Fig. 1(a) and (b), respectively. A circuit implementation of CFA can be achieved by using second-generation current conveyor (CCII) as input stage, followed by a buffered amplifier as depicted in Fig. 1(c).

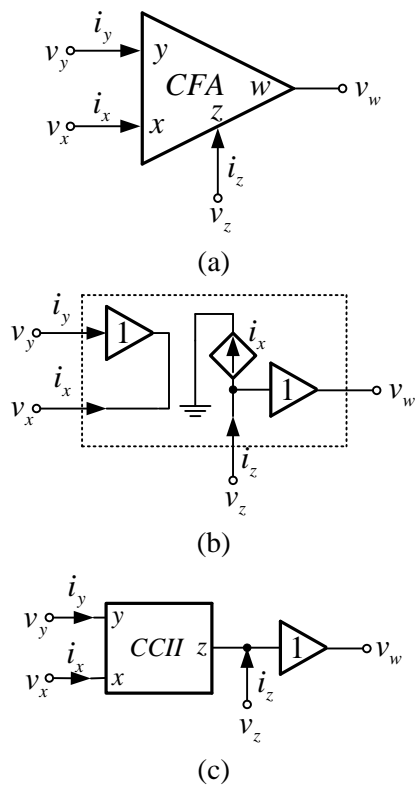


Figure 1. CFA (a) Symbol (b) Equivalent circuit (c) Element implementation

### 2.2 Basic Concept of CC-CFA

CC-CFA properties are similar to the conventional CFA, except that the CC-CFA has finite input resistance  $R_x$  at the  $x$  input terminal. This parasitic resistance can be controlled by the bias current  $I_B$  as shown in the following equation

$$\begin{bmatrix} I_y \\ V_x \\ I_z \\ V_w \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ R_x & 1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \\ V_w \end{bmatrix} \quad (2)$$

where

$$R_x = \frac{V_T}{2I_B} \quad (3)$$

$V_T$  is the thermal voltage, which is 26mV at room temperature. The symbol and equivalent circuit of the CC-CFA are illustrated in Fig. 2(a) and (b), respectively. In similar, we can realize the CC-CFA by using second-generation current controlled current conveyor (CCCII) as input stage, followed by a buffered amplifier as illustrated in Fig. 2(c).

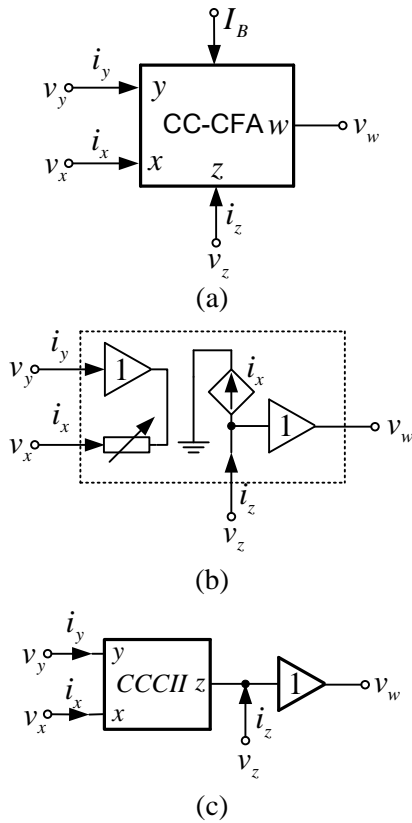


Figure 2. CC-CFA (a) Symbol (b) Equivalent circuit (c) Element implementation

**2.3 Simple BJT current mirror compared to MOS current mirror**

Since the current mirror is the basic block to realize CC-CFA, a comparison of the simple BJT and MOS current mirrors will be shown in this section. Fig. 3(a) displays the BJT current mirror. From routine analysis, the output current can be expressed to be [27]

$$I_{out} = \frac{I_{S2}}{I_{S1}} I_{in} \left( 1 + \frac{V_{CE2} - V_{CE1}}{V_A} \right) \cdot \left( 1 + \frac{1 - (I_{S2}/I_{S1})}{\beta_F} \right) \quad (4)$$

If  $I_{S2}/I_{S1}$  is the ideal gain of the BJT current mirror and  $V_A$  is the Early voltage, the systematic gain error of the BJT current mirror ( $\epsilon_{BJT}$ ) can be found to be

$$\epsilon_{BJT} = \frac{\left( 1 + \frac{V_{CE2} - V_{CE1}}{V_A} \right)}{1 + \frac{1 - (I_{S2}/I_{S1})}{\beta_F}} \cong \frac{V_{CE2} - V_{CE1}}{V_A} - \frac{1 - (I_{S2}/I_{S1})}{\beta_F} \quad (5)$$

From Eq. (5), the first term is originated from finite output resistance and the second term comes from finite  $\beta_F$ . The MOS current mirror is illustrated in Fig. 3(b). By straightforward analysis, we will receive

$$I_{out} = \frac{(W/L)_2}{(W/L)_1} I_{in} \left( 1 + \frac{V_{DS2} - V_{DS1}}{V_A} \right) \quad (6)$$

If  $(W/L)_2/(W/L)_1$  is the ideal gain of the MOS current mirror, the systematic gain error of the MOS current mirror ( $\epsilon_{MOS}$ ) can be expressed to be

$$\epsilon_{MOS} = \frac{V_{DS2} - V_{DS1}}{V_A} \quad (7)$$

From Eq. (7), the gain error of the MOS current mirror stems from only the finite output resistance implied from the Early voltage which differs from the gain error of the BJT as depicted in Eq. (5). This result shows that the MOS current mirror has more accuracy than the BJT one. One reason is that the MOS generally provides higher Early voltage than the BJT does [27]. Consequently, CMOS is employed in the current mirrors to implement the proposed CC-CFA.

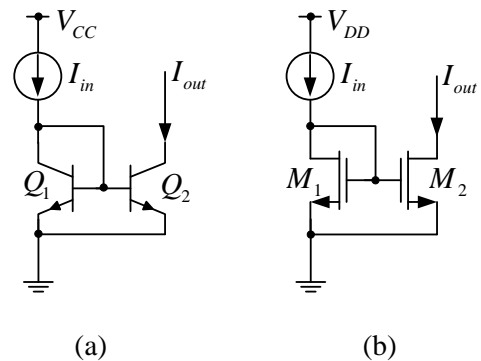


Figure 3. Simple current mirrors based on (a) BJT (b) MOS

**2.4 A BiCMOS second generation current controlled current conveyor**

Fig. 4 displays a class AB translinear loop, which is used as input section. The BJT translinear is used to achieve linear adjustability of intrinsic resistance. When all transistors are considered to be matched elements and working in saturation-mode. The following currents can be obtained [28].

$$I_7 = I_B e^{(V_{xy}/V_T)} \quad (8)$$

and

$$I_9 = I_B e^{-(V_{xy}/V_T)}. \quad (9)$$

Due to

$$I_x = I_7 - I_9. \quad (10)$$

Substituting Eqs. (8) and (9) into (10), it yields

$$I_x = 2I_B \sinh(V_{xy}/V_T). \quad (11)$$

Since  $\sinh(V_{xy}/V_T) \cong V_{xy}/V_T$  for  $V_{xy} \ll V_T$ , we will obtain

$$R_x = \frac{V_T}{2I_B}. \quad (12)$$

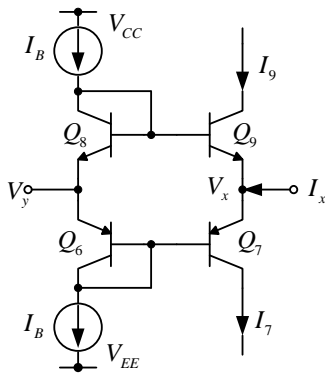


Figure 4. Class AB translinear loop

The BiCMOS class AB second generation current controlled current conveyor is shown in Fig. 5, which is modified from class A one in [29]. The circuit implementation consists of mixed translinear loops (Q<sub>6</sub>-Q<sub>9</sub>), which are DC biased by  $I_B$ . The z-terminal output that generates the current of x terminal is realized using transistors (M<sub>4</sub>-M<sub>5</sub> and M<sub>12</sub>-M<sub>13</sub>). The x terminal resistance can be obtained by Eq. (12). From elementary small-signal circuit analysis, the output current  $I_z$  of this circuit can be expressed as

$$I_z = \alpha I_x + \varepsilon, \quad (13)$$

where  $\alpha$  and  $\varepsilon$  are current gain and offset error terms, respectively. By straightforward analysis of the circuit in Fig. 5 and  $g_{mi} \gg g_{\pi i}$ , we will obtain the  $\alpha$  and  $\varepsilon$  as

$$\alpha = \frac{1}{g_{m4}g_{m12}} \left( \frac{g_{m4}g_{m9}g_{m13}}{g_{m9} + g_{m7}} + \frac{g_{m5}g_{m7}g_{m12}}{g_{m9} + g_{m7}} \right) \quad (14)$$

and

$$\varepsilon = K_1 + K_2, \quad (15)$$

where

$$K_1 = \frac{I_B}{g_{m4}g_{m6}g_{m12}} \left[ \frac{g_{m4}g_{m7}g_{m9}g_{m13}}{g_{m9} + g_{m7}} + g_{m5}g_{m7}g_{m12} \left( \frac{g_{m7}}{g_{m9} + g_{m7}} - 1 \right) \right] \quad (16)$$

$$K_2 = \frac{I_B}{g_{m4}g_{m8}g_{m12}} \left[ \frac{g_{m5}g_{m7}g_{m9}g_{m12}}{g_{m9} + g_{m7}} + g_{m4}g_{m9}g_{m13} \left( \frac{g_{m9}}{g_{m9} + g_{m7}} - 1 \right) \right] \quad (17)$$

If the transistors are matched, which means that  $g_{m6} = g_{m7} = g_{m8} = g_{m9}$ ,  $g_{m12} = g_{m13}$  and  $g_{m4} = g_{m5}$ , the current  $I_z$  can be expressed as

$$I_z = I_x. \quad (18)$$

The output resistance looking into the z terminal can be respectively expressed as

$$r_z \cong \frac{r_{ds}}{2}, \quad (19)$$

where  $r_{ds}$  is the drain-source resistance seen at the mentioned output terminal.

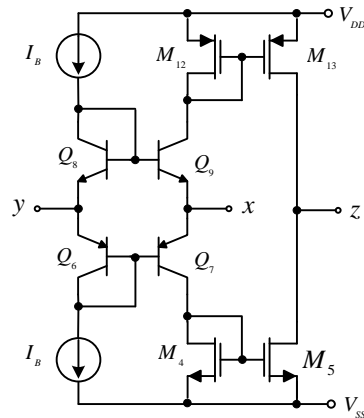


Figure 5. The BiCMOS class AB second-generation current controlled current conveyor

### 2.5 Modified BiCMOS Buffered Amplifier

Conventionally, the basic buffered amplifier [30] can be realized by the circuit shown in Fig. 6(a). It consists of Q<sub>10</sub>-Q<sub>12</sub> and Q<sub>14p</sub>, which is the translinear loop. From elementary small-signal circuit analysis,

the output voltage  $V_w$  of this circuit can be expressed as

$$V_w = \left( \frac{g_{m11} + \frac{g_{m11}g_{m12}}{g_{m10}}}{g_{m11} + g_{m14p}} \right) V_z + \frac{(g_{m11}g_{m12} - g_{m10}g_{m12})}{(g_{m10}g_{m14p} - g_{m11}g_{m12})} I_A. \quad (20)$$

We can form Eq. (20) to be

$$V_w = \gamma V_z + \varepsilon_b, \quad (21)$$

where  $\gamma = \frac{g_{m11} + \frac{g_{m11}g_{m12}}{g_{m10}}}{g_{m11} + g_{m14p}}$ ,  $\varepsilon_b = \left( \frac{g_{m11}g_{m12} - g_{m10}g_{m12}}{g_{m10}g_{m14p} - g_{m11}g_{m12}} \right) I_A$ .

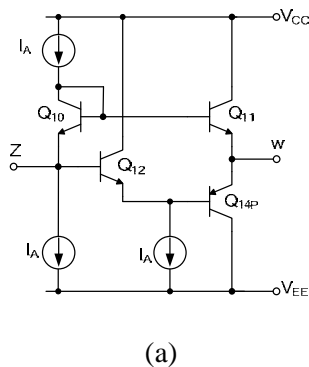
If transistors are well matched, which are  $g_{m10} = g_{m11}$  and  $g_{m12} = g_{m14p}$ , the parameters  $\beta \cong 1$  and  $\varepsilon_b = 0$ .

technology, any attempt to design wideband voltage follower will have to avoid MOS and pnp transistors in signal paths. The modified topology is an alternative solution to simulate the traditional class AB voltage follower in a standard BiCMOS technology, in which high frequency pnp bipolar junction transistor is not available.

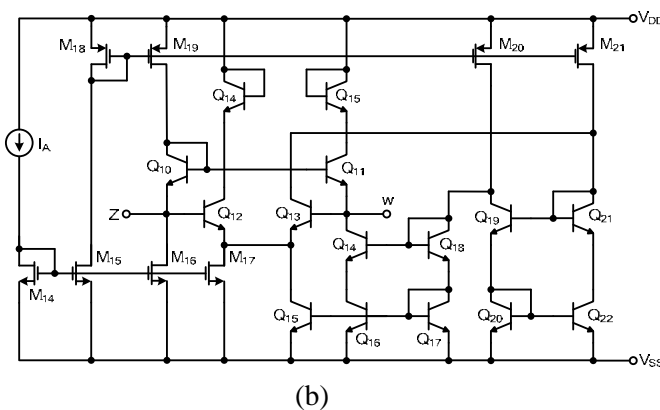
The output resistance looking into the w terminals is given by

$$r_w = \frac{V_T}{2I_A}. \quad (22)$$

The tunable output resistance of the modified circuit in Eq. (22) will be advantageous to implement low distortion voltage follower. Furthermore, this circuit includes a solution to simulate a pnp transistor in a translinear loop only using high speed npn transistors in signal paths ( $Q_9$ - $Q_{12}$ ). The translinear loop is DC biased by  $I_A$  using current mirrors ( $M_{14}$ - $M_{21}$ ).



(a)



(b)

Figure 6. Buffered amplifiers (a) basic topology (b) modified topology

However, due to the dissymmetry between npn and pnp transistors, this circuit exhibits a high output offset voltage. This problem should be solved by using a novel buffer amplifier, as depicted in Fig. 6(b) [30]. By means of a standard BiCMOS

### 3 Completed BiCMOS Current Controlled Current Feedback Amplifier

The proposed CC-CFA consists of two principal blocks: a second generation current controlled current conveyor and the modified voltage buffer, as explained. The proposed realization of the CC-CFA in BiCMOS technology is shown in Fig. 7. The second-generation current-controlled current conveyor as input stage consists of mixed translinear loops ( $Q_6$ - $Q_9$ ). The mixed loops are DC biased by  $I_B$  using current mirrors ( $M_1$ - $M_3$  and  $M_{10}$ - $M_{11}$ ). The x terminal resistance can be obtained by Eq. (12). The output z-terminal that generates the current of x terminal is realized using CMOS ( $M_4$ - $M_5$  and  $M_{12}$ - $M_{13}$ ).

The buffered amplifier is realized using BJTs and CMOS ( $Q_{10}$ - $Q_{22}$  and  $M_{14}$ - $M_{21}$ , respectively). It should be noted that only npn transistors are employed in this topology, which enables to achieve high frequency. A traditional high frequency class AB voltage follower, providing better linearity than its equivalent class A structure, could be implemented. Unfortunately, such technology requires complex and costly additional mask levels that constrain several companies to use only “standard” BiCMOS technology, which high frequency pnp bipolar junction transistor is not available [30].

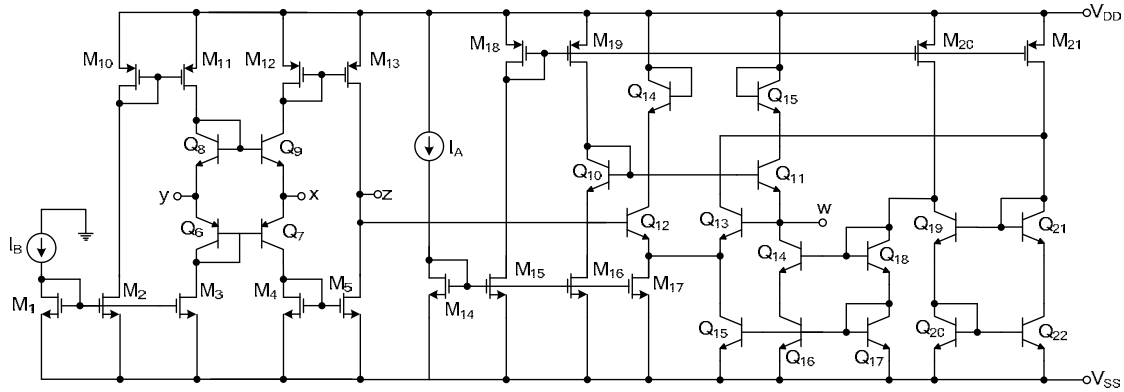


Figure 7. Proposed BiCMOS current controlled current feedback amplifier

## 4 Performance Analysis

### 4.1 Area mismatch

From Section 2.3, emitter area mismatch errors from transistors will mostly affect the operation of the BJT translinear circuit. For this reason, symmetrical and common centroid layout techniques should be employed for the transistors within the translinear loop. Good layout techniques will also help to reduce error due to process and thermal variations [31].

### 4.2 Finite output resistance

If the effects of base-width modulation are taken into account, the collector current of the transistor is changed to

$$I_C = I_s e^{(V_{BE}/V_T)} \left( 1 + \frac{V_{CE}}{V_A} \right). \quad (23)$$

Thus,

$$V_{BE} = V_T \ln [I_C / kI_s], \quad (24)$$

where  $k = 1 + V_{CE}/V_A$ . The Early voltage effect appears similar to an area mismatch.

The intrinsic input resistance when considering the finite output resistances of the transistors are modified to

$$R_x = \frac{V_T}{2I_B} + \frac{V_T}{I_x} \ln \left( \frac{I_{s8}k_8}{I_{s9}k_9} \right), \quad (25)$$

where  $k_i = 1 + V_{CEi}/V_{Ai}$ . From Eq. (25), it should be observed that the second term is the error originated from the Early voltage transistor

mismatch compared to Eq. (12). Consequently, keeping values of  $I_{s8}k_8$  and  $I_{s9}k_9$  to be equalled must be strictly considered [31].

### 4.3 Finite beta

Errors due to finite  $\beta_F$  occur frequently in BJT translinear circuits, since a bipolar transistor needs to be provided with base current. This base current is often taken directly from an input or output current source, and results in error terms in the circuit transfer function. These  $\beta_F$  errors are due to the circuit implementation, rather than being an inherent error in the translinear circuit principle. Any series base resistance ( $R_{bb}$ ) also affects the operation of a transistor circuit, since it ruins the exponential current-voltage relation in such

$$V_{BE} = V_T \ln \left( \frac{I_C}{I_s} \right) + \frac{I_C R_{bb}}{\beta_F}. \quad (26)$$

In similar, the intrinsic input resistance with considering the finite beta of the transistors are changed to

$$R_x = \frac{V_T}{2I_B} + \frac{I_B}{I_{in}} \left( \frac{R_{bb8}}{\beta_{F8}} - \frac{R_{bb9}}{\beta_{F9}} \right), \quad (27)$$

where  $\beta_{Fi}$  is the DC current gain of  $i^{\text{th}}$  transistor. From Eq. (27), it should be concluded that the second term is the error from finite beta transistor mismatch compared to Eq. (12). Thus, keeping ratio of  $R_{bb8}/\beta_{F8}$  and  $R_{bb9}/\beta_{F9}$  to be equalled is preferred. To simplify the analysis of translinear circuits, it is usual to neglect transistor base current. However, a full circuit analysis including base

current errors is often useful for comparing alternative circuit topologies [31].

TABLE I  
Dimensions of the MOS transistors

MOS Transistors	$W(\mu m) / L(\mu m)$
M1, M3	9/0.5
M2	8.5/0.5
M4-M5, M18-M19	5/0.5
M10-M13	15/0.5
M14-M17,	4/0.5
M20-M21	10/0.5

### 5 Simulation Results

To prove the performances of the proposed CC-CFA, the PSPICE simulation program was used for the examination. The PNP and NPN transistors employed in the proposed circuit in Fig. 7 were simulated by respectively using the parameters of the PR200N and NR200N bipolar transistors of ALA400 transistor array from AT&T [32] whereas the PMOS and NMOS transistors were simulated by using the parameters of a 0.35 $\mu m$  TSMC CMOS technology [33] with  $\pm 1.5V$  supply voltages. The aspect transistor ratios of PMOS and NMOS are listed in Table I. Fig. 8 depicts the parasitic resistance at x input terminal when  $I_B$  is varied, it is seen that the controllable parasitic resistance by adjusting  $I_B$  are about 1 $\mu A$ -300 $\mu A$  ranges.

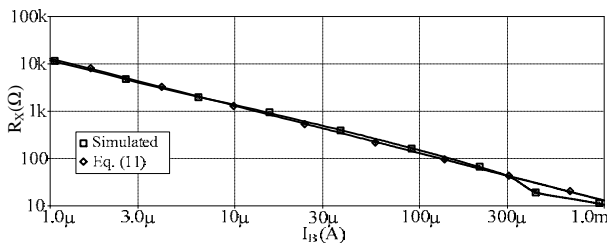


Figure 8. Parasitic resistance at x terminal relative to  $I_B$

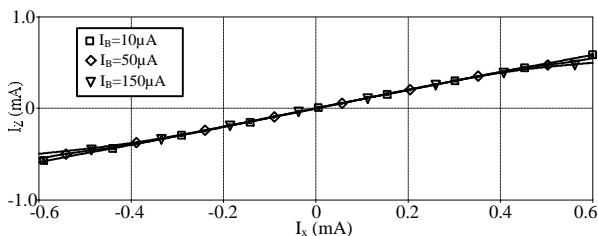
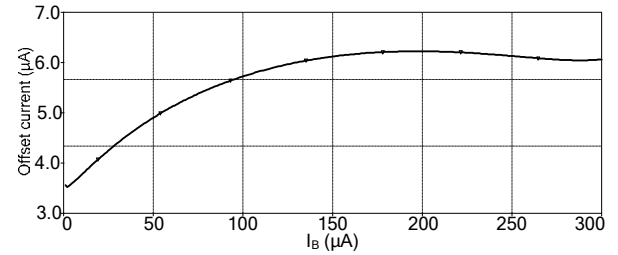
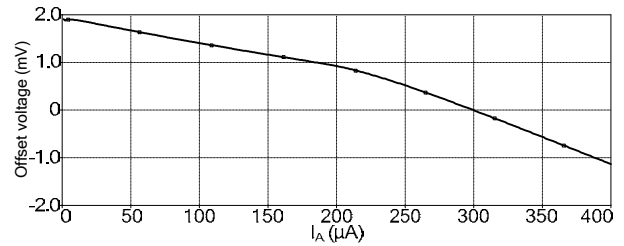


Figure 9. DC transfer characteristics of BiCMOS CC-CFA



(a)



(b)

Figure 10. Output offsets (a) offset current relative to  $I_B$  (b) offset voltage relative to  $I_A$

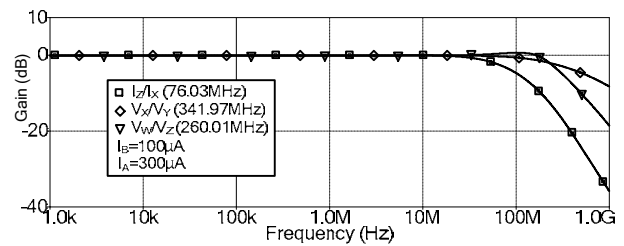


Figure 11. Frequency responses at output terminals of the CC-CFA

Fig. 9 displays DC transfer characteristic of the proposed BiCMOS CC-CFA, it is clearly seen that it is linear in range of  $-0.5mA \leq I_x \leq 0.5mA$  and can be adjusted. The offset current and voltage are shown in Fig. 10. When  $I_B$  and  $I_A$  are varied from 0–300 $\mu A$  and 0–400 $\mu A$ , we can found that the maximum output offset current and voltage are about 6.52 $\mu A$  and 1.91mV, respectively. There is seen that the proposed BiCMOS CC-CFA offers lower offset current and voltage. Moreover, the bandwidths of output terminals are investigated as shown in Fig. 11. Fig. 12(a) and (b) show the transient responses of the CC-CFA, these results confirm that the switching time delays of the CC-CFA at input stage and buffered amplifier are approximately 8ns and 2ns, respectively. The summarized properties of the proposed CC-CFA can be seen from Table. II.

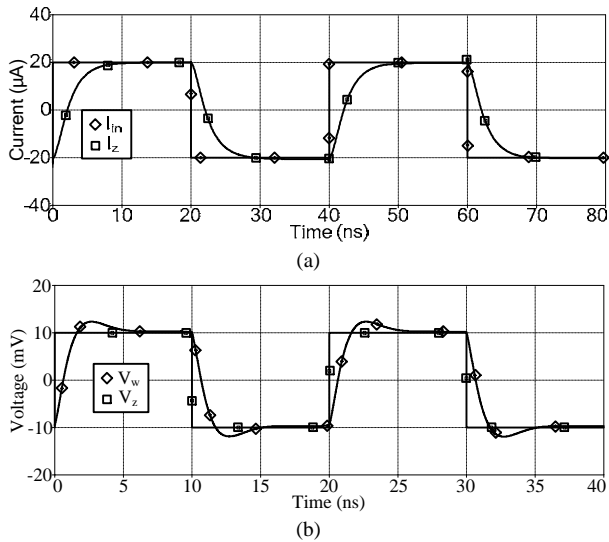


Figure 12. Transient responses to square wave inputs for (a) input stage (CCCII) (b) Buffered Amplifier

Table II: Conclusions of CC-CFA parameters

Parameters	Values
Power supply voltages	$\pm 1.5V$
Power consumption	4.16mW
3dB Bandwidth	76.03MHz( $I_z/I_x$ ), 341.97MHz( $V_x/V_y$ ), 260.01MHz( $V_w/V_z$ )
Input current linear range	-0.4mA to 0.4mA
$R_x$ range	53 $\Omega$ -12.62k $\Omega$
Input bias current range for controlling $R_x$	1 $\mu$ A-0.3mA
$R_z$	123.26k $\Omega$
$R_w$	207.87k $\Omega$
$R_y$	7.24M $\Omega$
Output offset current at $I_B=100 \mu A$	6.52 $\mu$ A
Output offset voltage at $I_A=300 \mu A$	1.91mV
Switching time delays	8ns (x to z), 2ns (z to w)
THD at z terminal	0.091% @ 10MHz
THD at w terminal	0.076% @ 10MHz

## 6 Application Examples

### 6.1 Current-mode multiplier/divider

The multiplier/divider based on the CC-CFA is shown in Fig. 13, which is modified from [34]. It employs only 2 CC-CFAs, where  $I_B$  and  $I_C$  are the bias current of CC-CFA1 and CC-CFA2, respectively. From routine analysis and using the CC-CFA properties, we will get

$$I_{z1} = I_A - i_{x1}, \quad (28)$$

and

$$I_{z1} = i_{x1}. \quad (29)$$

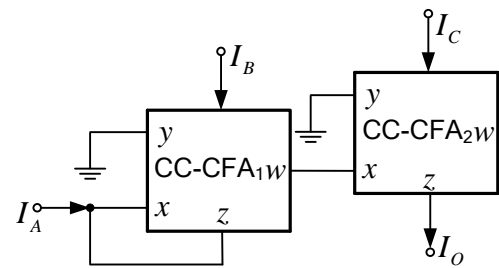


Figure 13. Multiplier/divider based on the CC-CFA

From Eqs. (28) and (29), it results

$$I_{z1} = I_A / 2. \quad (30)$$

The output voltage at  $W_1$  terminal can be found to be

$$V_{w1} = I_{z1} R_{x1} = I_A \frac{R_{x1}}{2}. \quad (31)$$

The output current can be obtained by

$$I_O = -\frac{V_{w1}}{R_{x2}} = -I_A \frac{R_{x1}}{2R_{x2}}. \quad (32)$$

If  $R_{x1} = V_T / 2I_B$  and  $R_{x2} = V_T / 2I_C$ . The output current in Eq. (32) will be changed to

$$I_O = -\frac{I_A I_C}{2I_B}. \quad (33)$$

From Eq. (33), it is seen that  $I_O$  is a result of either, multiplying of  $I_A$  and  $I_C$ , or dividing of  $I_A$  and  $I_B$ . Due to being a positive value of  $I_B$  and  $I_C$ , the proposed circuit can be a 2 quadrant multiplier/divider. In addition, if  $I_A$  is an input



current, the proposed circuit can work as a current amplifier, while the magnitude of output current can be controlled by  $I_B$  and  $I_C$ . Furthermore, the output current is theoretically temperature-insensitive owing to no term of  $V_T$ .

For non-ideal case, the  $V_x$ ,  $I_z$  and  $V_w$  of CC-CFA can be respectively characterized by

$$V_x = \beta V_y + I_x R_x, \quad I_z = \alpha I_x + \varepsilon_z, \quad (34)$$

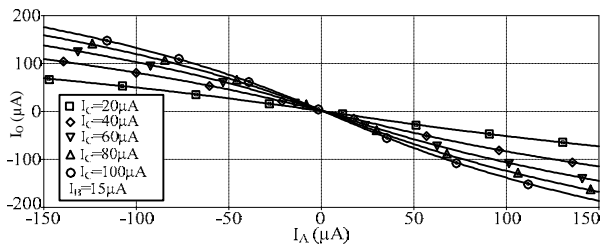
and

$$V_w = \gamma V_z + \varepsilon_b, \quad (35)$$

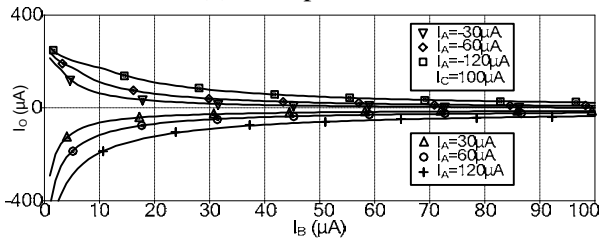
where  $\alpha$ ,  $\beta$  and  $\gamma$  are transferred error values deviated from one.  $\varepsilon_z$  and  $\varepsilon_b$  are the offset current and voltage at z, and w terminals, respectively. In the case of non-ideal and brief considerations, the  $I_o$  is subsequently changed to

$$I_o = \frac{I_A I_C}{I_B} \alpha_2 \gamma_1 \frac{\alpha_1}{1 + \alpha_1} + \alpha_2 \gamma_1 \frac{I_C}{I_B} \frac{\varepsilon_{z1}}{1 + \alpha_1} + \frac{\varepsilon_{b1} 2 I_C}{\alpha_2 V_T} + \varepsilon_{z2}. \quad (36)$$

From Eq. (36), we can see that the last three terms are offset currents. Consequently, to reduce the offset currents, the CC-CFA should be carefully designed to achieve these errors as low as possible. In addition, for the first term, these errors affect the magnitude of the output current. As a result, the magnitude output slightly depends on temperature due to temperature dependence of these errors. Thus, good design of the CC-CFA should be strictly considered to alleviate the effects.

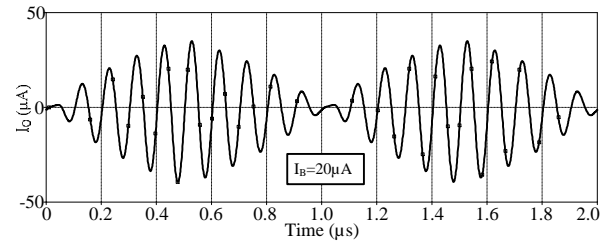


(a) Multiplication

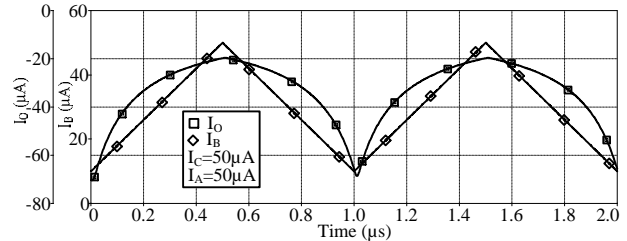


(b) Division

Figure 14. Static characteristics of the multiplier/divider in Fig. 13

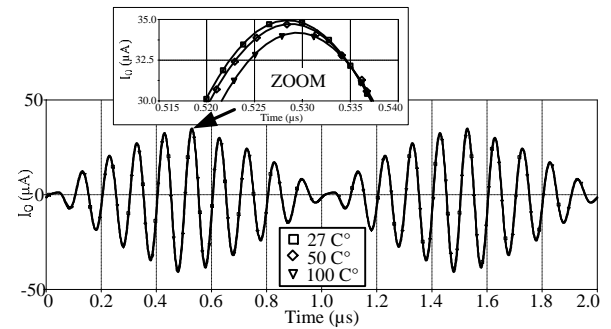


(a) Multiplication

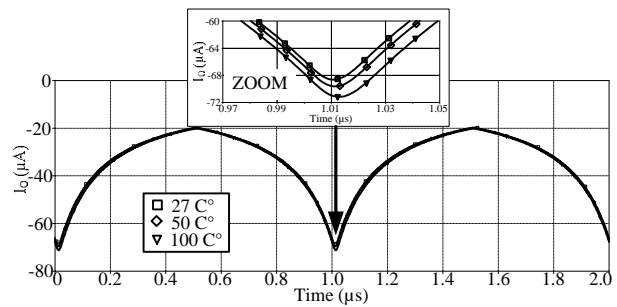


(b) Division

Figure 15. Transient responses of the multiplier/divider



(a) Multiplication



(b) Division

Figure 16. Output current deviations due to temperature variations of the multiplier/divider

Fig. 14(a) and (b) show the DC response characteristics of multiplication, where  $I_B = 20 \mu A$  and division of the proposed circuit, where  $I_C = 100 \mu A$ , respectively.

Fig. 15(a) shows the transient responses of multiplication, where  $I_A$  and  $I_C$  were set to be a sinusoidal signal of  $50 \mu A_{p-p}$  at 10MHz and a

triangular signal  $50\mu A_p$  at 1MHz frequency, respectively. Fig. 15(b) shows the division of the proposed circuit, where  $I_A$  and  $I_C$  were set to be  $50\mu A$  and  $I_B$  was a triangular signal with a frequency of 1MHz. Furthermore, the claimed temperature-insensitivities of the proposed circuit are confirmed by the results of Fig. 16, depicting transient responses.

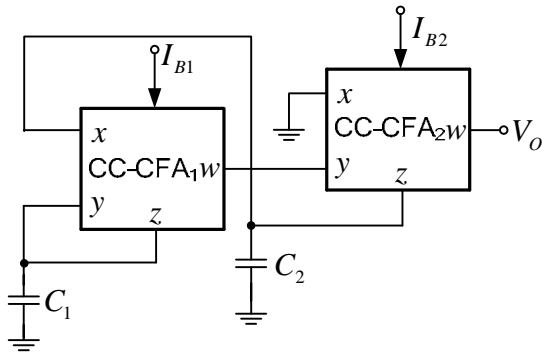


Figure 17. Oscillator based on the CC-CFA

### 6.2 Oscillator

The second application of proposed CC-CFA is an oscillator, shown in Fig. 17, which is modified from [35]. It consists of 2 CC-CFAs and 2 grounded capacitors. Considering the circuit in Fig. 17, and using the CC-CFA properties, yields the characteristic equation of this circuit as

$$s^2 C_1 C_2 R_{x1} + s(C_1 - C_2) + R_{x2} = 0. \quad (37)$$

From Eq. (37), it can be seen that the proposed circuit can be set to be an oscillator if

$$C_1 = C_2. \quad (38)$$

Eq. (38) is called the condition of oscillation, thus the characteristic equation of the system becomes

$$s^2 + \frac{g_m}{C_1 C_2 R_x} = 0. \quad (39)$$

From Eq. (39), the oscillation frequency of this system can be obtained by

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_{x1} R_{x2}}}. \quad (40)$$

It can be seen that, from Eq. (40), the oscillation frequency ( $\omega_0$ ) can be controlled by the bias currents.

If non-ideal characteristics of the CC-CFA as explained in Eqs. (34) and (35) are considered and assuming that no offset current and voltage occur in the CC-CFA, the system characteristic equation can be written as

$$s^2 C_1 C_2 R_{x1} R_{x2} + s(C_1 - \alpha_1 \beta_1 C_2) + \alpha_1 \alpha_2 \gamma_1 \gamma_2 \beta_2 = 0. \quad (41)$$

In this case the oscillation condition and oscillation frequency are respectively changed to be

$$C_1 = \alpha_1 \beta_1 C_2, \quad (42)$$

and

$$\omega_0 = \sqrt{\frac{\alpha_1 \alpha_2 \gamma_1 \gamma_2 \beta_2}{C_1 C_2 R_{x1} R_{x2}}}. \quad (43)$$

The confirmed performances of the oscillator can be seen in Fig. 18 and 19, showing the responses of the oscillator with bias currents, where  $I_{B1}$  and  $I_{B2}$  are equally set to  $100\mu A$ . Fig. 20 shows the simulated output spectrum, where the total harmonic distortion (THD) is about 2.68%.

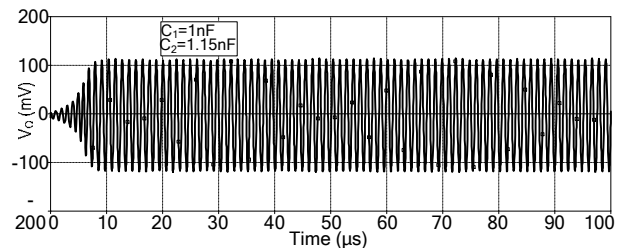


Figure 18. The simulation result of output waveform during initial state

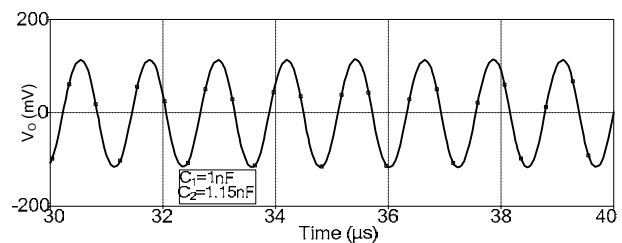


Figure 19. The simulation result of voltage waveform of oscillator in Fig. 17

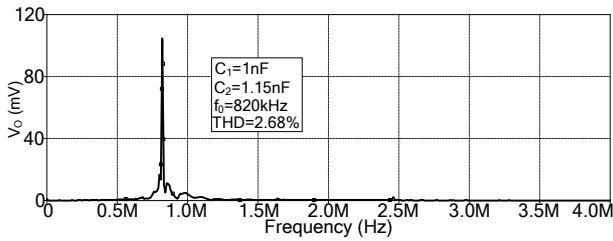


Figure 20. The simulation result of output spectrum

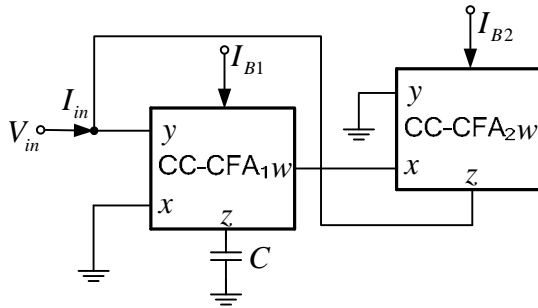


Figure 21. Grounded inductance simulator based on the CC-CFAs

**6.3 Grounded inductance simulator**

The grounded inductance simulator based on the CC-CFA is shown in Fig. 21, which is modified from [22], it employs 2 CC-CFAs and 1 grounded capacitor, which contrasts to ordinarily proposed circuits [36-37] in such that it consumes a few number of elements. From routine analysis and by using the CC-CFA properties, the input impedance of the circuit can be written as

$$Z_{in} = \frac{V_{in}}{I_{in}} = sCR_{x1}R_{x2} \tag{44}$$

From Eq. (44), it is obvious that the circuit shown in Fig. 21 performs a grounded inductance with a value

$$L_{eq} = CR_{x1}R_{x2} = \frac{CV_T^2}{4I_{B1}I_{B2}} \tag{45}$$

From Eq. (45), the inductance value  $L_{eq}$  can be adjusted electronically by either  $I_{B1}$  or  $I_{B2}$ .

If non-ideal characteristics of the CC-CFA as explained in Eqs. (34) and (35) are considered and assuming that no offset current and voltage occur in the CC-CFA, the input impedance can be written as

$$Z_{in} = \frac{sCR_{x1}R_{x2}}{\alpha_1\beta_1\gamma_1\alpha_2} = \frac{sCV_T^2}{\alpha_1\beta_1\gamma_1\alpha_2 4I_{B1}I_{B2}} \tag{46}$$

From Eq. (46), for non-ideal consideration, these error parameters will effect to the inductance value. The impedance and phase of the simulator relative to frequency are also shown in Fig. 22, where  $C=1nF$ ,  $I_{B1}=I_{B2}=100\mu A$ . Fig. 23 shows impedance values relative to frequency of the simulator for different  $I_B$ . To illustrate an application of the grounded inductance simulator, it is employed in an RLC parallel circuit shown in Fig. 24, where  $I_{in} = 20\mu A$ . The frequency responses of  $I_{LP}$ ,  $I_{HP}$  and  $I_{BP}$  are shown in Fig. 25.

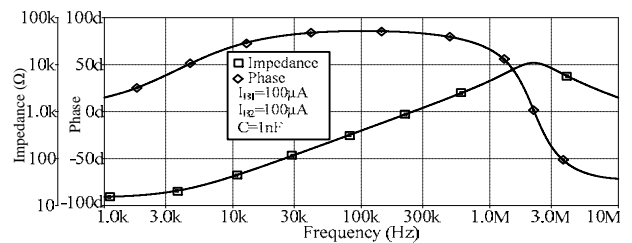


Figure 22. The impedance and phase relative to frequency of the grounded inductance simulator in Fig. 21

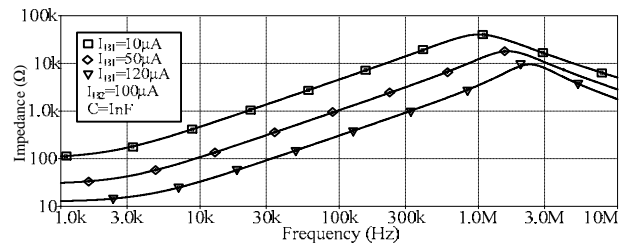


Figure 23. The impedance values relative to frequency of the simulators for different  $I_{B1}$

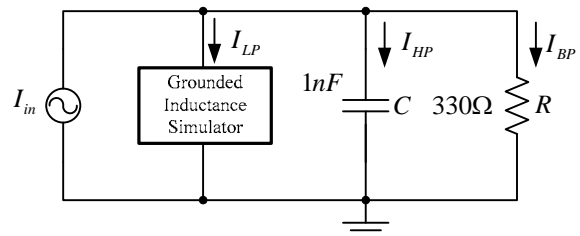


Figure 24. Parallels RLC resonant circuit

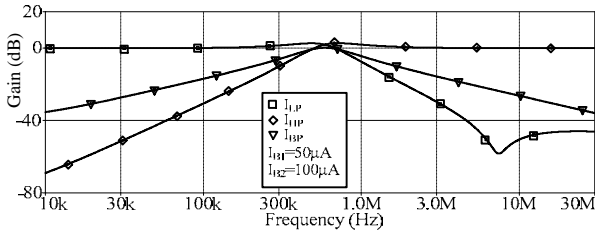


Figure 25. Simulated current characteristics of the resonant circuit in Fig. 24

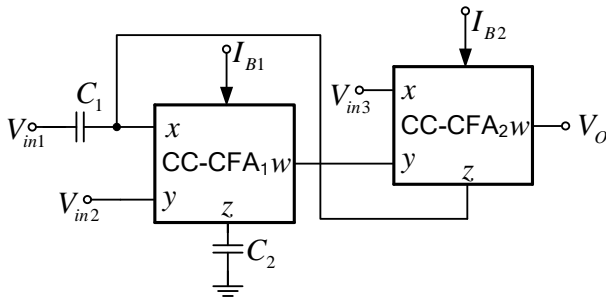


Figure 26. Voltage-mode universal biquad filter based on the CC-CFAs

**6.4 Voltage-mode biquad filter**

The voltage-mode biquad filter based on the CC-CFAs is shown in Fig. 26. By straightforward analysis of the circuit in Fig. 26, the output voltage of the network can be obtained as

$$V_o = \frac{V_{in1}s^2C_1C_2R_{x1}R_{x2} + V_{in2}(1 + sC_2R_{x2}) - V_{in3}sC_2R_{x1}}{s^2C_1C_2R_{x1}R_{x2} + sC_2R_{x2} + 1} \quad (47)$$

From Eq. (47), the magnitudes of input voltages  $V_{in1}$ ,  $V_{in2}$ , and  $V_{in3}$  are chosen as shown in Table. III to obtain a standard function of the 2<sup>nd</sup> order network. From Eq. (47), the pole frequency ( $\omega_0$ ) and quality factor ( $Q_0$ ) of each filter response can be respectively expressed as

$$\omega_0 = \sqrt{\frac{1}{C_1C_2R_{x1}R_{x2}}} \quad (48)$$

and

$$Q_0 = \sqrt{\frac{C_1R_{x1}}{C_2R_{x2}}} \quad (49)$$

Substituting intrinsic resistance as depicted in Eq. (12), it yields

$$\omega_0 = \frac{2}{V_T} \sqrt{\frac{I_{B1}I_{B2}}{C_1C_2}} \quad (50)$$

and

$$Q_0 = \sqrt{\frac{C_1I_{B2}}{C_2I_{B1}}} \quad (51)$$

From Eqs. (50) and (51), by maintaining the ratio  $I_{B1}$  and  $I_{B2}$  to be constant, it can be remarked that the pole frequency can be adjusted by  $I_{B1}$  and  $I_{B2}$  without affecting the quality factor.

TABLE III

The  $V_{in1}$ ,  $V_{in2}$  and  $V_{in3}$  values selection for each filter function response

Filter Responses	Input selections		
	$V_{in1}$	$V_{in2}$	$V_{in3}$
$V_o$			
BP	0	0	1
HP	1	0	0
BR ( $R_{x1}=R_{x2}$ )	1	1	1
AP ( $R_{x1}=R_{x2}$ )	1	1	2
LP ( $R_{x1}=R_{x2}$ )	0	1	1

If non-ideal characteristics of the CC-CFA as explained in Eqs. (34) and (35) are considered and assuming that no offset current and voltage occur in the CC-CFA, the output voltage can be written as

$$V_o = \frac{\gamma_2s^2C_1C_2R_{x1}R_{x2}V_{in1} + (\beta_1\beta_2\gamma_1\gamma_2\alpha_1\alpha_2 + \beta_1\gamma_2sC_2R_{x2})V_{in2} - \alpha_2\gamma_2sC_1R_{x1}V_{in3}}{s^2C_1C_2R_{x1}R_{x2} + sC_2R_{x2} + \beta_2\gamma_1\alpha_1\alpha_2} \quad (52)$$

In this case, the  $\omega_0$  and  $Q_0$  are changed to

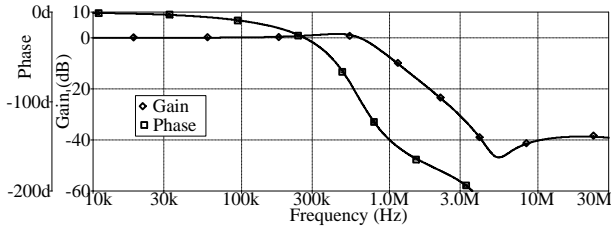
$$\omega_0 = \sqrt{\frac{\alpha_1\alpha_2\beta_2\gamma_1}{C_1C_2R_{x1}R_{x2}}} \quad (53)$$

and

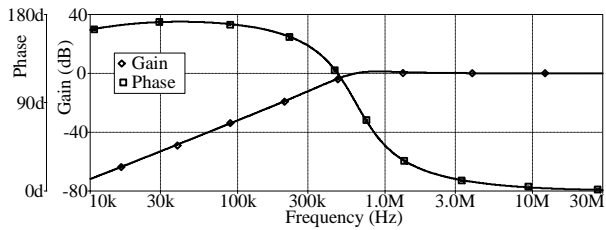
$$Q_0 = \sqrt{\frac{\alpha_1\alpha_2\beta_2\gamma_1C_1R_{x1}}{C_2R_{x2}}} \quad (54)$$

To prove the performances of the voltage-mode filter, the PSPICE simulation program was used for the examination, where  $I_{B1}=I_{B2}=50\mu A$  and  $C_1=C_2=1nF$ . The results shown in Fig. 27 are the gain and phase responses of the voltage-mode filter obtained from Fig. 26. This clearly shows that the circuit can provide low-pass, high-pass, band-pass, band-reject, and all-pass functions depending on digital selection [35] as shown in Table III, without modifying circuit topology. Fig. 28 shows gain

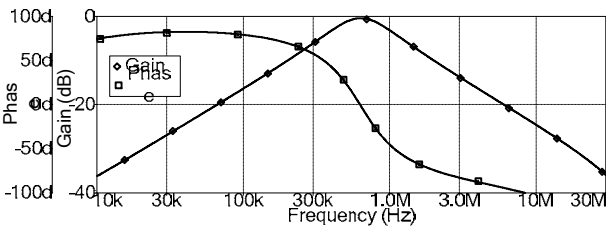
responses of band-pass function where  $I_{B1}$  and  $I_{B2}$  are equally set to keep the ratio to be constant and changed for several values. It is found that pole frequency can be adjusted without affecting the quality factor, as earlier explained.



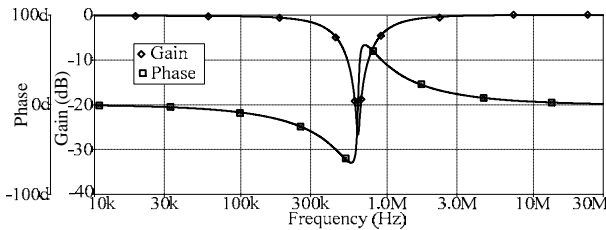
(a)



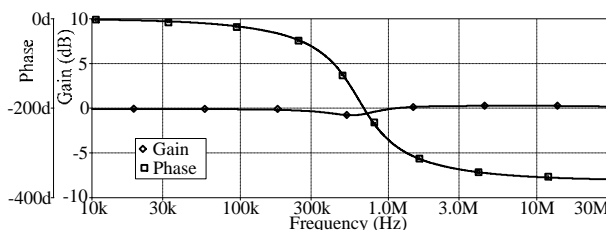
(b)



(c)



(d)



(e)

Figure 27. Gain and phase responses of the voltage-mode biquad filter in Fig. 24 for different responses (a) LP (b) HP (c) BP (d) BR (e) AP

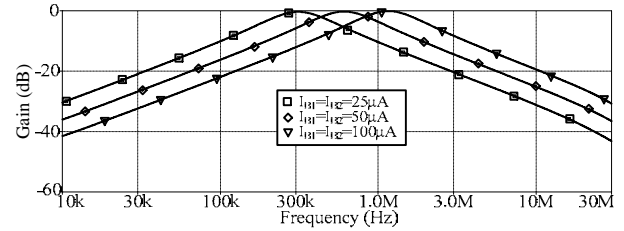


Figure 28. Band-pass responses for different values of  $I_{B1}$  and  $I_{B2}$  with keeping their ratios constant

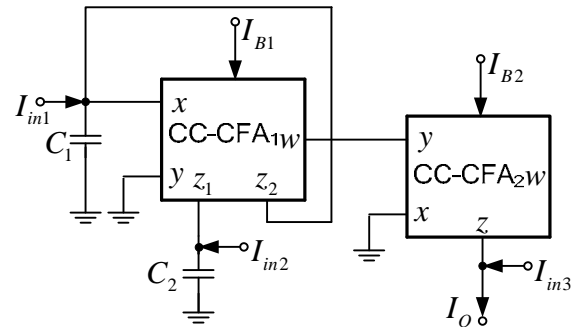


Figure 29. Current-mode universal biquad filter based on the CC-CFA

### 6.5 Current-mode biquad filter

The fifth application of the proposed CC-CFA is a current-mode biquad filter shown in Fig. 29. It employs only 2 active elements and 2 grounded capacitors, which is easy to fabricate, unlike the previous circuits [38-39]. The CC-CFA in Fig. 29 is slightly modified from the proposed CC-CFA in Fig. 7 by using multiple-output CC-CFA which can be achieved by using the current mirrors to copy current from the  $z_1$  to the  $z_2$  terminal to extend the usability of CC-CFA. Straightforward analysis of the circuit in Fig. 29 and using CC-CFA properties in section 2, the output current of the network can be obtained as

$$I_o = \frac{I_{in1}sC_2R_{x2} + I_{in2} - I_{in3}(s^2C_1C_2R_{x1}R_{x2} + sC_2R_{x2} + 1)}{s^2C_1C_2R_{x1}R_{x2} + sC_2R_{x2} + 1} \quad (55)$$

TABLE IV

The  $I_{in1}$ ,  $I_{in2}$  and  $I_{in3}$  value selections for each filter function response

Filter Responses	Input selections		
$I_o$	$I_{in1}$	$I_{in2}$	$I_{in3}$
BP	1	0	0
HP	1	1	1
BR	1	0	1
AP	2	0	1
LP	0	1	0

From Eq. (55), the magnitudes of input currents  $I_{in1}$ ,  $I_{in2}$ , and  $I_{in3}$  can be chosen as in Table. IV to obtain a standard function of the 2<sup>nd</sup> order network. The circuit for selection can be seen in [40]. Moreover,  $I_{in1}$  must be double of  $I_{in3}$  in the case of AP. So to achieve this condition, the current amplifier which has gain of 2 is required. From Eq. (55), the pole frequency ( $\omega_0$ ) and quality factor ( $Q_0$ ) of each filter response can be respectively expressed as

$$\omega_0 = \sqrt{\frac{1}{C_1 C_2 R_{x1} R_{x2}}}, \quad (56)$$

and

$$Q_0 = \sqrt{\frac{C_1 R_{x1}}{C_2 R_{x2}}}. \quad (57)$$

Substituting intrinsic resistance as depicted in Eq. (12), it yields

$$\omega_0 = \frac{2}{V_T} \sqrt{\frac{I_{B1} I_{B2}}{C_1 C_2}}, \quad (58)$$

and

$$Q_0 = \sqrt{\frac{C_1 I_{B2}}{C_2 I_{B1}}}. \quad (59)$$

If non-ideal characteristics of the CC-CFA as explained in Eqs. (34) and (35) are considered and assuming that no offset current and voltage occur in the CC-CFA, the output current in Fig. 29 can be written as

$$I_o = \frac{I_{in1} s C_2 R_{x2} \alpha_{12} + I_{in2} \alpha_2 \beta_2 \gamma_1 \alpha_{12} - I_{in3} D(s)}{D(s)}, \quad (60)$$

where  $D(s) = s^2 C_1 C_2 R_{x1} R_{x2} + s C_2 R_{x2} + \beta_2 \gamma_1 \alpha_{11} \alpha_{12} \alpha_2$ .

In this case, the  $\omega_0$  and  $Q_0$  are changed to

$$\omega_0 = \sqrt{\frac{\beta_2 \gamma_1 \alpha_{11} \alpha_{12} \alpha_2}{C_1 C_2 R_{x1} R_{x2}}}, \quad (61)$$

and

$$Q_0 = \sqrt{\frac{\beta_2 \gamma_1 \alpha_{11} \alpha_{12} \alpha_2 C_1 R_{x1}}{C_2 R_{x2}}}. \quad (62)$$

To prove the performances of the current-mode filter, the PSPICE simulation program was used with same conditions to the voltage-mode filter, where  $I_{B1} = I_{B2} = 100\mu A$  and  $C_1 = C_2 = 1nF$ . The results shown in Fig. 30 are the gain and phase responses of the current-mode filter obtained from Fig. 29. This clearly shows that the circuit can provide low-

pass, high-pass, band-pass, band-reject, and all-pass functions depending on digital selection as shown in Table IV, without modifying circuit topology. Fig. 31 shows gain responses of band-pass function where  $I_{B1}$  and  $I_{B2}$  are equally set to keep the ratio to be constant and changed for several values. It is found that pole frequency can be adjusted without affecting the quality factor.

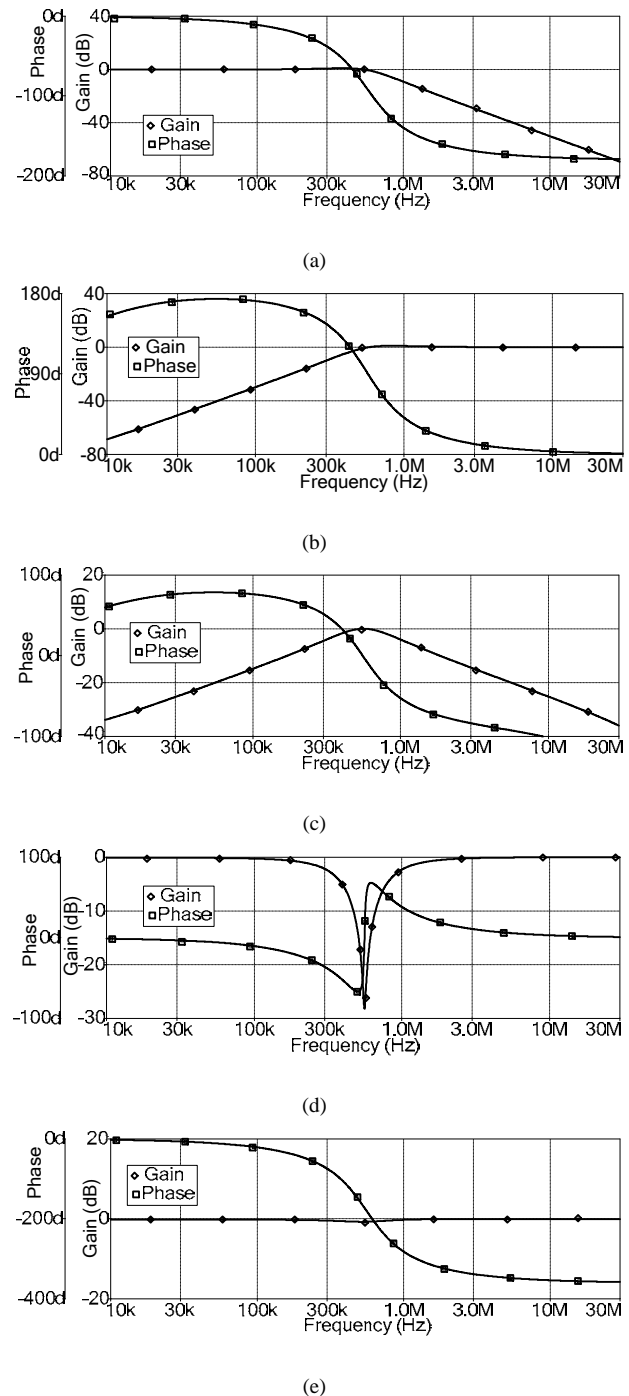


Figure 30. Gain and phase responses of the current-mode biquad filter in Fig. 29 for different responses (a) LP (b) HP (c) BP (d) BR (e) AP

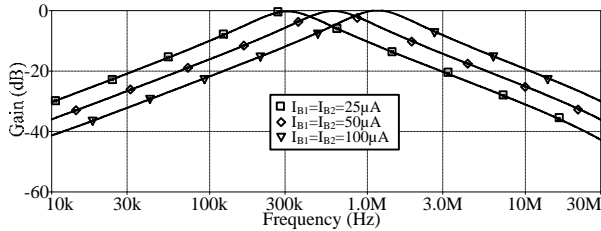


Figure 31. Band-pass responses for different values of  $I_{B1}$  and  $I_{B2}$  with keeping their ratios constant

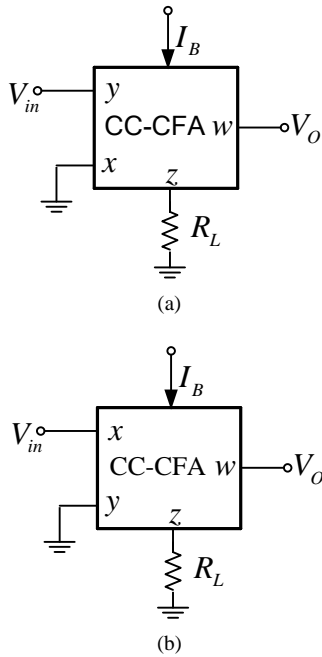


Figure 32. (a) Inverting Amplifier (b) Non-Inverting Amplifier

**6.6 Voltage Amplifiers**

The voltage non-inverting and inverting amplifiers based on the CC-CFA are shown in Fig. 32(a) and (b), respectively. By straightforward analysis of the circuit in Fig. 32, the output voltages of the circuits can be respectively obtained as

$$V_o = \frac{R_L}{R_x} V_{in}, \tag{63}$$

and

$$V_o = -\frac{R_L}{R_x} V_{in}. \tag{64}$$

Substituting intrinsic resistance, as depicted in Eq. (12), it yields

$$V_o = \frac{2I_B R_L}{V_T} V_{in}, \tag{65}$$

for non-inverting configuration and

$$V_o = -\frac{2I_B R_L}{V_T} V_{in}, \tag{66}$$

for inverting configuration. It can be seen from Eqs. (65) and (66) that the circuits in Fig. 32(a) and (b) can perform as voltage amplifiers whose voltage gain can be electronically controlled via control current  $I_B$ .

If non-ideal characteristics of the CC-CFA as explained in Eqs. (34) and (35) are considered, the output voltages can be rewritten as

$$V_o = \alpha\beta\gamma R_L \frac{V_{in}}{R_x} + \gamma R_L \varepsilon_z + \varepsilon_b, \tag{67}$$

for non-inverting configuration and

$$V_o = -\left( \alpha\gamma R_L \frac{V_{in}}{R_x} + \gamma R_L \varepsilon_z + \varepsilon_b \right), \tag{68}$$

for inverting configuration, the last two terms of Eqs. (67) and (68) are offset voltages. Consequently, to reduce the offset voltages, the CC-CFA should be carefully designed to achieve these errors as low as possible. In addition, for the first term, these errors affect the magnitude of the output voltage.

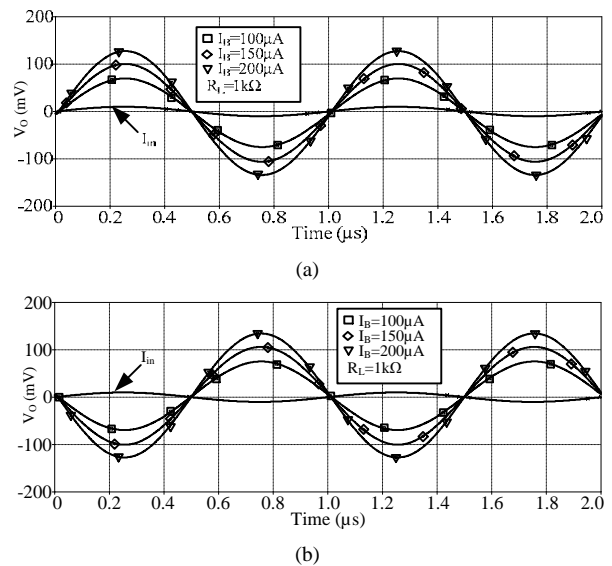


Figure 33. Output voltages relative to input bias current (a) non-inverting amplifier (b) inverting amplifier

Fig. 33(a) and (b) display the output voltages as a function of the input bias current  $I_B$  whereas  $V_{in}=10mV$ . These figures prove that the magnitude of the output voltage can be easily/electronically

controlled in accordance with the theoretical anticipations, as depicted in Eqs. (65) and (66).

## 7 Conclusion

The modified version of building block, called CC-CFA, has been introduced via this paper. The realization has been done by a BiCMOS technology to reduce offset errors at the outputs. The usabilitys have been proven by the simulation and application examples. They consume a few numbers of components, while electronic controllability is still available, which differs from other recently proposed elements. The proposed CC-CFA provides low distortions, low output offset errors and wide bandwidth of frequency responses. It is very appropriate to realize in commercially-purposed integrated circuit for employing in instrumentation/measurement systems, battery-powered, portable electronic equipments or wireless communication systems. Our future work is to find more applications of the CC-CFA, emphasizing on the current or voltage-mode signal processing circuits such as signal generator, rectifier, etc.

## Acknowledgement

This work was supported in part by a grant from King Mongkut's University of Technology North Bangkok (KMUTNB).

### References:

- [1] C. Toumazou, F. J. Lidgey, and D. G. Haigh, *Analogue IC design: the current-mode approach*, London: Peter Peregrinus, 1990.
- [2] D. R. Bhaskar, V. K. Sharma, M. Monis and S. M. I. Rizvi, "New current-mode universal biquad filter," *Microelectronics Journal*, vol. 30, pp. 837-839, 1999.
- [3] A. Sedra and K. C. Smith, "A second-generation current conveyor and its applications," *IEEE Transactions on Circuits Theory*, vol. 17, pp. 132-134, 1970
- [4] C. Acar and S. Ozoguz, "A new versatile building block: current differencing buffered amplifier suitable for analog signal processing filters," *Microelectronics Journal*, vol. 30, pp. 157-160, 1999.
- [5] D. Biolek, "CDTA-Building Block for Current-Mode Analog Signal Processing," *Proceedings of the European conference on circuit theory and design 2003 - ECCTD'03*, Krakow, Poland, pp. 397-400, 2003.
- [6] Comlinear Corp., "Designer's guide for 200 series op amp," *Application note 200-1*, 4800 Wheaton Drive, Ft. Collins, CO 80525, 1984.
- [7] Analog Devices: "Linear products data book." Norwood MA, 1990.
- [8] A. Fabre, "Insensitive voltage mode and current mode filters from commercially available transimpedance opamps," *Proc. IEE (G)*, vol. 140, pp. 319-321, 1993.
- [9] S.-I. Liu and Y.-S. Hwang, "Realization of R-L and C-D impedances using a current-feedback amplifier and its applications," *Electronics Letters*, vol. 30, no. 5, pp. 380-381, 1994.
- [10] C.-M. Chang, C.-S. Hwang, and S.-H. Tu, "Voltage-mode notch, lowpass and bandpass filter using current-feedback amplifiers," *Electronics Letters*, vol. 30, no. 24, pp. 2022-2023, 1994.
- [11] M. T. Abuelma'atti and S. M. Al-shahrani, "New universal filter using two current-feedback amplifiers," *International Journal of Electronics*, vol. 80, pp. 753-756, 1996.
- [12] J-W. Horng and M-H. Lee., "High input impedance voltage-mode lowpass, bandpass and highpass filter using current-feedback amplifiers," *Electronics Letters*, vol. 33, no. 11, pp. 947-948, 1997.
- [13] N. A. Shah nad M. A. Malik, "Voltage/current-mode universal filter using FTFN and CFA," *Analog integrated circuits and signal processing*, vol. 45, pp. 197-203, 2005.
- [14] S. Selvanayagam and F.J. Lidgey, "Wide bandwidth CMOS current feedback op amp for inverting amplifier applications," *IEE Colloquium, Modelling and Techniques, Wideband Circuits*, pp. 7/1-7/4, 1996.
- [15] S. I. Liu, C. C. Chang, and D. S. Wu, "Active-R sinusoidal oscillators using CFOA pole," *International Journal of Electronics*, vol. 77, pp. 1035-1042, 1994.
- [16] D. S. Wu, S. I. Liu, Y. S. Hwang, and Y. P. Wu, "Multiphase sinusoidal oscillator using CFOA pole," *IEE Proc., Circuits, Devices Systems*, vol.142, pp. 37-40, 1995.
- [17] M. T. Abuelma'atti and S. M. Al-Shahrani, "A novel low-component count single-element-controlled oscillator using CFOA pole," *International Journal of Electronics*, vol. 80, pp. 747-753, 1996.
- [18] R. Senani and V. K. Singh, "Novel single resistance controlled oscillator configuration using current feedback amplifiers," *IEEE*



- Trans. Circuits Syst. I*, vol. 43, pp. 698–700, 1996.
- [19] S. S. Gupta, D. R. Bhaskar, R. Senani, “New voltage controlled oscillators using CFOAs,” *International Journal of Electronics and Communications*, available online, 2008.
- [20] S. Natarajan, “Inductance simulation using modern current feedback amplifiers (CFAs),” *Proceedings of the Thirty-Seventh Southeastern Symposium on System Theory, 2005, SSST'05*, pp. 60–64, 2005.
- [21] T. K. Bandyopadhyay, R. K. Nagaria, S. K. Sanyal and R. Nandi, “Lossless inductor using current feedback amplifier,” *International Symposium on Signals, Circuits and Systems, 2005. ISSCS 2005*, vol. 2, pp. 689–692, 2005.
- [22] A. Fabre, “Gyrator implementation from commercially available transimpedance operational amplifiers,” *Electronics Letters*, vol. 28, pp. 263–264, 1992.
- [23] M. Abuelma'atti and S. al-Shahrani, “New CFOA-based triangular/square wave generator,” *International Journal of Electronics*, vol. 84, pp. 583–588, 1998.
- [24] M. Weng, J. R. Lai and M. H. Lee, “Realization of  $n$ -th-order series impedance function using only  $(n-1)$  current-feedback amplifiers,” *International Journal of Electronics*, vol. 87, no. 1, p. 63–69, 2000.
- [25] H. Z. Abouda and A. Fabre, “New high-value floating controlled resistor in CMOS technology,” *IEEE Transaction on Instrumentation and Measurement*, vol. 51, no. 7, pp. 1017–1020, 2006.
- [26] M. Siripruchyanun and W. Jaikla, “Electronically Controllable Current-Mode Universal Biquad Filter Using Single DO-CCCDTA,” *Circuits Systems and Signal Processing*, vol. 27, pp. 113–122, 2008.
- [27] P. R. Gray, P. J. Hurst, S. H. Lewis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, New York: John Wiley & Sons, 2001.
- [28] A. Fabre, “Dual translinear voltage/current convertor,” *Electronics Letters*, vol. 19, pp. 1030–1031, 1983.
- [29] F. Seguin and A. Fabre, “2 GHz controlled current conveyor in standard 0.8 $\mu$ m BICMOS technology,” *Electronics Letters*, vol. 37, pp. 329–330, 2001.
- [30] H. Barthélemy and E. Kussener, “High speed voltage follower for standard BiCMOS technology,” *IEEE Transaction on Circuits and Systems*, vol. 48, pp. 727–732, 2001.
- [31] A. Grebene, *Bipolar and MOS analog integrated circuit design*, John Wiley & Sons, Inc., New York, 1984.
- [32] D. R. Frey “Log-domain filtering: an approach to current-mode filtering,” *IEE Proc. Circuit Devices Syst.*, vol. 140, pp. 406–416, 1993.
- [33] E. Yuce, S. Tokat, A. Kızılkaya and O. Cicekoglu, “CCII-based PID controllers employing grounded passive components,” *International Journal of Electronics and Communication*, vol. 60, no. 5, pp. 399–403, 2006.
- [34] M. T. Abuelma'atti and M.A. Al Qahtani, “A current mode current controlled current conveyor based analogue multiplier/divider,” *International Journal of Electronics*, vol. 85, pp. 71–77, 1998.
- [35] D. R. Bhaskar and Raj Senani, “New CFOA-Based single-element-controlled sinusoidal oscillators,” *IEEE Transaction on Instrument and Measurement*, vol. 55, pp. 2004–2221, 2006.
- [36] I. A. Khan and M. H. Zaidi, “A novel ideal floating inductor using translinear conveyors,” *Active and Passive Electronic Components*, vol. 26, no. 2, pp. 87–89, 2003.
- [37] J. S. Pena-Finol and J. A. Connelly, “Novel lossless floating immittance simulator employing only two FTFNs,” *Analog Integrated Circuits and Signal Processing*, vol. 29, no. 3, pp. 233–235, 2001.
- [38] W. Tangsrirat, “Low-voltage digitally programmable current-mode universal biquadratic filter,” *International Journal of Electronics and Communication*, vol. 62, pp. 97–103, 2008.
- [39] M. A. Ibrahim, S. Minaei, and H. A. Kuntman “A 22.5 MHz current-mode KHN-biquad using differential voltage current conveyor and grounded passive elements,” *International Journal of Electronics and Communication*, vol. 59, pp. 311–318, 2005.
- [40] C. L. Hou, C. C. Huang, Y. S. Lan, J. J. Shaw and C. M. Chang “Current-mode and voltage-mode universal biquads using a single current-feedback amplifier,” *International Journal of Electronics*, vol. 86, no. 8, pp. 929–932, 1999.