A Novel Low Input Impedance Low Power Fully Differential Current Buffer with ±0.65V Supply Voltage and high bandwidth of 520MHz

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Abstract: - A new fully differential (FD) low input impedance CMOS current buffer with low voltage, and low power operation is presented. The low input impedance is achieved by remarkable reduction of the input node voltage swing using a novel double feedback scheme. Some advantages of the proposed double feedback scheme over the conventional (either positive or negative) feedback techniques are: lower input impedance, robustness to process tolerances and a very simple and compact design. As a fundamental building block, this current buffer can also be used to implement such current mode circuits as current conveyors, current differencing buffered amplifiers (CDBA), current mode operational amplifiers, oscillators, filters and some voltage operational amplifiers (VOA). The proposed current buffer is designed and simulated with HSPICE using TSMC 0.18µm CMOS process parameters and supply voltage of ±0.65V. The simulated input impedance is 0.44Ω which shows a reduction factor of 6250 compared to the conventional common gate structure. It exhibits excellent -3dB bandwidth of 520MHz and low power consumption of 180µW which stem from its very simple structure. The proposed current buffer also exhibits high common mode rejection ratio (CMRR) of 90dB, very high positive and negative power supply rejection ratio (PSRR+/PSRR-) of 112dB and 143dB respectively which makes it very suitable for low voltage mixed mode applications. The corner case and Monte Carlo simulation results are also provided which proves the outstanding robust performance of the proposed current buffer against technology process tolerances.

Key-Words: - Low input impedance, Current Buffer, Current Conveyor, Constant bandwidth voltage amplifier, Current Amplifier, Current Mode, Dual Feedback.

1 Introduction

Excellent performance features of current mode signal processing such as high bandwidth, wide dynamic range, low voltage and low power operation, are the main reasons of current mode design popularity in recent years [1-6]. Under the strict low voltage-low power limitations imposed by the modern technologies[7], low voltage operation of current mode circuits which mainly stems from their low impedance nodes, have made current mode signal processing a suitable alternative for voltage mode one [1-6].

Current buffers are one of the main building blocks of current mode signal processing. They have found wide applications in the design of current mode filters and oscillators or in applications involving such current output sensors as pressure sensors, light sensors, magnetic sensors etc[8-15]. Furthermore they are used in the design of almost all current mode building blocks such as current mode amplifiers, current difference buffered amplifiers (CDBA), current differencing transconductance amplifiers (CDTA), current follower/inverter buffered transconductance amplifier (CITBA) and operational floating current conveyors (OFC) [16-29]. Finally current buffers can also be exploited to implement constant bandwidth voltage amplifiers [30].

As a result it plays a fundamental role in the current mode signal processing. One of the main characteristic of current buffers is input impedance which should be kept as low as possible. The importance of low input impedance is significant particularly where it is

used as the input stage of optical preamplifiers. Due to large parasitic capacitance of photo diodes, the input impedance of current buffer is the dominant factor in determining the optical preamplifier bandwidth as wide as required [31]. Current buffers should have simple structure with high frequency performance and low power consumption. Apparently high power consumption, complicated structure and poor frequency performance of current buffers, will degrade at least the same performance parameters of the larger current mode circuits containing them. Current buffers can be classified into three groups of single input single output (SISO), differential input single output (DISO) and fully differential (FD) configurations. Popularity of mixed mode design distinguishes the fully differential (FD) current buffers. This type owing high PSRR and CMRR can suppress the noise and unwanted common mode signals, clock feed through and interferences caused from the digital part of the design [32] hence is the most demanded type. Very interesting characteristic of FD structure is its generality in a way that it can also be used as SISO or DISO configurations to offer high CMRR and PSRR performance, thus has become the most frequently approached type.

Common gate stage is the simplest current buffer consisting of only one transistor and one current source as shown in fig.1-a. Its input impedance is not low enough and is in the order of 1/gm where gm is the transconductance of input transistor. The current mode operational amplifiers reported in [21] and [22] which use common gate stage at their inputs have high input impedance of 21KΩ and 5.8KΩ respectively. Increasing either input transistor aspect ratio or/and bias current are traditional methods to increase gm and consequently to decrease input impedance. These methods cause two negative consequences: 1) degraded frequency performance due to increased parasitic capacitances. 2) Large chip area and high power consumption. In some current mode circuits [16, 18, 32] positive feedback approach has been used to reduce the input impedance of common gate stage as is shown in fig.1-b. In this scheme the source of M2 is grounded making zero the voltage of the input node due to equality of the currents of the input transistor M1 and positive feedback network transistor M2. This arrangement thus theoretically results in zero value for input impedance of the current buffer. In practice, the input impedance of this current buffer can be found from [16]:

$$R_{in} = \frac{1}{g_{m1} \cdot g_{m3}} \cdot [(g_{ds1} + g_{m3} + g_{ds3}) - \frac{g_{m1} \cdot g_{m4}}{g_{ds4} + g_{m2} + g_{ds2}}] \quad (1)$$

Where gm_i and gds_i denote their usual meaning of the related transistors. As can be deduced from (1), setting the term in bracket [] equal to zero provides zero input impedance. Unfavourably any small perturbation- due to environmental effects such as temperature or the ones happen during fabrication process- can cause negative input impedance. Consequently the term in the bracket in (1) should be larger than zero to avoid negative input impedance and instability problems even in worst case. The reported input impedances using this method are 120Ω [16], 123Ω [18] and 8.4Ω [32].

Negative feedback is another method to reduce the input impedance of common gate stage which has been widely used [17, 20, 23-28, 33]. It does not have the negative input impedance problem of positive feedback approach. Using negative feedback technique, input impedances of 147Ω, 23 Ω, 14Ω and 18Ω are reported in [20], [23],[28] and [33] respectively. According to the feedback theory [34], the input impedance of common gate stage is divided by the feedback loop gain. Hence larger loop gains result in lower input impedance. In the past, high loop gains have been realized by cascoding transistors to generate high-output impedances. Unfavourably such high impedance cascode nodes demand large supply voltages which have to be avoided in modern CMOS technologies. Although multi stage amplifiers can increase loop gain under low supply voltage constraint of modern CMOS technologies, they suffer from closed loop stability problems. In fact frequency compensation of multi stage amplifiers is very difficult and need complicated frequency compensation schemes. In [35], a complete COA is used in closed loop unity gain configuration to form a current buffer with low input impedance. Although this

approach results in a current buffer with low input impedance, the resulted current buffer can hardly be used to design other current mode circuits. Employing such current buffer in the design of other current mode circuits will results in a complicated circuit, large consumed power and area especially in the case of FD ones.

Based on the above considerations, in this paper a novel robust low input impedance FD current buffer based on the negative feedback approach is introduced. The proposed current buffer exhibits very low input impedance, simple structure, high frequency performance, high CMRR and PSRR. Another merit of the proposed current buffer is its robust performance which has been achieved by avoiding the probable negative input impedance of positive feedback and the closed loop stability problem of negative feedback approaches. Favourably due to its very simple structure, it has very low power consumption and high frequency performance too. The novelty of the proposed current buffer is that in its structure two negative feedback loops are so elaborately arranged to work completely independent from each other making the high loop gain (and the required frequency compensation) completely unnecessary and offering such advantages as very low input impedance, high bandwidth and robust operation to the current buffer. The input impedance is reduced by the first negative feedback loop and then it is further reduced by the second one without any need to high gain multi stage feedback loops and additional frequency compensation. Favourably the proposed technique results in a simple design procedure and a compact circuit.

By the authors' knowledge; the proposed current buffer based on the proposed approach is the first yet reported fully differential current buffer with the lowest reported input impedance under low supply voltage. The proposed technique can be used in the implementation of almost all current mode building blocks such as COA, CDBA, CDTA and etc. The arrangement of the paper is as follows:

In section 2 the proposed current buffer is presented. Simulation results are presented in section 3 and finally section 4 concludes the paper.

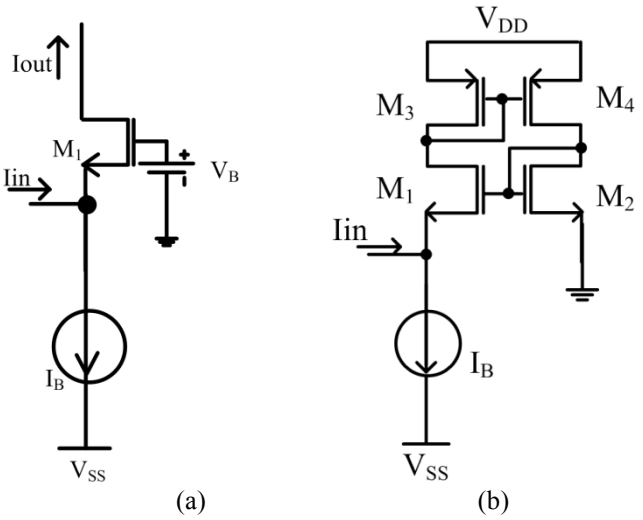

Fig.1 two current buffers a) simple common gate stage b) common gate stage employing positive feedback

2 The Proposed Low Input Impedance Current Buffer

The proposed low input impedance current buffer is based on the simple concept of:

"In an ideal current buffer with zero input impedance, voltage swing at the input node will be zero for any value of input current"

Hence in the proposed approach we try to keep input node voltage swing as close to zero as possible in order to achieve the lowest possible input impedance. The conceptual schematic of the proposed current buffer is shown in fig.2 in which for simplicity, half of the circuit is shown. It is composed of input transistor M1 and two negative feedback loops as are shown in dashed line in the right and left sides of M1. Input transistor M1 and auxiliary amplifier A constitute the first negative feedback loop. The positive input of Auxiliary amplifier is connected to ground potential and tends to force the input node (which is connected to the negative input node of A) to ground potential due to negative feedback action. However due to the limited voltage gain of auxiliary amplifier the absolute value of input node voltage will be larger than zero implying

only moderately low input impedance. The auxiliary amplifier reduces the input node voltage by a factor of A (its voltage gain) resulting in a reduction in the input impedance by the same factor. Using simple feedback theory [34], gives the input impedance as:

$$rin' = \frac{\frac{1}{g_{m1}}}{1+A} \approx \frac{1}{g_{m1}.A} \qquad (2)$$

Where gm1 is the transconductance of input transistor M1. Increasing auxiliary amplifier voltage gain by using high gain cascode structures or multi stage amplifiers further reduces the input impedance but impose high supply voltages and complicated frequency compensation schemes as are explained briefly in the introduction. To avoid these limitations, in the proposed current buffer the input impedance is further decreased by employing another negative feedback loop which works completely independent from the first one. The second feedback loop which is made up of M2 and M3 transistors further reduces the input node voltage by reducing the gate-source voltage of M1. It is a shunt-shunt feedback operates in a way that any change in the input current is drained by M3 rather than M1 resulting in a reduced gate-source voltage for M1 and hence reduced input node voltage. Its operation can be simply explained as: Due to low input impedance of M1 (which is 1/A.gm) compared to the output impedance of M3, input current initially enters M1 and is converted to voltage at the gate of M2. M2 acts as a level shifter and transfers the produced voltage to the gate of M3. Transistor M3 is configured as a common source amplifier and converts its gate voltage back to current performing a negative feedback loop which finally causes the input current to be drained by M3 rather than M1. Hence the M1 current is reduced by the second feedback loop resulting in an effective reduction in the input node voltage swing. The factor of reduction is equal to the loop gain of second feedback loop which can be found as:

$$A' \approx r_{oB1} \times \frac{r_{oB2}}{\frac{1}{g_{m2}} + r_{oB2}} \times g_{m3} = \frac{r_{oB1} \times (g_{m2} \times r_{oB2}) \times g_{m3}}{1 + (r_{oB2} \times g_{m2})} \approx r_{oB1} \times g_{m3} \qquad (3)$$

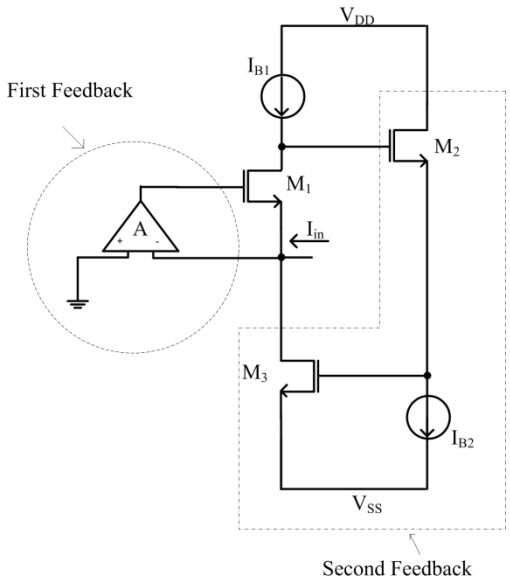

Fig.2 Conceptual Schematic of the proposed approach

Where r_{oB1} and r_{oB2} are the output impedances of current sources I_{B1} and I_{B2} respectively. Other parameters have their usual meaning. The input impedance stated at (2) is further reduced by the second feedback loop resulting in the final input impedance of:

$$rin = \frac{\frac{1}{g_{m1}}}{A \times A'} = \frac{\frac{1}{g_{m1}}}{A \times r_{oB1} \times g_{m3}} \qquad (4)$$

It can be simply shown that by a proper design, both negative feedback loops become stable and need not any frequency compensation resulting lower chip area and wider bandwidth (due to the absence of large value compensation capacitors). Another outstanding property of the proposed approach is that both negative feedback loops have very simple structure and work completely independent from each other which simplifies analyzing their frequency performance and stability. We start from first feedback loop. Examining fig.2 shows that the first feedback loop has one dominant pole at the output of auxiliary amplifier and one non dominant pole at the input node that can be expressed as:

$$P_d = \frac{1}{Ro \times Co} \qquad (5)$$

$$P_{nd} = \frac{1}{\frac{1}{\mathrm{A.A'}.g_{m1}} \times C_{in}} \quad (6)$$

Where Cin, Co and Ro are the total capacitance at the buffers input node, total capacitance at the gate of M1 and output impedance of auxiliary amplifier A respectively. Since A is a transconductance amplifier with high output impedance; the non dominant pole would be much larger than the dominant one and the transfer function of first feedback loop could be considered as a single pole function. Such a single pole transfer function will have 90º of phase margin which makes additional frequency compensation unnecessary.

Second feedback loop, similar to the first one, has one dominant and one nondominant pole which can be found as eq. (7) and (8) respectively:

$$P_d = \frac{1}{Ro_{IB1} \times C_2} \quad (7)$$

$$P_{nd} = \frac{1}{\frac{1}{g_{m2}} \times C_1} \quad (8)$$

Where gm2, C1, Ro_{IB1} and C2 are the transconductance of M2, total capacitance at the gate of M2, output impedance of IB2, and total parasitic capacitance at the gate of M3 respectively. As can be deduced from (7) and (8), due to the large value of R_{OIB1} compared to $(g_{m2})^{-1}$, the nondominant pole is larger than the dominant one. Furthermore, the nondominant pole is proportional to the gm2 and can be controlled by IB2 to be pushed to much higher frequencies offering single pole frequency performance with near 90º of phase margin for the second feedback loop. This is the remarkable advantage of the proposed approach in which input impedance is reduced by two independent negative feedback loops without any need to high gain feedback loops and additional frequency compensation.

Fig.3 shows the conceptual schematic of differential input implementation of the proposed approach in which an auxiliary amplifier with three input (one connected to ground and the other two connected to the buffers inputs) and differential output is used.

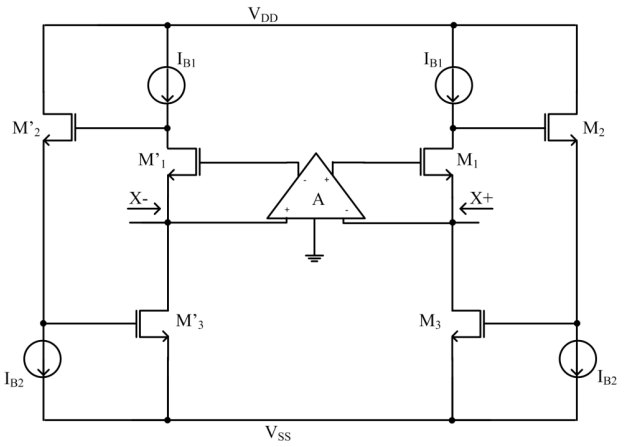

Fig.3 Conceptual Schematic of the proposed current buffer with differential input

Fig.4 shows the complete implementation of the proposed fully differential current buffer in which M1-M'1 are the input transistors, transistors M8-M16 constitute the three input differential output auxiliary amplifier and transistors M2-M3 and M'2-M'3 form the second feedback loop. Low voltage composite cascode transistors [35] are used at the load of auxiliary amplifier in the first feedback loop gain. The fully differential output is achieved employing two PMOS current mirrors consisting of M6-M7, M'6-M'7 transistors and two NMOS current mirrors consist of M4-M5 and M'4-M'5. The cross coupled connection of NMOS and PMOS current mirrors causes to subtract the common mode currents at the output branch resulting in a significant high CMRR for the fully differential structure given by:

$$CMRR = \frac{1}{\lambda_1 - \lambda_1.\lambda_2} \quad (9)$$

Where λ1 and λ2 are the current mirror ratio of M6-M7 (and M'6-M'7) PMOS and M4-M5 (and M'4-M'5) NMOS current mirrors respectively.

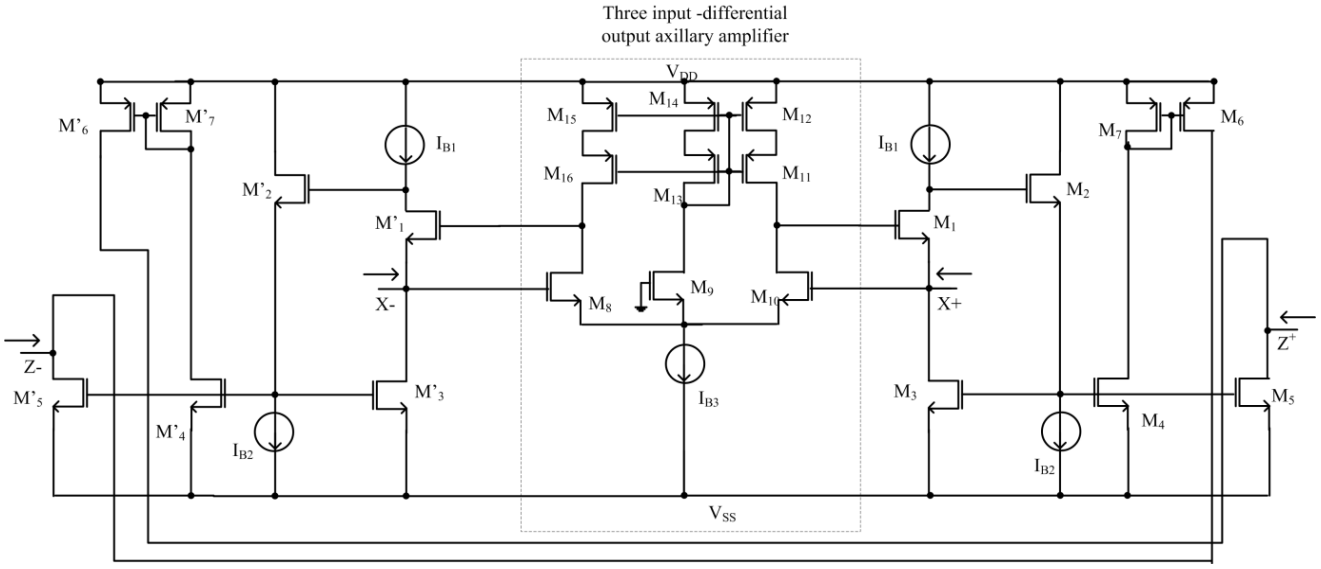

Fig.4 the proposed low input impedance current buffer in fully differential structure

The small signal transfer function of the proposed current buffer can be found as:

$$Ai = \frac{\frac{A'}{A'+1}}{(1+\frac{S}{\frac{A'}{Ro_{IB1}\times C_2}}).(1+\frac{S}{\frac{A}{Ro\times Co}})} \quad (10)$$

Where:

$$A' = r_{oIB1}\times\frac{r_{oIB2}}{r_{oIB2}+\frac{1}{g_{m2}}}\times g_{m3} = r_{oIB1}\times\frac{r_{oIB2}}{r_{oIB2}+\frac{1}{g_{m'2}}}\times g_{m'3} \quad (11)$$

$$A = g_{m8}\times[r_{o8}\|((m-1)r_{o16}] = [r_{o10}\|((m-1)r_{o11}] \quad (12)$$

$$m = \frac{(\frac{W}{L})_{11}}{(\frac{W}{L})_{12}} = \frac{(\frac{W}{L})_{16}}{(\frac{W}{L})_{15}} > 1 \quad (13)$$

$$C_o \approx Cgs_1 + Cdb_{10} + Cdb_{11} + Cdg_{11} + Cdg_1 + Cgd_{10} \quad (14)$$

$$C_2 \approx Cgd_2 + C_{IB2} + Cdg_1 + Cdb_1 + Cdg_1 + C_{eq} \quad (15)$$

$$C_{eq} = Cgs_2\|(Cgs_3 + Cgs_4 + Cgs_5) = \frac{Cgs_2\times(Cgs_3 + Cgs_4 + Cgs_5)}{(Cgs_2.Cgs_3 + Cgs_2.Cgs_4 + Cgs_2.Cgs_5)} \quad (16)$$

Inserting (11) and (12) into (4) results the input impedance as:

$$r_{in}^{+} = \frac{\frac{1}{g_{m1}}}{(r_{oIB1}\times\frac{r_{oIB2}}{r_{oIB2}+\frac{1}{g_{m2}}}\times g_{m3}).g_{m8}\times[r_{o8}\|((m-1)r_{o16}]} \quad (17)$$

$$r_{in}^{-} = \frac{\frac{1}{g_{m'1}}}{(r_{oIB1}\times\frac{r_{oIB2}}{r_{oIB2}+\frac{1}{g_{m'2}}}\times g_{m'3}).[r_{o10}\|((m-1)r_{o11}]} \quad (18)$$

3 Simulation Results

The proposed FD current buffer of fig.4 was designed and simulated in 0.18µm TSMC CMOS technology with nominal threshold voltages of 0.43V and -0.45V for NMOS and

PMOS transistors respectively. The transistors aspect ratios and bias settings are summarized in tables 1 and 2 respectively. All current sources are implemented using simple current mirrors with transistors aspect ratios of 8μm/0.5μm, 10μm/0.5μm and 12μm/0.5μm for IB1, IB2 and IB3 respectively.

The frequency performance of input impedance is shown in fig.5 which shows an input impedance of 0.44Ω for the proposed FD current buffer. The effectiveness of the proposed double feedback approach in reducing input impedance becomes evident by comparing the input impedance of the proposed current buffer and conventional common gate stage. Simulation results show that common gate stage with bias current of 15μA and aspect ratio of 70μm/0.3μm without employing the proposed negative feedbacks shows an input impedance of 2.75KΩ which is 6250 times larger than that of the proposed one. Comparing the input impedance of the proposed current buffer with the advanced ones reported in litrechures employing the aforementioned conventional techniques proves the superiority of the proposed approach over them. To have a fair comparison, three important parameters affecting the input impedance including bias current, input transistors aspect ratio, supply voltage as long as input impedance of the proposed current buffer and some advanced works are summarized in table 3. As can be seen, the proposed current buffer offers the lowest input impedance under the lowest supply voltage. Corner case simulations results also show input impedance of 0.53Ω, 0.51Ω, 0.51Ω and 1Ω for the FF, FS, SF and SS corners which again proves the robustness of the proposed current buffer and its very low input impedance in all situations.

Fig.6 shows the current gain frequency performance of the proposed current buffer with an excellent -3dB bandwidth of 520MHz. Corner case simulation is also carried out to examine the effect of process on the frequency performance of the proposed current buffer. The results are shown in fig.7 which shows -3dB bandwidth of 531MHZ, 520MHz, 498MHz and 485MHz for the FF, FS, SF and SS corners respectively. Robust performance and approximately constant -3dB bandwidth in all process corners is the remarkable characteristic of the proposed current buffer.

Table .1 Transistors aspect ratios

Transistor	Aspect Ratio
M_1, M'_1	70μm/0.3μm
M_2, M'_2	5μm/0.3μm
M_3-M'_3	8μm/0.3μm
M_4,M'_4	8μm/0.3μm
M_5, M'_5	8μm/0.3μm
M_6, M'_6	16μm/0.5μm
M_7, M'_7	16μm/0.5μm
M_8-M_{10}	8μm/0.8μm
M_{11},M_{13}, M_{16}	150μm/1μm
M_{12},M_{14}, M_{15}	12μm/1μm

Table .2 Bias Settings

Parameter	Value
V_{DD}	0.65V
V_{SS}	-0.65V
I_{B1}	15μA
I_{B2}	12μA
I_{B3}	14μA

The stability of the proposed current buffer in all process corners are investigated by applying a step input of ±20μA to its inputs. The result is shown in fig.8 which proves the stability of the proposed current buffers in all situations.

Fig.9 shows the CMRR frequency performance of the proposed current buffer. As can be seen, it exhibits a high CMRR of 90.16dB and

excellent frequency performance with high f_T of 1.3GHz. To investigate CMRR variation with mismatches, Monte Carlo simulation was carried out by considering 3% mismatch in threshold voltage and Tox of all transistors in 100 runs. The resulted CMRR variation is shown in fig.10. As can be seen the maximum and minimum values of CMRR are 105dB and 51dB which are sufficient for most applications. Its simulated PSRR+ and PSRR- are also 112dB and 143dB respectively which is shown in fig.11. These results prove the high capability of the proposed FD current buffer in low voltage mixed mode applications requiring high CMRR and PSRR. Power dissipation of the proposed current buffer is only 180µW which makes it suitable for the design of low power current mode building blocks.

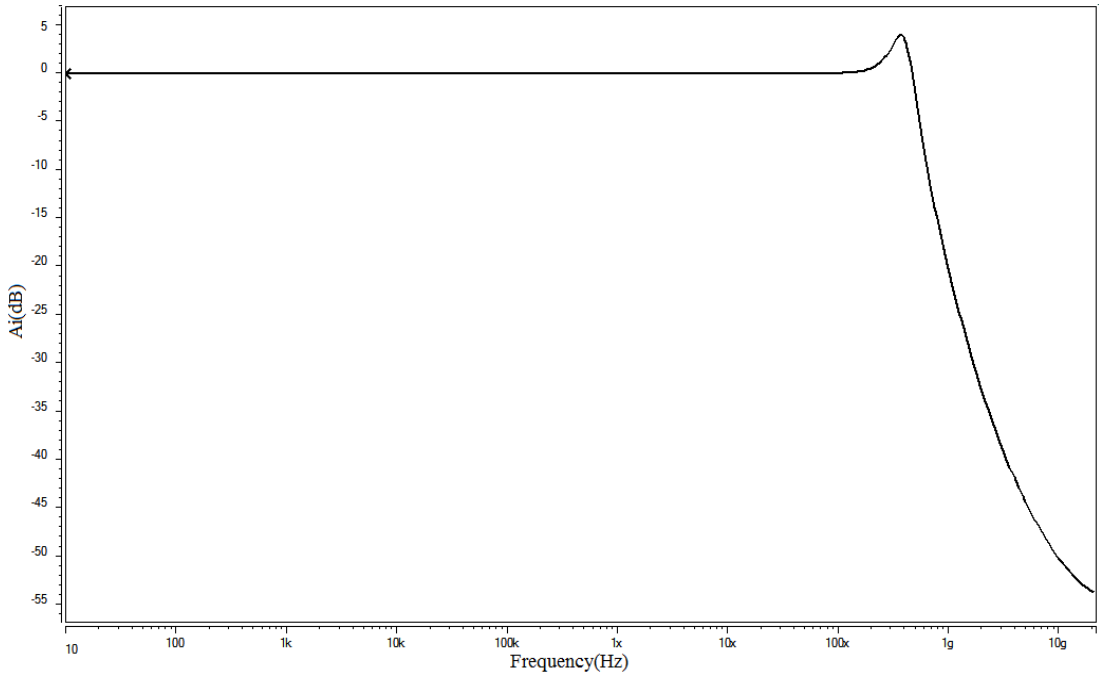

Fig.5. Input impedance frequency response

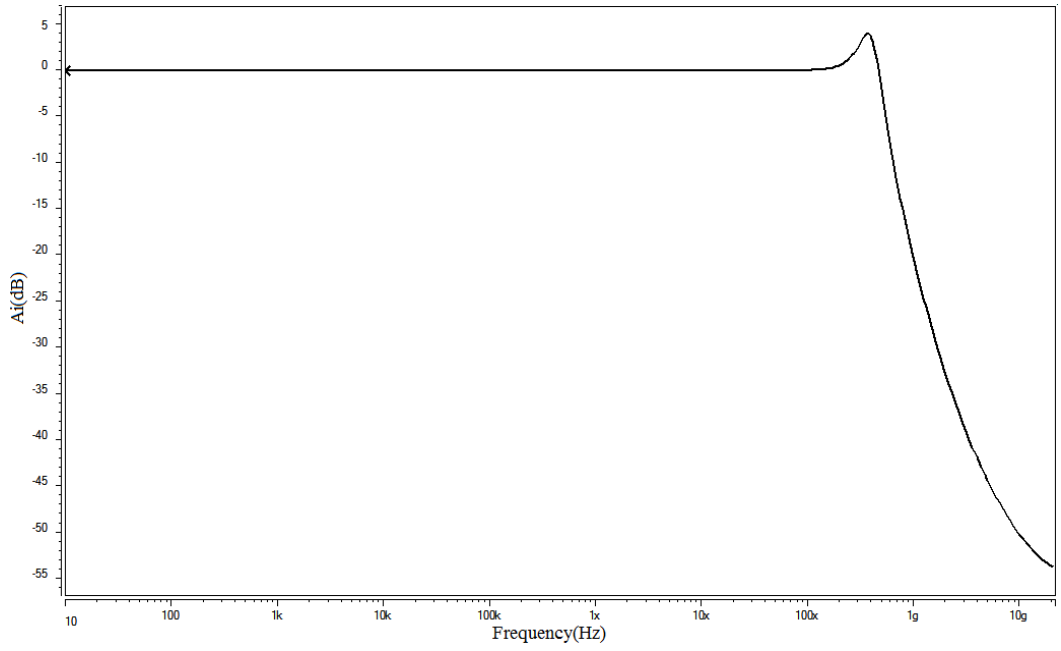

Fig.6. Current gain frequency response of the proposed current buffer

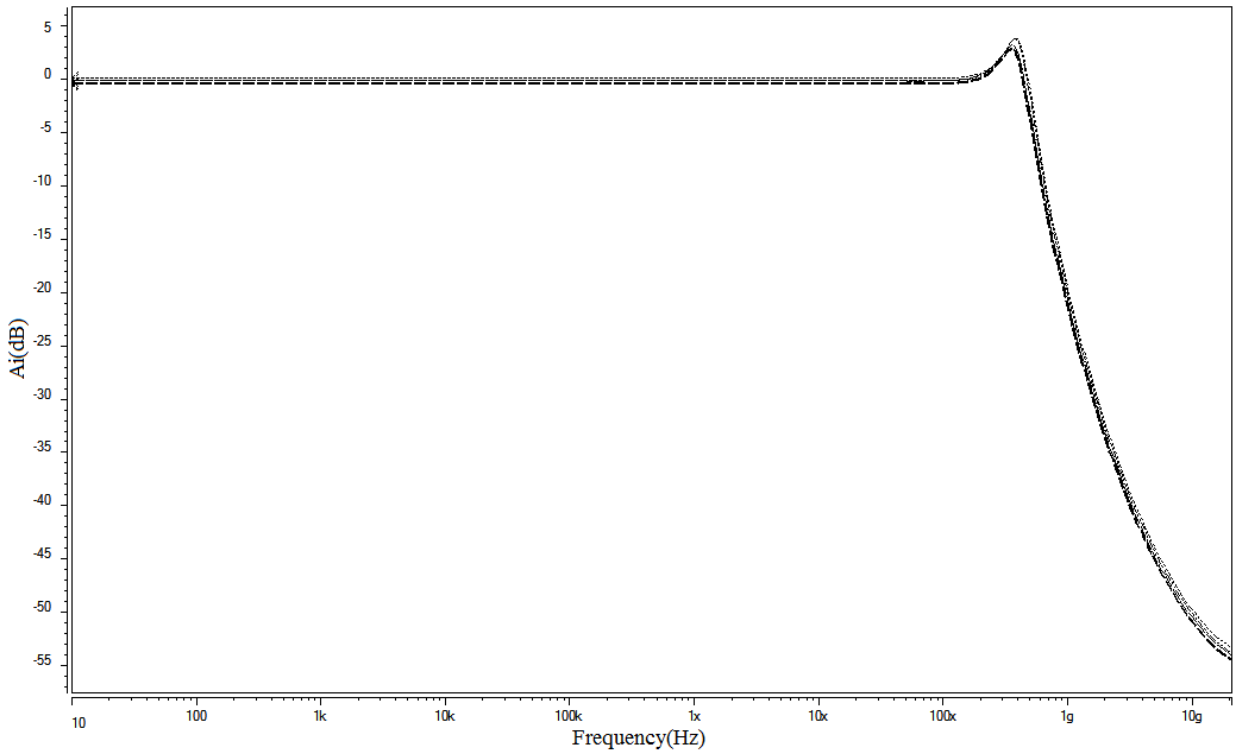

Fig.7. Current gain frequency response of the proposed current buffer in FF, FS, SF and SS process corners

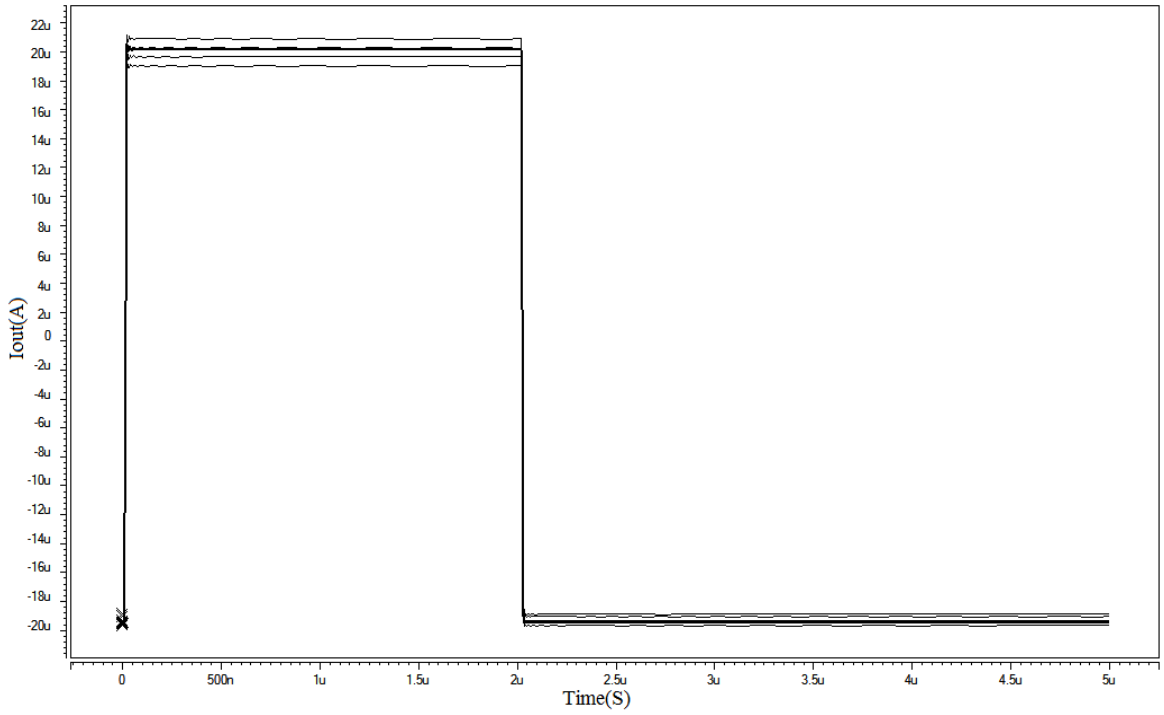

Fig.8 Step response of the proposed current buffer in typical case and all process corners

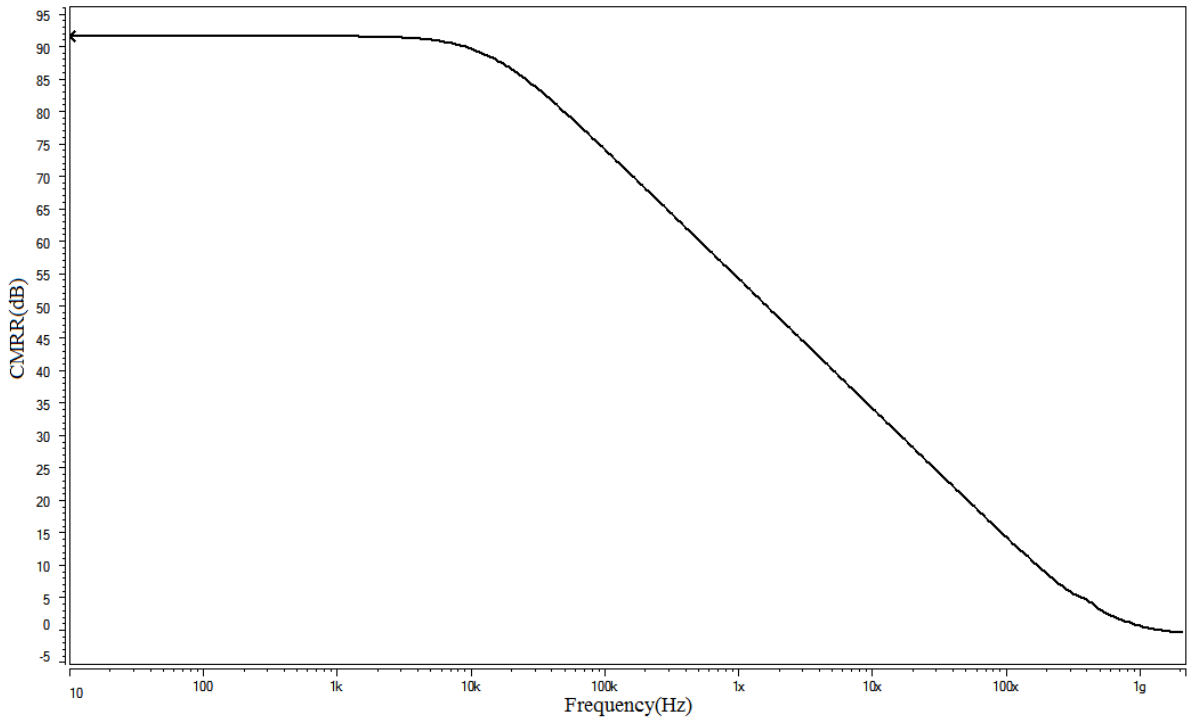

Fig.9 CMRR frequency performance of the proposed FD current buffer

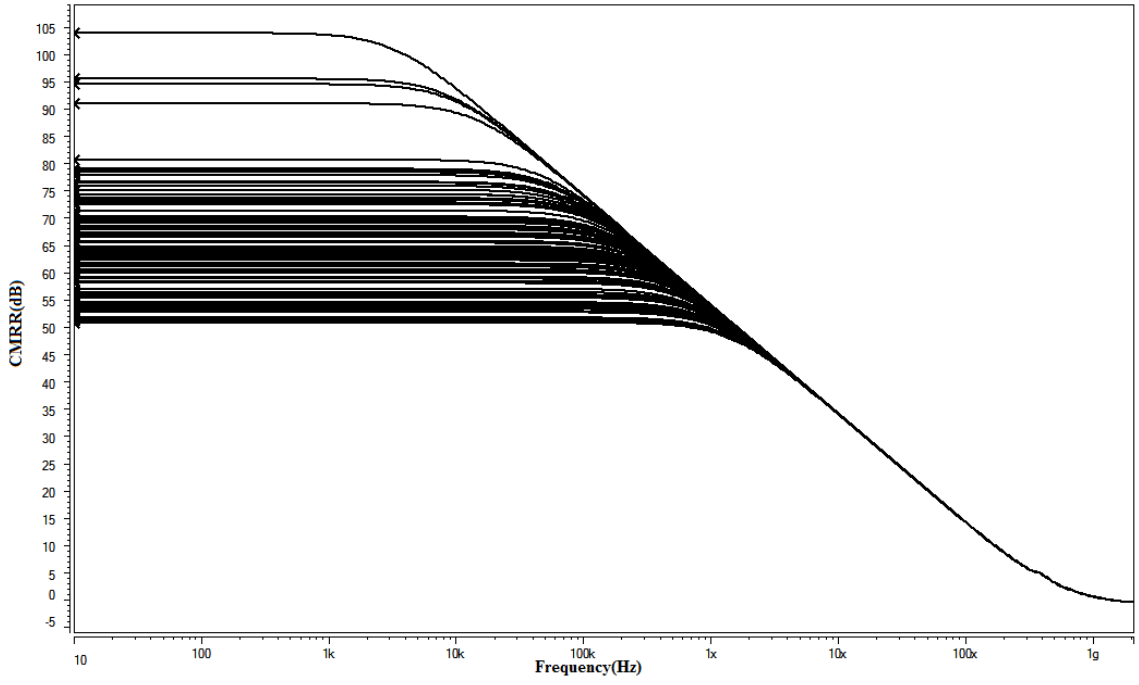

Fig.10 CMRR frequency performance of the proposed FD current buffer in the presence of mismatches

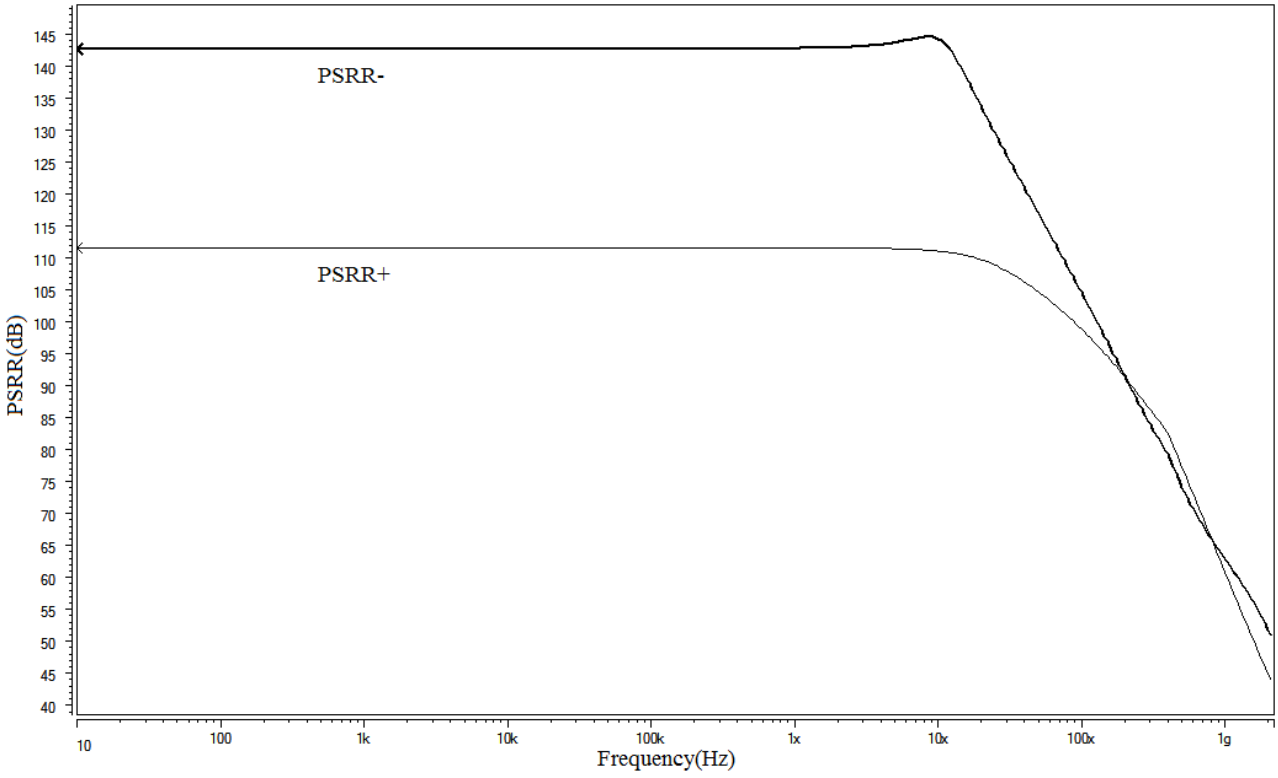

Fig.11 PSRR frequency performance of the proposed FD current buffer

Table 3. Input impedance comparison between some reported advanced current buffers and the proposed one

Current buffer employing	Input transistor		Supply voltage	Input Impedance (Ω)	Ref/Pub. Year
	Aspect ratio	Bias current			
Positive feedback	20µm/0.7µm	30µA	±1.5	120	[16]/2008
	6µm/1µm	10µA	±1.5	123	[18]/2007
	10µm/0.22µn	10µA	±0.75	8.48	[31]/2010
Negative feedback	NA	NA	±3	147	[20]/1997
	NA	NA	±1.5	22	[23]/2005
	NA	NA	±0.75	50	[25]/2008
	20	30 µA	±1.25	32	[27]/2004
	24µm/1.2µm	20 µA	±0.75	10	[33]/1999
Proposed Double Feedback	70µm/0.3µm	15µA	±0.65	0.44	-

4 Conclusion

In this paper, a new low voltage low power fully differential current buffer with low input impedance is introduced which can be employed independently or as input stage of such current mode circuits as COA, CDBA, CDTA etc. Besides very low input impedance, the high CMRR and PSRR offered by the proposed current buffer makes it suitable in the mixed mode design. It has simple configuration that involves two negative feedback loops which work independently. Each feedback loop is so designed that exhibits single pole frequency performance. The overall result is that no frequency compensation is needed resulting in a very simple design and small chip area (due to the absence of compensation capacitors). Two feedback loops work in a way that voltage swing at the input node is reduced resulting in very low input impedance. Simulation results of the proposed current buffer confirm its low input impedance, high bandwidth, high CMRR and PSRR. In conclusion, the proposed low input impedance current buffer can be used to design wide variety of current mode building blocks.

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