A Design Approach for DC Voltage Controller of CHB-based STATCOM

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Abstract: - In this paper, a novel parameter design approach of the PI controller used for individual DC voltage balancing control of cascaded H-bridge converter-based STATic synchronous COMpensator(STATCOM) is presented. By means of phase shift sinusoidal pulse width modulation, using two control loops(DC voltage control loop and phase angle shift control loop) to ensure DC voltage balance, the proposed approach can calculate parameters of the PI controller of the two control loops relative accurately by finding the relationship of the input and output of PI controller, The simulation and experimental results verify that the proposed method has good effects of balancing individual DC voltage, meanwhile, it makes the system a good dynamic performance.

Key-Words: - CHB inverter, Static synchronous compensator (STATCOM), DC voltage controller, parameter design, Sinusoidal pulse width modulation

1 Introduction

Multilevel converters have received more and more attention because of their capability of high voltage operation, high efficiency, and low electromagnetic interference. especially, multilevel converters have been used for STATCOM widely as it can improve the power rating of the compensator to make it suitable for medium or high-voltage high power applications[1-2]. There are many types of multilevel converters used for constructing STATCOMs such as diode-clamp converter, flying-capacitor based converter, and cascaded H-bridge converter. cascaded H-bridge topologies is more popular because of its many advantages: (1)it can generate almost sinusoidal waveform voltage from several separate dc sources to reduce harmonics. (2) it can response faster because of eliminating the need of a transformer to provide the requisite voltage levels. (3)modularized circuit layout and packing is very easy due to the simplicity of structure[3-4].

Fig. 1 shows the block diagram of a cascaded H-bridge multilevel converter based STATCOM.

The converter used in STATCOM acts as an inverter, and each H-bridge cell can generate three different voltage outputs by connecting dc voltage to ac side through different states of the four switches. The control of the phase angle between line voltage and voltage source converter (VSC) voltage leads STATCOM to absorb or supply reactive power. For cascaded H-bridge converters based STATCOM, it is important to ensure that the power drawn from each DC side is equal. Thus, each H-bridge cell in the inverter is equally utilized. However, due to inverter devices are not ideal and have different tolerance errors, each dc capacitor voltage may not be exactly balancing. It is a main disadvantage for cascaded H-bridge converters used for STATCOM, so it is necessary using an additional control strategy to balance the DC voltages [5-12] [14].

Several literatures have discussed how to balance the DC voltage of the cascaded H-bridge multilevel converter. In [8] shifting a small phase angle of the output voltage for every H-bridge cells is presented. In[9][10] a switching pattern swapping scheme is presented. However, a low-frequency switching modulation--looking-up table method was used in it due to the limitations of high power electronic switches. In [1], it combines individual balancing control with clustered balancing control to regulate DC voltage. However, it is not easy to assign appropriate values to gain parameters. like in [1], in[14], additional control loop is used to regulate

each phase voltage, where phase shift is still used. A similar control strategy is used in[11]. In [12] individual voltage balancing strategy (IVBS) used for a single-phase STATCOM is presented, individual DC voltage and the reference value are used directly to regulate the active power absorbed by each cell.

Generally, phase angle shift control scheme is one of the most simple methods and easy to realize.This paper proposed a novel design approach about the PI controller of the two control loops (traditional DC voltage control loop and a small phase angle shift control loop), by means phase shift SPWM technique, it can realize DC voltage well balance.

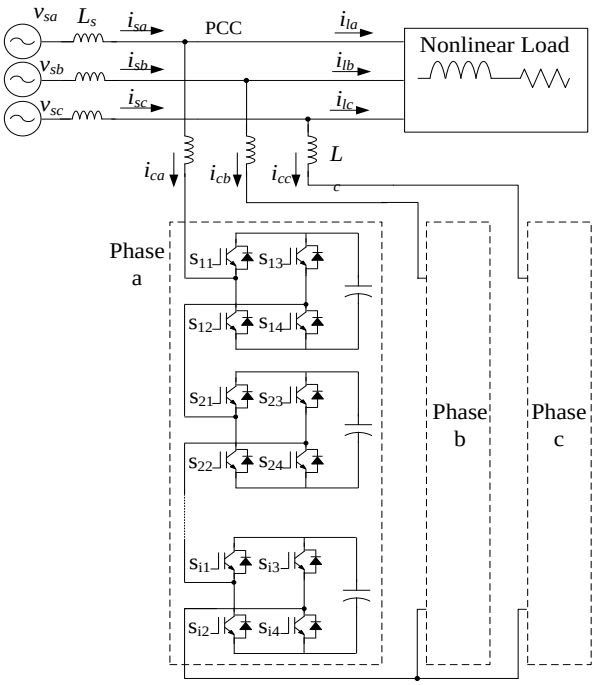

Fig. 1- Schematic of a cascaded-multilevel converter based STATCOM system

2 Control scheme

2.1 Dynamic model of STATCOM

Fig. 2 shows the equivalent circuit of the STATCOM system, where v_s is the source voltage, v_c is the generated voltage of the STATCOM and i_c is the current drawn by the STATCOM, L_c and R are reactance and resistance of source and filter reactor.

According to equivalent circuit shown in Fig. 2

$$L\frac{dI_c}{dt}+RI_c=V_s-V_c \tag{1}$$

In d-q synchronous reference frame, the mathematical expression of the STATCOM is shown as follows:

$$L\frac{d}{dt}\begin{bmatrix}i_{cd}\\ i_{cq}\end{bmatrix}+R\begin{bmatrix}i_{cd}\\ i_{cq}\end{bmatrix}=\begin{bmatrix}v_{sd}\\ v_{sq}\end{bmatrix}-\begin{bmatrix}v_{cd}\\ v_{cq}\end{bmatrix}+\omega L\begin{bmatrix}i_{cq}\\ -i_{cd}\end{bmatrix} \tag{2}$$

$$\begin{bmatrix}v_{sd}\\ v_{sq}\end{bmatrix}=\sqrt{3}U_s\begin{bmatrix}1\\ 0\end{bmatrix} \tag{3}$$

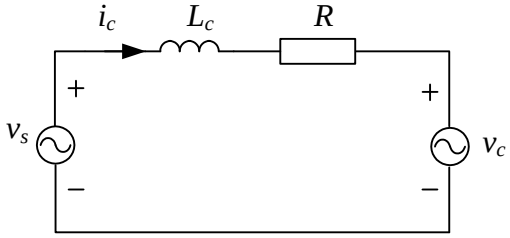

Fig. 2- Equivalent circuit of the STATCOM

2.2 Decoupled Currents Control Strategy

Equation (2) can be expressed as:

$$\frac{d}{dt}\begin{bmatrix}i_{cd}\\ i_{cq}\end{bmatrix}=\begin{bmatrix}-R/L & 0\\ 0 & -R/L\end{bmatrix}\begin{bmatrix}i_{cd}\\ i_{cq}\end{bmatrix}+\frac{1}{L}\begin{bmatrix}v_{sd}-v_{cd}+\omega Li_{cq}\\ v_{sq}-v_{cd}-\omega Li_{cd}\end{bmatrix} \tag{4}$$

Combine equation (4)with(3) , Introducing two intermediate variables, x_1, x_2

$$\begin{cases}x_1=v_{sd}-v_{cd}+\omega Li_{cq}\\ x_2=-v_{cq}-\omega Li_{cd}\end{cases} \tag{5}$$

Then convert (4) to

$$\frac{d}{dt}\begin{bmatrix}i_{cd}\\ i_{cq}\end{bmatrix}=\begin{bmatrix}-R/L & 0\\ 0 & -R/L\end{bmatrix}\begin{bmatrix}i_{cd}\\ i_{cq}\end{bmatrix}+\frac{1}{L}\begin{bmatrix}x_1\\ x_2\end{bmatrix} \tag{6}$$

Variables x1, x2 can be obtained

$$\begin{cases}x_1=k_p(i_{cd}^*-i_{cd})+k_i\int(i_{cd}^*-i_{cd})dt\\ x_2=k_p(i_{cq}^*-i_{cq})+k_i\int(i_{cq}^*-i_{cq})dt\end{cases} \tag{7}$$

i_{cq}^* is the reference of the reactive current, and it can be got through reactive current detection. The reference of the active current, i_{cd}^*, is derived from a PI controller as follows:

$$i_{cd}^*=(k_p+k_i/s)(v_{dc}^*-2\sum v_{dci}/(n-1)) \tag{8}$$

Where n is the number of level.

the d-axis and q-axis reference voltage equations of the STATCOM in Fig. 3 are

$$\begin{bmatrix}v_{cd}^*\\ v_{cq}^*\end{bmatrix}=\begin{bmatrix}v_{sd}\\ v_{sq}\end{bmatrix}-\begin{bmatrix}x_1\\ x_2\end{bmatrix}+\omega L\begin{bmatrix}i_{cq}\\ -i_{cd}\end{bmatrix} \tag{9}$$

The modulation index and phase angle of

STATCOM output voltage are given by:

$$MI = \sqrt{(v_{cd}^*)^2 + (v_{cq}^*)^2} \Big/ kn\bar{v}_{dc} \quad (10)$$

$$\delta = \tan^{-1}(v_{cq}^* / v_{cd}^*) \quad (11)$$

where k is a constant whose value depends on the modulation technique scheme used, n is the cascade number. in this paper, k is 0.5.

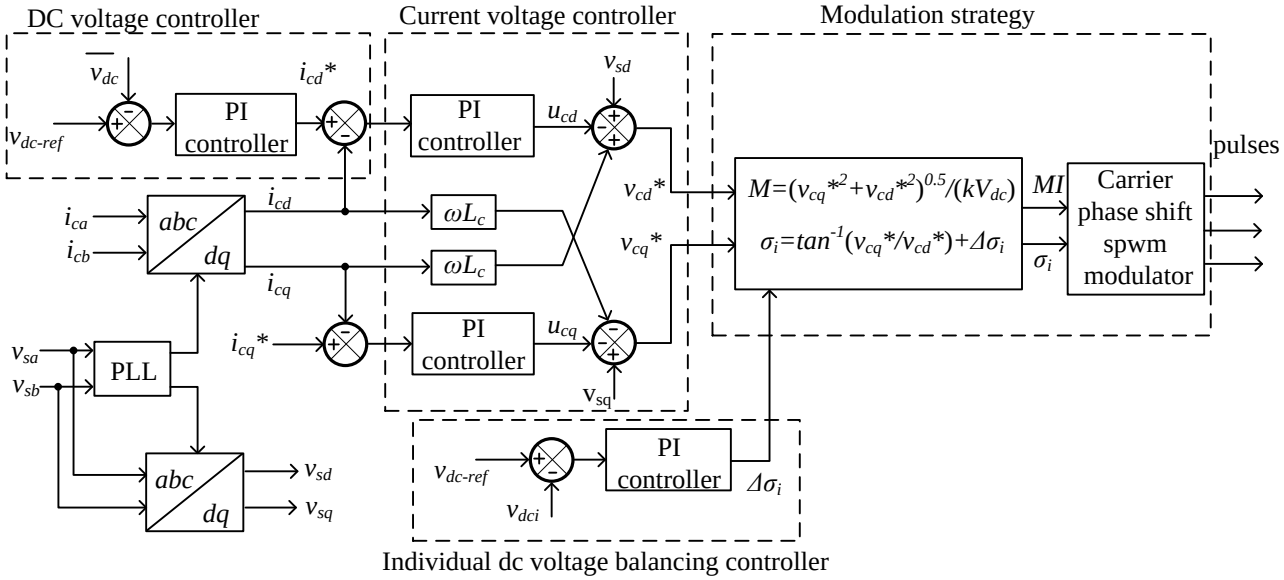

Fig. 3- The complete control block diagram of cascaded H-bridge converter based STATCOM system.

2.3 Analysis and Parameter Design of individual DC Voltage controllers

In Fig. 3, the output of DC voltage controller is used as the reference of the active current, and its main purpose is to maintain the DC voltage stable and compensate the loss power of the compensator. In order to get relative accurate parameter about PI controller, the relationship between the active current and DC capacitor variation is analyzed.

Assuming the main voltage of a A-phase $u_s(t)$ is expressed as follows:

$$u_{sa}(t) = U_s \sin \omega t \quad (12)$$

For STATCOM, the A-phase compensation current can be expressed as

$$i_{ca}(t) = I_c \sin(\omega t + \theta) \quad (13)$$

So $i_{ca}(t) = I_c \sin \omega t \cos\theta + I_c \cos \omega t \sin\theta$ (14)

Let $I_{pa} = I_c \cos\theta$, $I_{qa} = I_c \sin\theta$,then, I_{pa} , I_{qa} is respectively the amplitude value of fundamental active current and fundamental reactive current :

$$i_{ca}(t) = I_{pa} \sin \omega t + I_{qa} \cos \omega t \quad (15)$$

The majority of the output current of the STATCOM is reactive current to compensate reactive power of the load, but there is a little active current contained in i_c . loss power of the cascaded STATCOM is obtained as follows:

$$p_{ca}(t) = I_{pa} U_s \sin^2 \omega t \quad (16)$$

The integration of the loss power in a period

$$\int_{t_0}^{t_0+T_s} p_{ca}(t)dt = \int_{t_0}^{t_0+T_s} (I_{pa} U_s \sin^2 \omega t)dt$$

$$= I_{pa} U_s T_s / 2 \quad (17)$$

The integration of the active power in a period is used to stabilize the voltage of DC Capacitor:

$$\Delta p = \frac{1}{2} C(U_{dc} + \Delta V_{dc})^2 - \frac{1}{2} C V_{dc}^{\ 2} = \int_{t_0}^{t_0+T_s} p_{ca}(t)dt \quad (18)$$

Combine (17) with (18), we can get the following formula:

$$I_{pa} = \left(\frac{2V_{dc}C}{T_s U_s} \right) \Delta V_{dc} + \left(\frac{C}{T_s U_s} \right) (\Delta V_{dc})^2 \quad (19)$$

Converting I_{pA} to three-phase system will get the reference of active current.

$$i_{cd}^* = \left(\frac{\sqrt{6}V_{dc}C}{T_s U_s} \right) \Delta V_{dc} + \left(\frac{\sqrt{3}C}{\sqrt{2}T_s U_s} \right) (\Delta V_{dc})^2 \quad (20)$$

According to (20), DC voltage controller has been designed.

Theoretically, every H-bridge cell has the same structure, and carrier signals are distributed. So the amount of reactive currents drawn in and out of the

DC capacitor over a cycle are equal. Voltages on all the dc side capacitors will keep balanced finally. DC voltage balance can ensure that the power drawn from each DC side is equal, Thus, each H-bridge cell in the inverter is equally utilized. However, because of non-ideal converters and their internal losses are not identical, each VSC will have different DC voltages. Different DC voltages will affect the character of STATCOM and even damage the switch device. In conclusion, for all the STATCOM based on multilevel, DC voltage regulation is essential for normal operation. This paper, the additional control loop- phase angle shift balancing control is used.

Phase angle shift balancing control Principle is explained in the following.

Fig. 4 shows the output current and output voltage of an H-bridge converter in STATCOM application[13]. In order to simplify the explanation, take the current and the voltage are exactly 90° phase shifted for example, the total charge of the DC capacitor is zero, therefore, the capacitor voltage is stable.

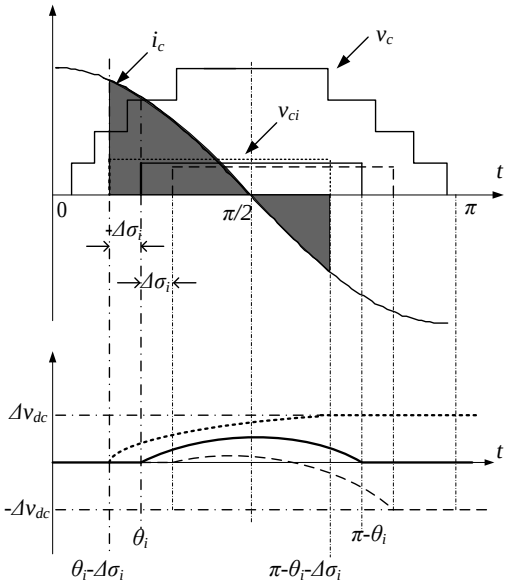

Fig. 4-Relationship of the phase angle shift in output voltage to the capacitor voltage change

However, if a small phase angle shift is introduced to the voltage waveform, the total charge in the capacitor is not zero, and a small positive phase angle shift means DC voltage will decrease, then the capacitor voltages can be corrected by adjusting the phase of the output voltage.

For phase angle shift control, the value of angle shift for each H-bridge cell is obtained by PI control of its practical DC voltage in Fig. 3

$$\Delta\delta_i = (k_{p1} + k_{i1}/s)(\frac{\sum v_{dci}}{(n-1)/2} - v_{dci}) \qquad (21)$$

In order to calculate more accurate parameters of PI controller, we also need to study on the relationship between the phase angle variable quantity and DC capacitor variation.

Fig. 4 shows a H-bridge cell average charge over a half cycle, where, the phase current lagging the phase voltage by 90°, and it indicate the system is working at full-inductive mode. If a phase angle is shifted ahead by $\Delta\delta_i$, then the energy absorbed by capacitor can be expressed as

$$w_{half} = \int_{\theta_i-\Delta\delta_i}^{\pi-\theta_i-\Delta\delta_i} \sqrt{2}V_{dci} I\cos\theta dt$$
$$= \frac{2\sqrt{2}}{\omega} V_{dci} I\cos\theta_i \sin\Delta\delta_i \qquad (22)$$

In one cycle, the active power injected from the mains is

$$w_{one} = \frac{4\sqrt{2}}{\omega} V_{dci} I\cos\theta_i \sin\Delta\delta_i \qquad (23)$$

Because of $\Delta\delta_i$ is small, $\Delta\delta_i \approx \sin\Delta\delta_i$

$$w_{one} = \frac{4\sqrt{2}}{\omega} V_{dci} I\cos\theta_i \Delta\delta_i \qquad (24)$$

w_{one} is used to compensate the loss power of each cell of the STATCOM . Hence:

$$w_{one} = \frac{1}{2}C_i(V_{dci} + \Delta V_{dci})^2 - \frac{1}{2}C_i {V_{dci}}^2 \qquad (25)$$

According to (24) and (25), the additional phase shift can be obtained to be:

$$\Delta\delta_i = \frac{C_i\omega}{4\sqrt{2}I\cos\theta_i}\Delta V_{dci} + \frac{C_i\omega}{8\sqrt{2}V_{dci}I\cos\theta_i}(\Delta V_{dci})^2 \qquad (26)$$

Because the switching scheme adopts phase shift unipolar sinusoidal pulse width modulation, $\theta_i = \pi/4$.

$$\Delta\delta_i = \frac{C_i\omega}{4I}\Delta V_{dci} + \frac{C_i\omega}{8V_{dci}I}(\Delta V_{dci})^2 \qquad (27)$$

The additional phase angle shift controller could be designed by (27).

2.4 Required Capacitance of DC Capacitors

When the switching scheme adopts phase shift sinusoidal pulse width modulation introduced next section, expression for DC voltage shown as follows[15]

$$v_{dc}(t) = V_{DC} + \frac{1}{4\omega C} m_a I\cos 2\omega t \qquad (28)$$

In (28), m_a is the MI, and I is the peak current drawn by the STATCOM. From(28), peak to peak voltage of DC capacitor is

$$\Delta V_{dc} = \frac{m_a I}{2\omega C} \tag{29}$$

In this paper, in order to keep ΔV_{dc} below 5% V_{DC}, required capacitance of DC capacitors is $3300\mu F$

2.5 Switching scheme

As shown in Fig. 5, switching scheme adopt phase shift unipolar sinusoidal pulse width modulation. There are three respectively, and they are shifted by $T_s/3$, where triangle carrier signals for three H-bridge inverters T_s is the period of these carrier signals. For modulating sinusoidal signals $v_{s(t)}$ and $-v_{s(t)}$, their initial phase angle is decided by the sum of δ and $\Delta\delta_i$,

$$\begin{cases} v_{sa(t)} = MI\cos(\theta' + \delta + \Delta\delta_i) \\ v_{sb(t)} = MI\cos(\theta' + \delta + \Delta\delta_i - 120^\circ) \\ v_{sc(t)} = MI\cos(\theta' + \delta + \Delta\delta_i + 120^\circ) \end{cases} \tag{30}$$

One of the main advantages of this switching scheme is that the harmonics of the resultant STATCOM output voltage only appear as sidebands centered around the frequency of $2Nf_s$ and its multiples.[15]

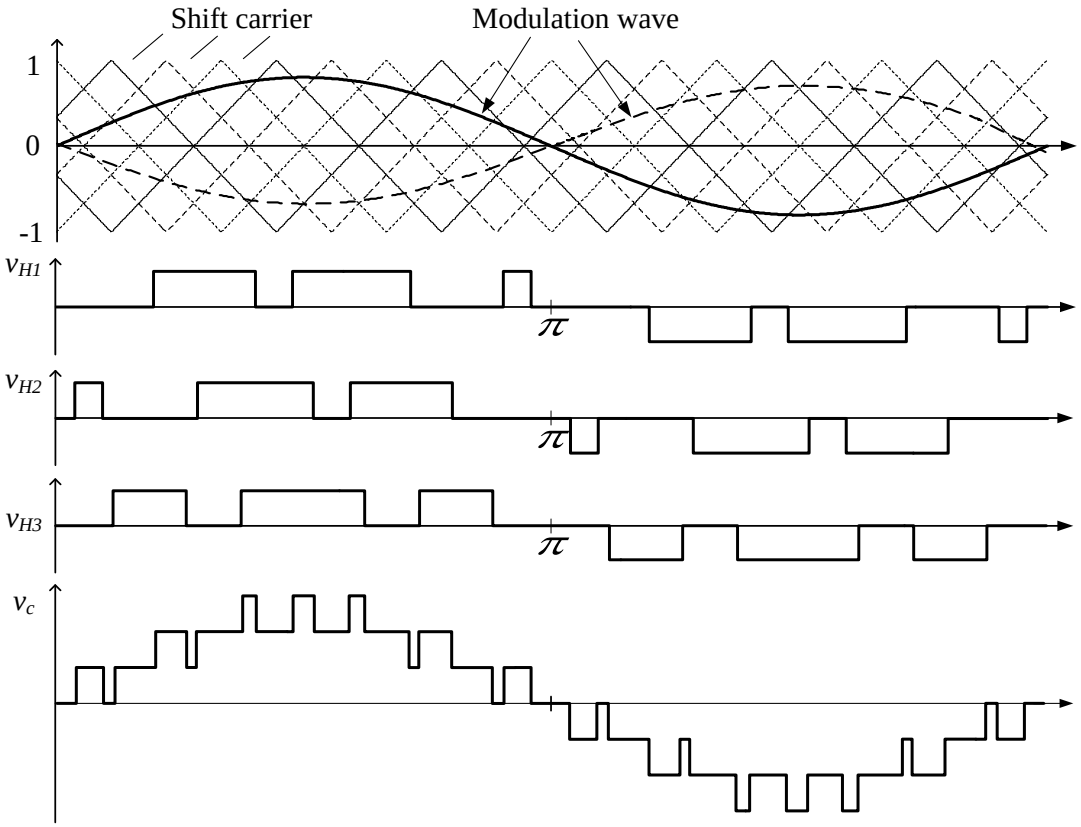

Fig. 5-Schematic diagram of multilevel voltage generation under phase shift unipolar SPWM

3 Simulation results

3.1 Steady state

Fig. 6-7 show the simulation results when the system under steady state.

The values of the parameters of simulation system is shown in Table 1.

Fig. 6(a) is the system voltage v_{sa} and load current i_{la} and Fig. 6(b) shows that the system current i_{sa} and voltage v_{sa} are almost in same phase when STATCOM absorbs reactive power from the system.

the output current of the STATCOM is shown in Fig.6 (c).

Fig. 7 shows there phase output voltages and current of STATCOM.

3.2 Dynamic state

DC voltage controller parameters are designed in this paper to control individual dc capacitor voltage, In order to make the active loss of every H-bridge cell is not identical, add different resistance to each DC side of H-bridge.

Fig. 8 shows the DC voltage control situation, the

first 0.3s, phase angle shift control loop is not active. at that time, it is enabled.

From Fig. 8, it can be seen that ,after 0.3s, the DC voltage are regulated quickly. Voltage balance is achieved after 50ms.

To indicate the dynamic performance of the H-bridge cascaded STATCOM. Fig. 9-11 shows the

Table. 1 Electrical and control parameters for the simulation system

parameters	values
Source voltage u_s/V	220
Line frequency f/Hz	50
DC capacitor capacitance C/μF	1 650
Source inductance L_s/mH	0.2
Filter inductance L_c/mH	5
Filter capacitance C_c/μF	1.88
Sampling frequency f_s/kHz	10
Switching frequency f_c /kHz	10

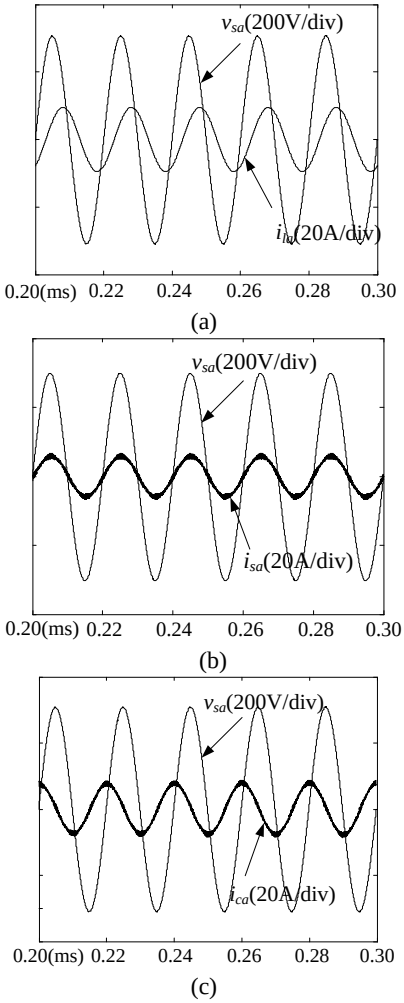

Fig. 6- Simulation results

waveforms in a transient state from full-inductive to full-capacitive operation with a step change at 0.1s, the DC voltage reference is 115V and 125V respectively.

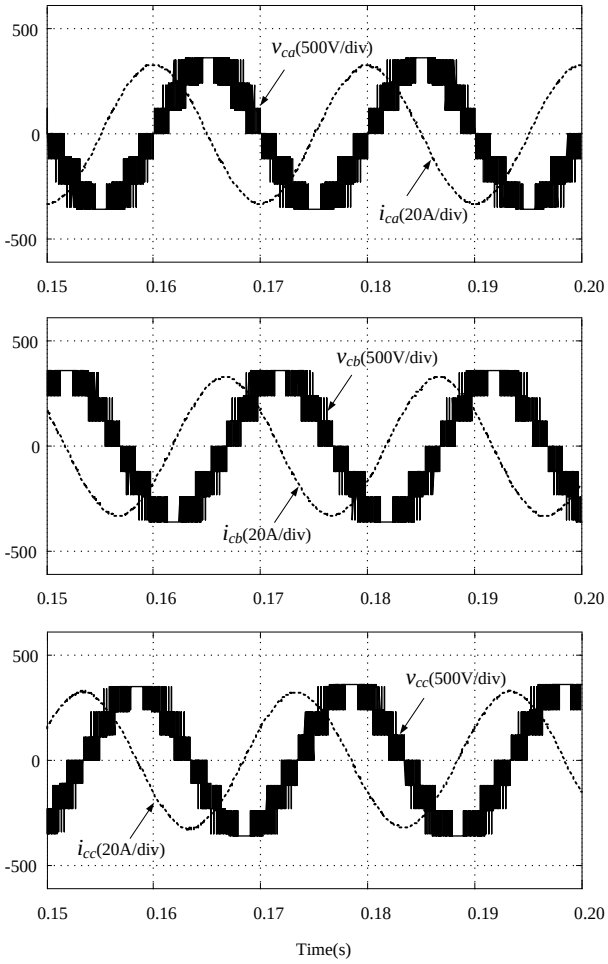

Fig. 7-Output currents and voltages of the STATCOM in steady state

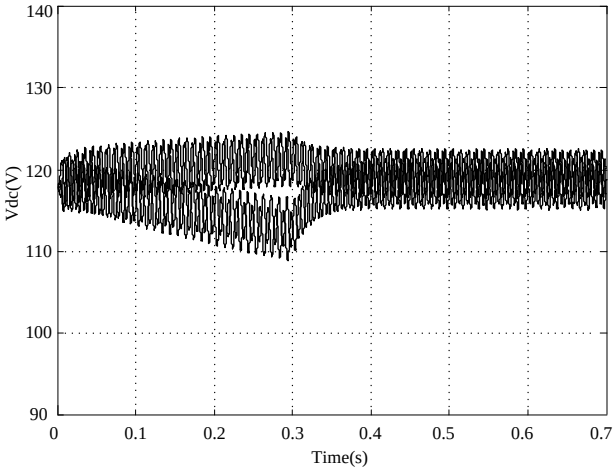

Fig. 8-DC voltage of each H-bridge cell of the STATCOM

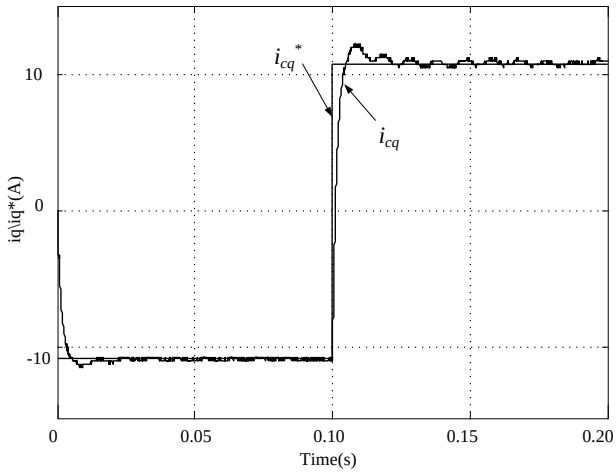

Fig. 9-Reactive current and reactive current reference

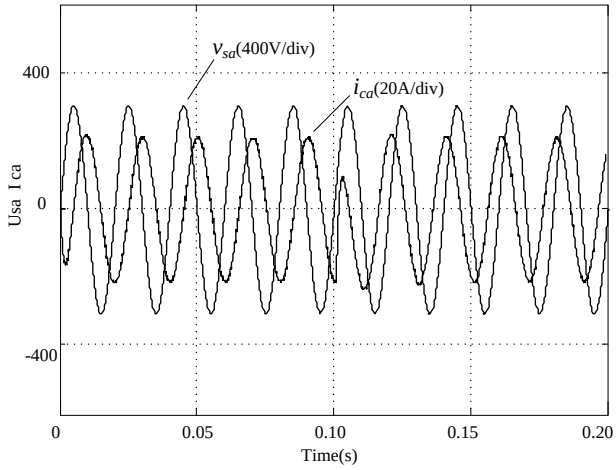

Fig. 10-System voltage and compensate current

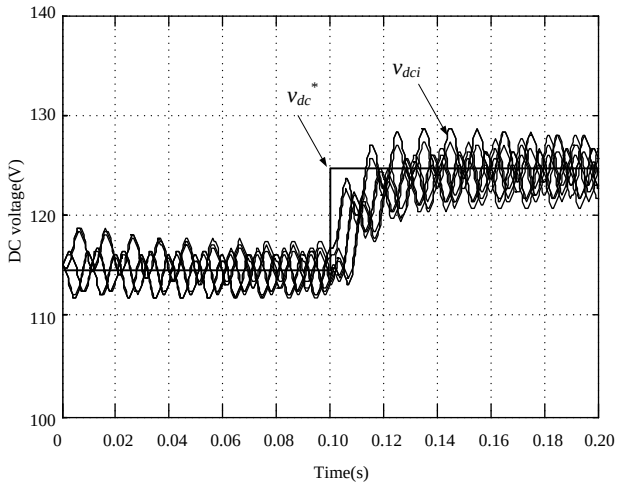

Fig. 11-DC voltages and DC voltage reference

4 Experimental results

The whole control strategy has been realized on a 3 kW five voltage level prototype CHB-based STATCOM to demonstrate the performance. The block diagram is shown in Fig.12. As there are two phase input voltages, two phase input currents and all DC-Link voltages to be measured, consequently, twelve A/D conversion circuits have to be designed. The control algorithm is implemented on a DSP Texas Instruments TMS320F2812 32-b fixed point microprocessor and a XC3S50AN FPGA, where FPGA is used to realize modulation strategy, and DSP is used to complete The entire algorithm, including Clarke transformation, PI regulator, etc.

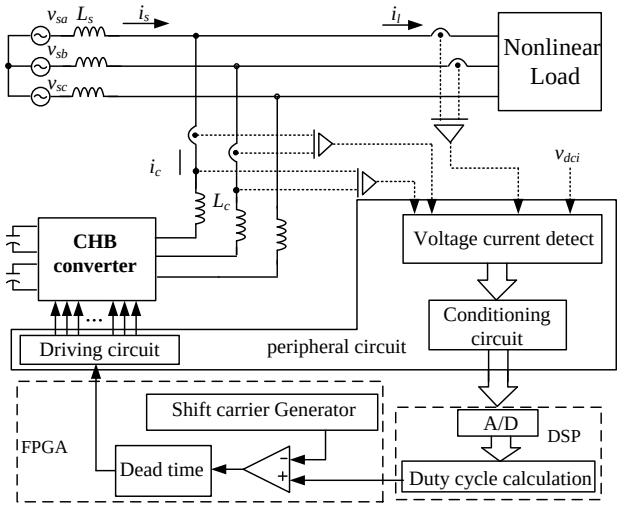

Fig.12- Experimental setup for a prototype CHB-based STATCOM

About FPGA, three main blocks are presented: Clock management block, PWM generation block, Dead time generation block . All programming is done in verilog HDL circuit description language, and each functional block is an entity in verilog HDL. the program of Dead time generation in in verilog HDL are given in Appendix.

Simulate the Dead time generation in Modelsim and the simulation result is shown in Fig.13

Experimental result in steady state shown in Fig.14. it is obvious that the system current i_{sa} and voltage v_{sa} are almost in same phase when STATCOM absorbs reactive power from the system. the a-phase output voltage of STATCOM v_{ca} is a five level voltage.

Experimental results under dynamic state is shown in Fig.15, the variation of dc capacitor voltages (Two dc capacitor voltages in a-phase) when individual balancing control is enabled. Initially, the dc capacitor voltages are unbalanced due to the different power losses of H-bridge units, but when the individual balancing control is activated, the voltage balance is achieved in 0.2s.

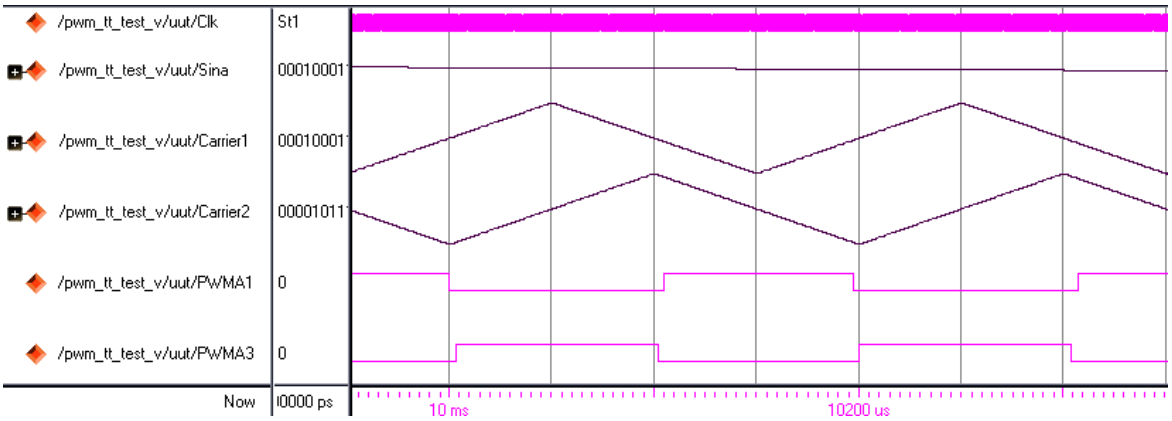

Fig.13- Modelsim simulation results

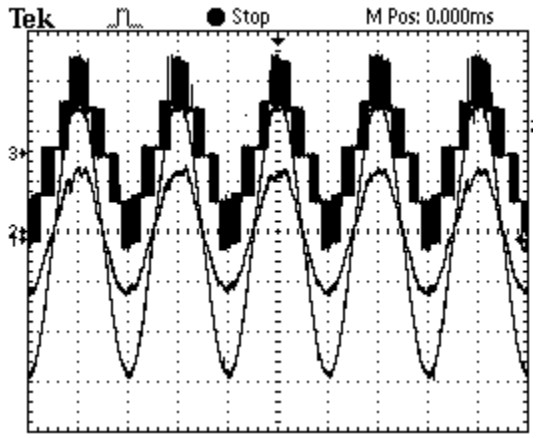

Fig.14- Experimental waveforms in steady state.
(1) source voltage(line-neutral) v_{sa} ,
(2)inverter output voltage (line-neutral) v_{ca} ,
(3)the source current i_{sa} .

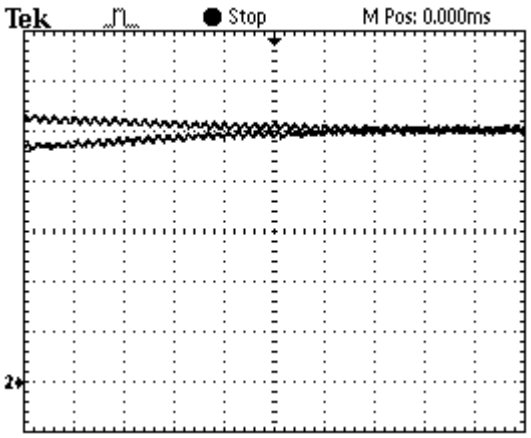

Fig.15- Dc capacitor voltages waveforms when individual balancing control was enabled

5 Conclusion

A novel approach to design PI controller for individual DC voltage balancing control of H-bridge cascaded STATCOM has been proposed in this paper. Generally, using two control loops to maintain DC voltage stable, however, it is not easy to design the controller of the two control loops. This approach can get relatively accurate parameters by finding the relationship of the output and input of the controller.

The simulation and experimental results show superior of the design controller, the DC voltage balancing is accomplished, meanwhile , the system has very fast responses to the step commands.

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Appendix

```
//Deadtime generator

always @(posedge temppwma1, negedge nRst)
 begin
  if(!nRst)
  begin
      PWMA1<=1'b0;
      PWMA3<=1'b0;
   end
  else
    begin
    DTdir<=1'b1;
    PWMA1<=1'b0;
    PWMA3<=1'b0;
 end
```

```
end

always @(posedge Clk, negedge nRst)
  begin
     if(!nRst)
       DTimer<=16'h0000;
   else if(DTdir==1'b1)
      DTimer<=DTimer+1;
   end

 always @(posedge Clk,negedge nRst)
  begin
     if(!nRst)
       DTdir<=1'b0;
   else if(DTimer==16'h0095)  //0096  150
      begin
      DTdir<=1'b0;
      DTimer<=16'h0000;
   end
   end

always @(negedge DTdir, negedge nRst)
begin
   if(!nRst)
   PWMA1<=1'b0;
   else
   begin
  PWMA1<=1'b1;
 // DTimer<=16'h0000;
  end
end

always @(negedge temppwma1, negedge nRst)
begin
   if(!nRst)
   begin
       PWMA1<=1'b0;
       PWMA3<=1'b0;
     end
   else
     begin
     DTdir1<=1'b1;
     PWMA1<=1'b0;
     PWMA3<=1'b0;
  end
end

always @(posedge Clk, negedge nRst)
  begin
     if(!nRst)
       DTimer1<=16'h0000;
   else if(DTdir1==1'b1)
      DTimer1<=DTimer1+1;
   end

 always @(posedge Clk,negedge nRst)
  begin
     if(!nRst)
       DTdir1<=1'b0;
   else if(DTimer1==16'h0095)  //0096  150
      begin
      DTdir1<=1'b0;
      DTimer1<=16'h0000;
   end
end

always @(negedge DTdir1, negedge nRst)
begin
   if(!nRst)
   PWMA3<=1'b0;
   else
   begin
  PWMA3<=1'b1;
 // DTimer1<=16'h0000;
  end
end
```

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