An Off-Chip ESD Protection Strategy for High-Speed USB Interfaces

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Abstract: - The electrostatic discharge (ESD) is one of the most important reliability problems in an electronic product. For Universal Serial Bus (USB) is a hot insertion and removal interface, its components are easily subject to ESD damage. This work focuses on the influence of the using of USB in plugging and/or unplugging impact arisen from ESD. Employing the off-chip protection technique and commercial protection products, the paper proposes an ESD Protection Strategy for USB (EPSU) to effectively enhance ESD robustness. The comparisons among these ESD protection designs are also discussed. Numerous experiments have been made, the EPSU is around 39.6% more efficient for improving the power trace test, 38.7% for the signal trace D+ test, 41.2% for the signal trace D- test, 39.0% for the GND test, and 39.9% for the shield test. All the ESD tests are complied with the test standard of IEC61000-4-2. To conclude, not but the least of USB, the protection strategy can also be applied to some other USB related electronic products.

Key-Words: - Electrostatic discharge (ESD), High-speed USB interfaces, EPSU, Off-chip ESD protection, ESD robustness, 61000-4-2 standard

1 Introduction

The phenomenon of electrostatic discharge (ESD) has been known as a serious problem for integrated circuit (IC) products fabricated by the state-of-the-art semiconductor process technologies because of their smaller size and higher operation frequency. Most of the failures and damages found in ICs were demonstrated to be related to ESD impact [1], [2]. Design the ESD clamp device or circuit for I/O (input/output) pins or power pins is one of the most appropriate technologies to reduce IC failures under ESD-stress conditions. One of the promising ESD protections is to provide the IC with ESD protection scheme to bypass any ESD stress while the IC is in the ESD impact conditions.

The thinner gate oxide and the silicided drain/source terminal in nanoscale complementary metal-oxide-silicon (CMOS) technology seriously degrade the ESD robustness of ICs. Therefore, ESD protection designs must be considered at all I/O pads in ICs against ESD damage. There have been extensive research efforts to improve ESD robustness for CMOS ICs. They were broadly classified as the following three areas : (1) process level improvement (such as the ESD-implant and silicided-diffusion blocking process) [3], [4]; (2) device level improvement (such as the low-voltage triggering silicon-controlled rectifier (LVTSCR) and complementary LVTSCR) [5], [6]; (3) circuit level improvement (such as the gate-coupled, substrate-triggered and inductor-triggered designs) [7], [8]. The recent development of the ESD protection was always focused on the on-chip protection for CMOS technologies. However, as IC becomes smaller and more complex and on-chip area gets more valuable, the external and off-chip protection techniques of the ESD may gain popularity. Furthermore, to achieve more and faster functionality, on-chip ESD protection is often sacrificed in favour of chip performance.

The Universal Serial Bus (USB) is one of the most popular peripheral interfaces in electronic

industry and consumer electronic products [9], [10]. State-of-the-art USB ICs are manufactured on high integration CMOS processes making them extremely sensitive to ESD damage. USB can detect the attachment of an external peripheral and automatically install the relevant software needed to access the device for immediate use. User can plug it into the bus and unplug it any time, but both power and data lines connections are vulnerable to ESD strikes. In order to protect electronic products from ESD damage, protection circuits are often used to bypass the transient ESD energy.Currently study on ESD robustness of the high-speed USB interface is still absent [11], [12]. But some aspects of ESD protection products employed in high-speed signal lines have been reported by several semiconductor manufactories [13], [14], [15]. There is a challenge how to use and integrate the ESD protection products to achieve all-round ESD protection and get better ESD robustness of the USB. In this work, employing the off-chip ESD protection technique, an attempt has been made to design and implement a simple and efficient protection scheme for the high-speed signal lines. The paper proposed an ESD Protection Strategy for USB-EPSU which utilized commercial ESD protection products associated with the ESD immunity test standard IEC61000-4-2 to robust ESD protection. Numerous experiments have demonstrated the effectiveness of the proposed EPSU and verified the feasibility of the protection implementation.

The remainder of the paper is organized as the following manner: Section 2 presents an overview of the IEC61000-4-2 standard test used to evaluate ESD immunity and USB2.0. The commercial ESD protection products are described in Section 3. In Section 4, the EPSU is implemented and confirmed experimentally. Finally, a brief conclusion of this work is drawn in Section 5.

2 IEC61000-4-2 Standard and USB

2.1 ESD Standard

To qualify the ESD immunity of IC products, there are some test methods and standards developed by several organizations. The IEC61000-4-2 standard published by IEC (International Electro-technical Commission) is known as the dominant ESD test method on system-level electrical and electronic equipment for reliability and safety concern. There are four recommended stress levels for contact discharge (conducting surfaces) test mode and air discharge (insulating surfaces) test mode as displayed in Table 1 [16]. In addition, the IEC defined an ESD current pulse with a rise time of 0.7ns to 1ns as highlighted in Fig. 1 and Table 2 [17]. Any ESD pulse generator must be consistent with the specifications. The standard test conditions for ambient temperature and relative humidity are 15°C-35°C and 30%-60% respectively. Contact discharge with a 2-kV ESD pulse was employed in this paper to perform the ESD measurements on USB.

Table 1 Tables of stress levels for IEC61000-4-2

Contact Discharge		Air Discharge	
Level	Test Voltage	Level	Test Voltage
1	2-kV	1	2-kV
2	4-kV	2	4-kV
3	6-kV	3	6-kV
4	8-kV	4	8-kV

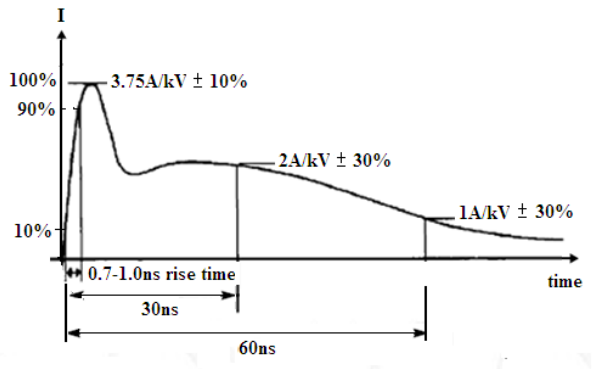

Fig. 1 ESD pulse is defined by IEC61000-4-2 standard

Table 2 Discharge current parameters for IEC 61000-4-2 standard

Level	Test voltage (kV)	First peak (A)	Rise time (ns)	Current at 30ns (A)	Current at 60ns (A)
1	2	7.5	0.7 - 1	4	2
2	4	15	0.7 - 1	8	4
3	6	22.5	0.7 - 1	12	6
4	8	30	0.7 - 1	16	8

2.2 USB2.0

USB ports are available on all recent personal computers and peripheral devices of every variety. An USB 2.0 cable (Fig. 2) has two wires for power (+5 volts and ground), a twisted pair of wires to carry data, and an overall shield [18]. The USB transfers data packets using differential signals and a twisted pair cable to reduce the disturbance of electronic noise and the effects of crosstalk due to electromagnetic interference (EMI). It provides three speed modes: Low-Speed (1.5 Mbps), Full-Speed (12 Mbps) and High-Speed (480 Mbps) modes. For the high-speed mode, the maximum allowed capacitance according to the USB 2.0 specification is about 10 pF overall, otherwise it would distort or deteriorate signal integrity.

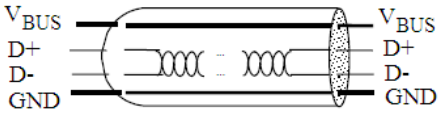

Fig. 2 USB2.0 cable

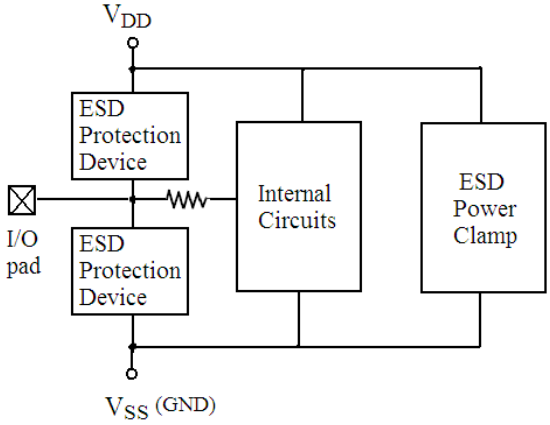

Fig. 3 ESD protection scheme

3 Commercial Products for ESD Protection

ESD events often involve high current (1-10A) and high voltage stress (several kV) on small electronic products. To make highly reliable IC products that are insensitive to ESD threats, an ESD protection scheme is always used to divert high current away from the internal circuitry and clamp high voltage at a safe level, while the electronic product is in ESD-stress conditions [19], [20], [21]. The conventional ESD protection scheme is shown in Fig. 3.

3.1 MLCC

Many designs utilize a capacitor at the I/O pad to integrate the voltage and thereby protect the IC from ESD damage. A Multilayer Ceramic Capacitor (MLCC) is a monolithic block of ceramic composed of hundreds of alternating interleaved layers of ceramic dielectric and metal electrodes stacked together [22], [23], [24]. The MLCC characterized by its high inherent reliability and compactness is the dominant form of ceramic capacitor. It is widely used passive component in modern electronic devices, such as portable products and laptop computers. The MLCC along with higher capacitance and higher voltage ratings usually acts as a bypass capacitor to provide low impedance path for electrical surges, and then prevent IC products from ESD impact. Fig. 4 shows the bypass unwanted ripple voltage (high frequency noise) by using the capacitor.

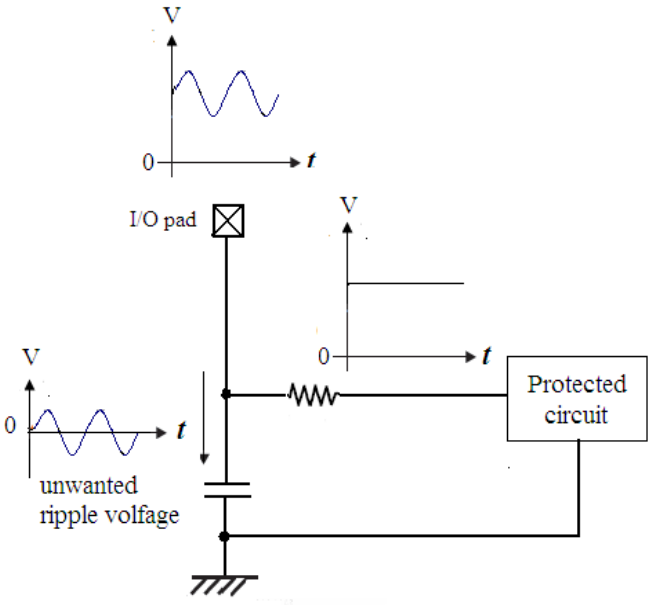

Fig. 4 Typical bypass function of MLCC

3.2 TVS diode array

A transient voltage suppressor (TVS) diode array is composed of multiple, discrete diodes on a single silicon chip. It is commonly applied for protecting ICs from damages due to the inadvertent occurrence of an over voltage imposed onto the IC [13], [14], [15], [24]. The main method of protecting electronic circuits from the effects of ESD is to shunt the ESD current to the ground. In Fig. 5, the power-rail ESD clamp circuit (TVS diode array) is placed between V_{DD} and V_{SS} of power lines of the protected IC to overcome the ESD stresses in the V_{DD}-to-V_{SS} ESD

stresses. The high side and low side diodes are designed with a small size to reduce the I/O (input/output) capacitance and thereby decrease the insertion loss in the high-speed signal lines. The Zener or avalanche diode is an ideal device for ”cutting” or ”clamping” voltage spikes or voltage transients down to low voltage level when it is operated in reverse bias mode. At a time, when a positive transient spike presents on I/O pad, the high side diode provides a forward bias and is clamped by the Zener diode. This establishes an alternative ESD current path and electrical connectivity to both power rails. The clamping voltage on the I/O pad is small and the protected IC circuit will not be damaged. On the other hand, the TVS diode array provides a bypass path to shunt the transient current away from the protected circuit and achieves an ESD robust implementation.

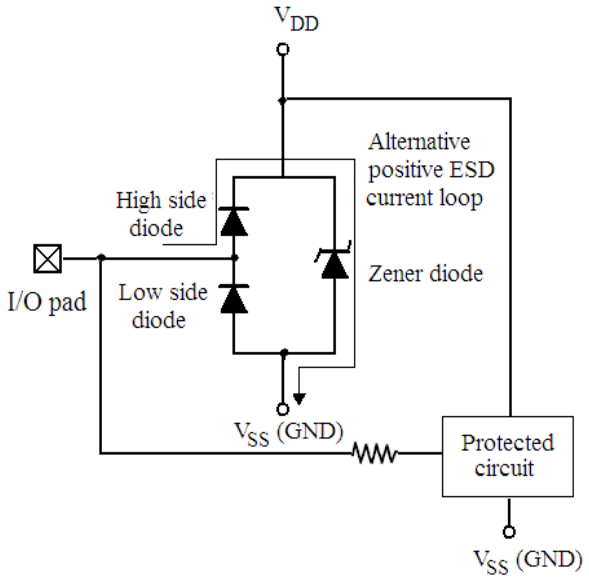

Fig. 5 Schematic diagram to show the ESD current discharging path through the TVS diode array

4 Design and Implementation of EPSU

The ESD immunity tests was built and tested as shown in Fig. 6. The experiment setup included a USB2.0 connection port for the ECS MCP61PM-HM motherboard, a Digital Phosphor Oscilloscope (TDS3054 made in Tektronix) which had a bandwidth of 500 MHZ and a sampling rate of 5GSa/s, a calibrated ESD pulse generator (NSG 438 made in Schaffner) that was built in accordance with IEC 61000-4-2 standard, a high voltage probe which connected the oscilloscope to the south bridge motherboard chip, and a self-made USB2.0 connection test board for the ESD test. The ESD immunity test was performed at 24.0°C and 58% relative humidity.

The layout of the USB2.0 connection port for MCP61PM-HM motherboard is shown in Fig. 7. To verify the performance of the proposed EPSU, the protection products were placed in socket CI3 for USB power trace and socket U20 for USB D+ and D- signals traces. Numerous experiments were made as follows:

- *Original Case*
  Without protection products
- *Protection Strategy 1*
  Insert MLCC (TDK C1608X7R1C104KT) into socket CI3
- *Protection Strategy 2*
  Insert TVS diode array (AZ1015-04S) into socket U20
- *Protection Strategy 3*
  Insert MLCC into socket CI3 and TVS diode array into socket U20

By a self-made USB2.0 connection test board shown in Fig. 8, the calibrated ESD pulse generator was charged to 2-kV and then directly contacted discharge to power VBUS pin, signal D+ pin, signal D- pin, GND pin, and Shield pin respectively.

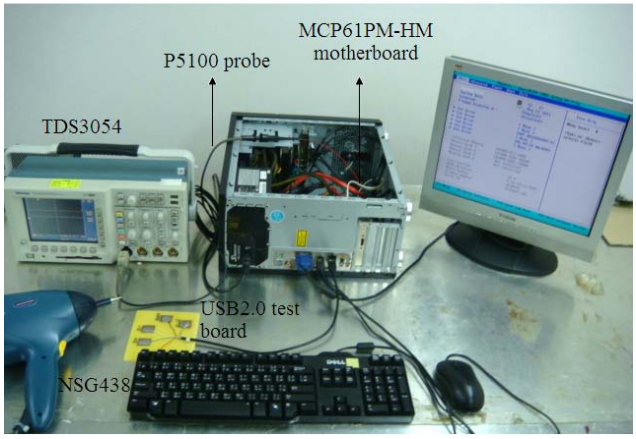

Fig. 6 Experiment setup for the ESD immunity test

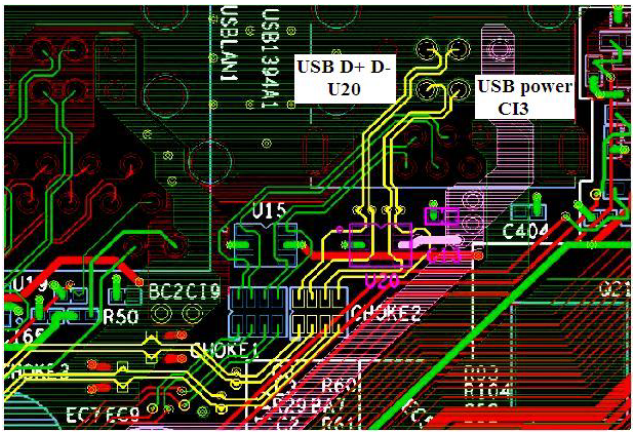

Fig. 7 MCP61PM-HM motherboard

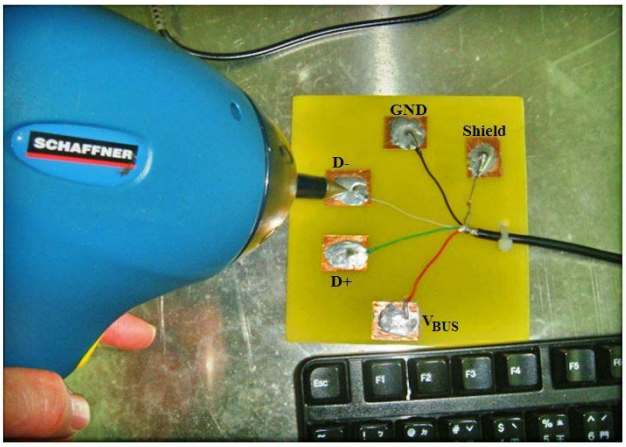

Fig. 8 A self-made USB2.0 connection test board

4.1 Test Results for Original Case

The measured voltage waveforms of the USB pins for Original Case without protection products are shown in Figs. 9-13. The focus here was on the positive and negative transient peak voltages of the USB pins that impact on a 2-kV ESD pulse. For example, the positive transient peak voltages for V_{BUS} pin, D+ pin, D- pin , GND pin, and Shield pin were 788V, 764V, 780V, 780V, and 792V respectively. The Shield pin was rather susceptible to ESD impact.

4.2 Test Results for Protection Strategy 1

Figs. 14 - 18 are the measured voltage waveforms of the USB pins for Protection Strategy 1 with MLCC protection. The results showed that the positive transient peak voltages for V_{BUS} pin, D+ pin, D- pin , GND pin, and Shield pin were reduced to 720V, 704V, 701V, 720V, and 716V respectively. Comparing to the Original Case, the ESD robustness for USB pins were improved by 8.63%, 7.85%, 10.13%, 7.69%, and 9.60% respectively. Additionally, the D- pin had the best ESD robustness for MLCC protection.

4.3 Test Results for Protection Strategy 2

Figs. 19 - 23 are the measured voltage waveforms for Protection Strategy 2 with TVS diode array protection. The results show that the positive transient peak voltages for V_{BUS} pin, D+ pin, D- pin , GND pin, and Shield pin are reduced to 492V, 488V, 461V, 487V, and 492V respectively. Comparing to the Original Case, the ESD robustness for USB2.0 was improved by 37.56%, 36.13%, 40.90%, 37.56%, and 37.88% respectively. Consequently, the TVS diode array protection was rather better than MLCC protection.

4.4 Test Results for Protection Strategy 3

Figs. 24 - 28 are the measured voltage waveforms of the USB pins for Protection Strategy with MLCC and TVS diode array protection. The positive transient peak voltages for V_{BUS} pin, D+ pin, D- pin, GND pin, and Shield pin were significantly reduced to 476V, 468V, 459V, 476V, and 476V respectively. As a result, the positive transient peak voltages were around reduced by 310V. Comparing the results with the Original Case, the performance of the ESD robustness was improved by 39.59%, 38.74%, 41.15%, 38.97%, and 39.90% respectively. Obviously, the proposed Protection Strategy 3 achieved the best ESD robustness and significantly enhanced the performance of the ESD immunity among EPSU.

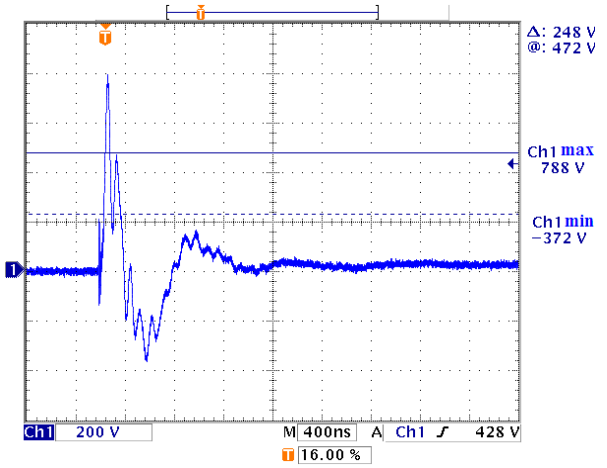

Fig. 9 The waveform of V_{BUS} pin for the Original Case

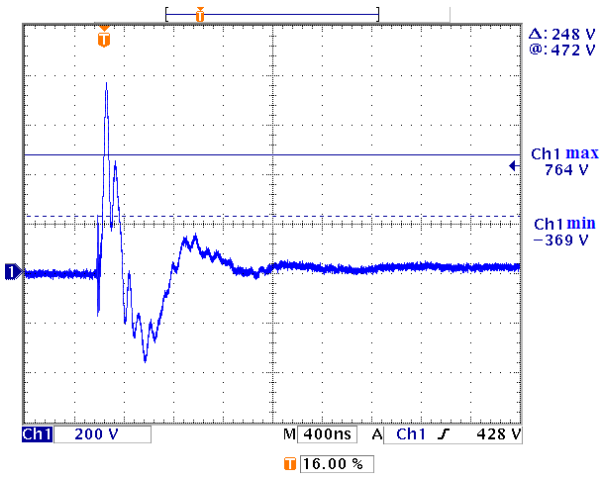

Fig. 10 The waveform of D+ pin for the Original Case

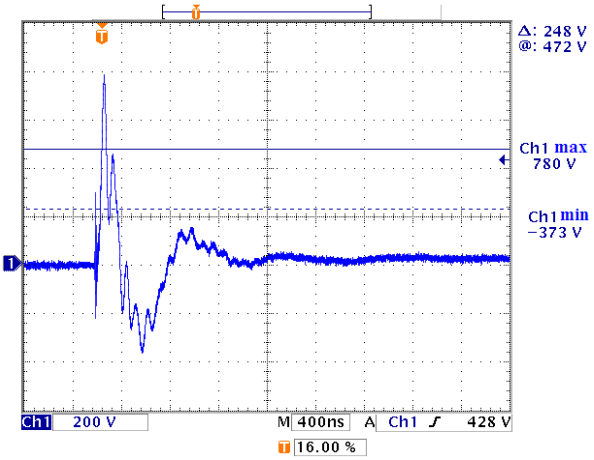

Fig. 11 The waveform of D- pin for the Original Case

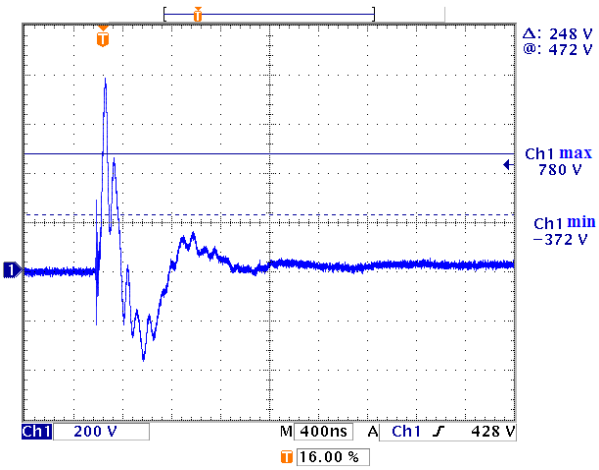

Fig. 12 The waveform of GND pin for the Original Case

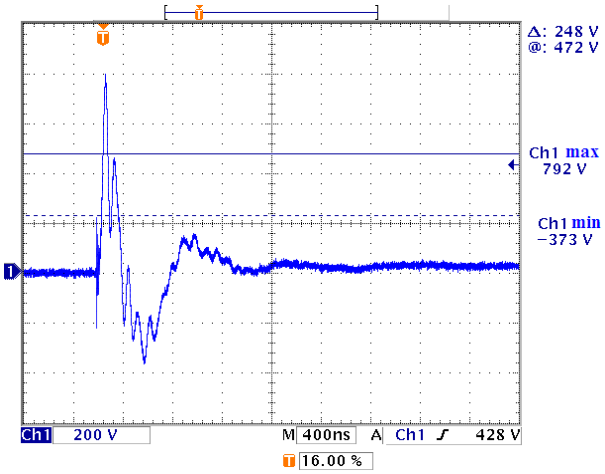

Fig. 13 The waveform of Shield pin for the Original Case

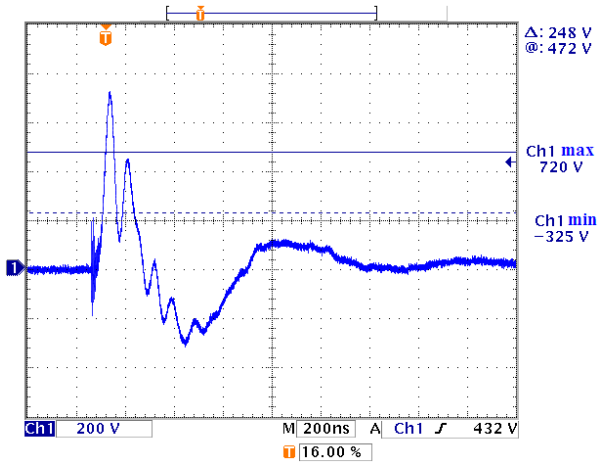

Fig. 14 The waveform of V_{BUS} pin for Protection Strategy 1 with MLCC protection

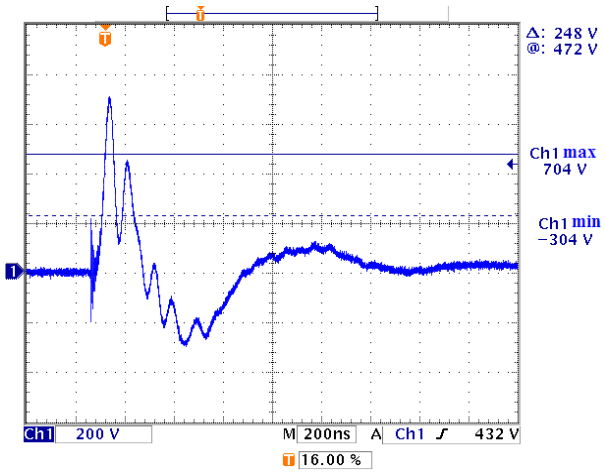

Fig. 15 The waveform of D+ pin for Protection Strategy 1 with MLCC protection

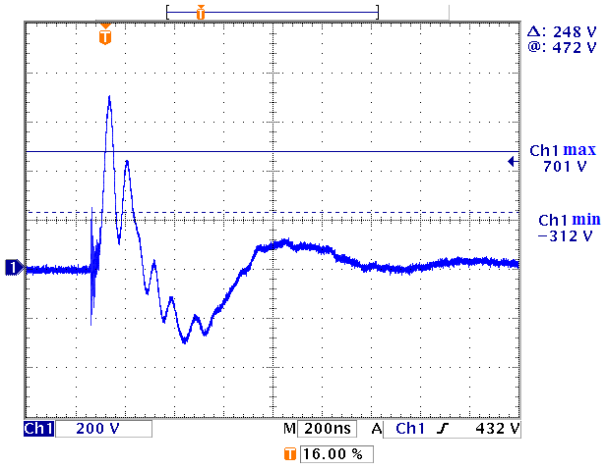

Fig. 16 The waveform of D- pin for Protection Strategy 1 with MLCC protection

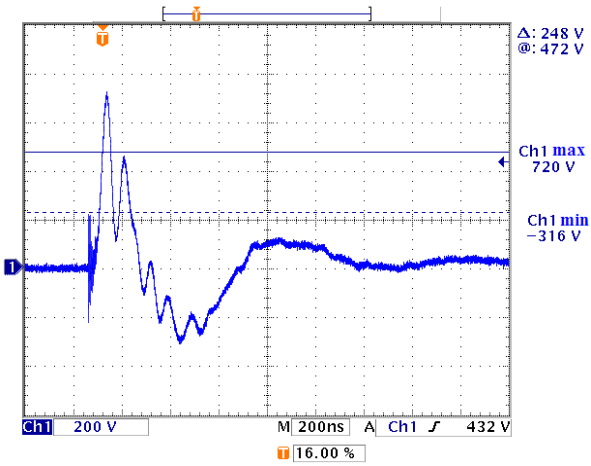

Fig. 17 The waveform of GND pin for Protection Strategy 1 with MLCC protection

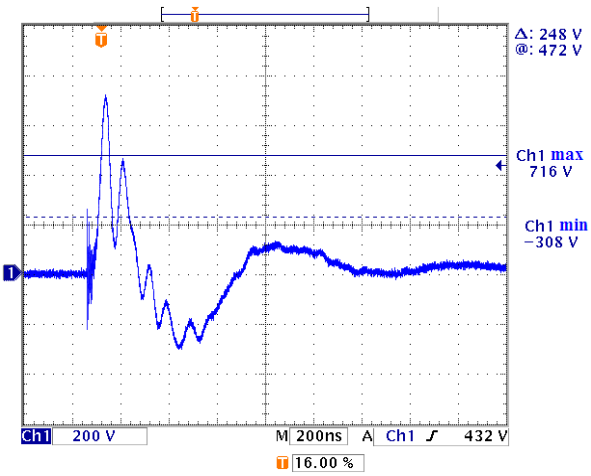

Fig. 18 The waveform of Shield pin for Protection Strategy 1 with MLCC protection

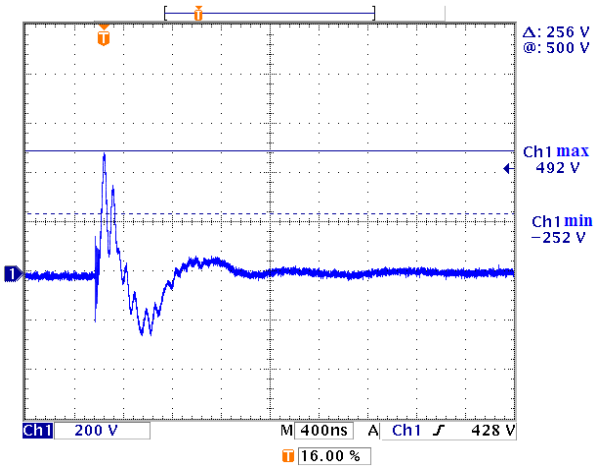

Fig. 19 The waveform of V_{BUS} pin for Protection Strategy 2 with TVS diode array protection

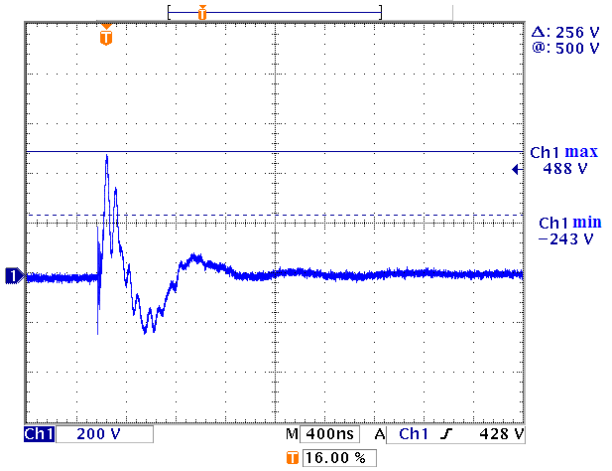

Fig. 20 The waveform of D+ pin for Protection Strategy 2 with TVS diode array protection

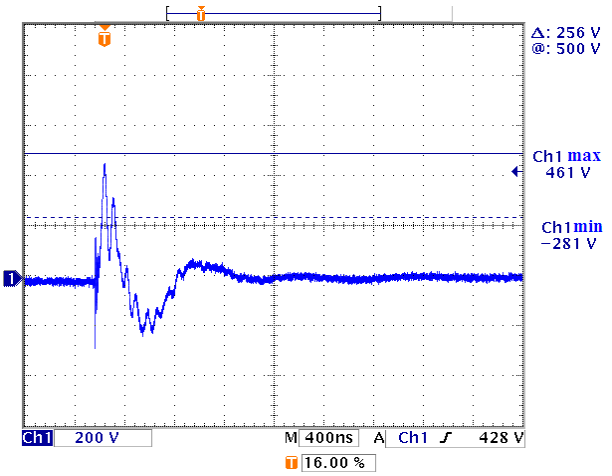

Fig. 21 The waveform of D- pin for Protection Strategy 2 with TVS diode array protection

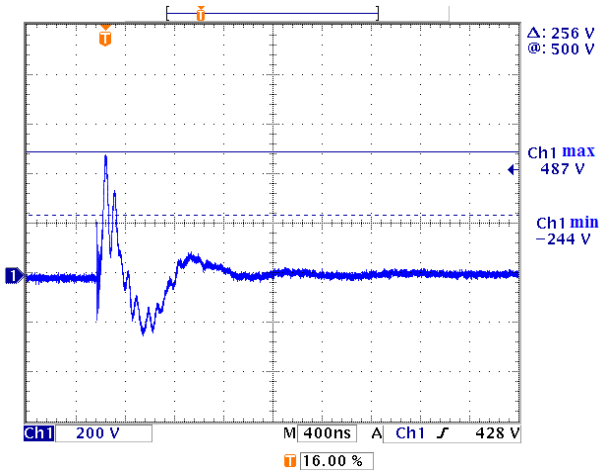

Fig. 22 The waveform of GND pin for Protection Strategy 2 with TVS diode array protection

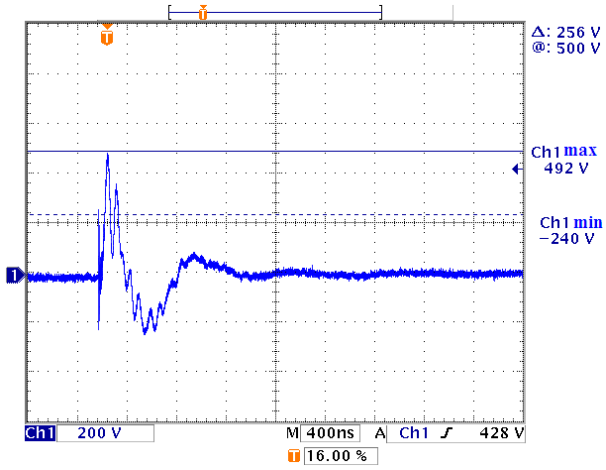

Fig. 23 The waveform of Shield pin for Protection Strategy 2 with TVS diode array protection

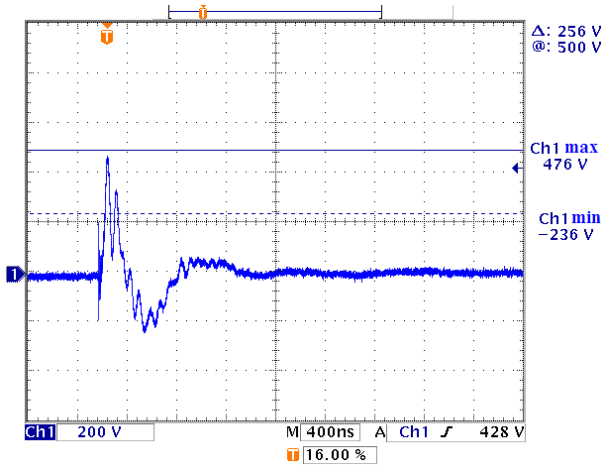

Fig. 24 The waveform of V_{BUS} pin for Protection Strategy 3 with MLCC and TVS diode protection

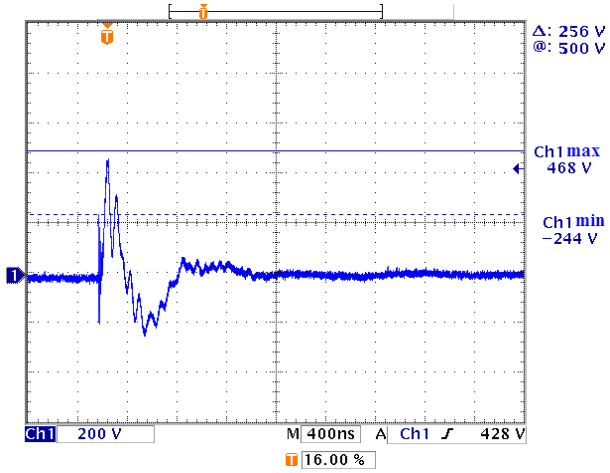

Fig. 25 The waveform of D+ pin for Protection Strategy 3 with MLCC and TVS diode protection

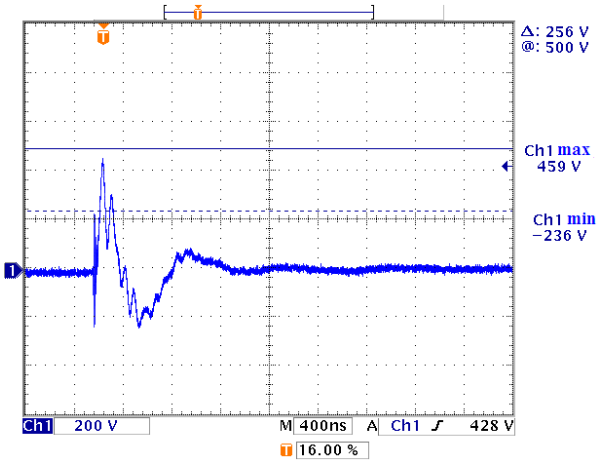

Fig. 26 The waveform of D- pin for Protection Strategy 3 with MLCC and TVS diode protection

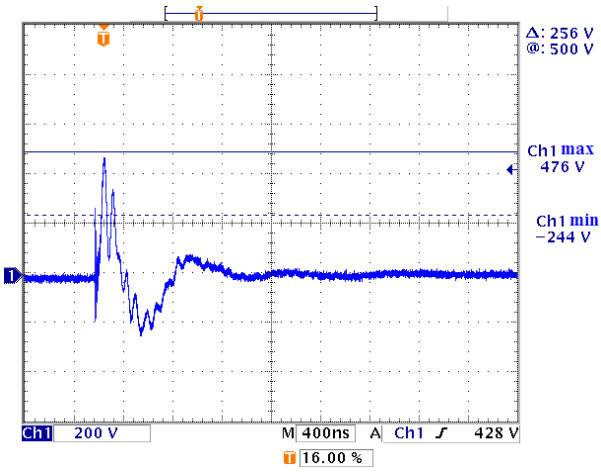

Fig. 27 The waveform of GND pin for Protection Strategy 3 with MLCC and TVS diode protection

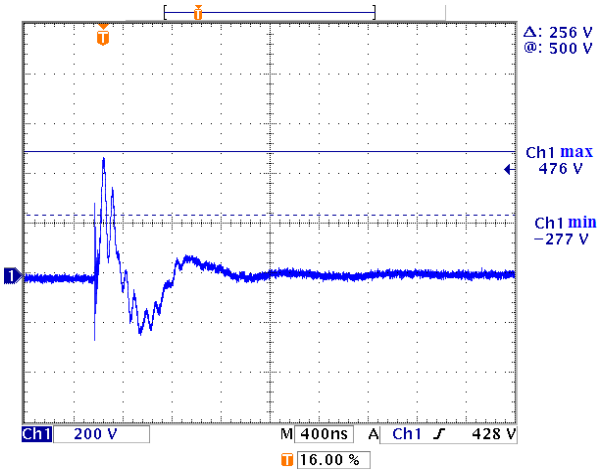

Fig. 28 The waveform of Shield pin for Protection Strategy 3 with MLCC and TVS diode protection

5 Conclusion

The ESD damage problems are today a cause for increasing concern. The paper has proposed a simple and effective protection strategy-EPSU that applied to the high-speed USB interface for MCP61PM-HM motherboard. The improvement of the ESD protection has been verified with numerous experiment tests. Experiment results showed that the developed EPSU was all-round ESD protection and achieved the following attractive features: (1) Power trace protection, (2) Signals traces protection, (3) GND protection, and (4) Shield protection. In the presented EPSU, the ESD protection with MLCC and TVS diode array protection can achieve a significant improvement on the ESD immunity. Additionally, the transient positive peak voltage was reduced by 300V while the USB was hit with a 2-kV ESD pulse. The valuable features of the ESD protection were as follows:

(1) Power trace protection was improved by 39.6%
(2) Signal D+ trace protection was improved by38.7%
(3) Signal D- trace protection was improved by 41.2%
(4) GND protection was improved by 39.0%
(5) Shield protection was improved by 39.9%

Accordingly, all the ESD robustness was around up to 40% improvement. The empirical findings lead us to believe that the work may be helpful to IC industry and ESD researchers.

References:

[1] J. Ackaert and B. Greenwood, Design solutions for preventing process induced ESD damage during manufacturing of interconnects, *IEEE International Conference on IC Design and Technology*, Grenoble, 2010, pp. 98-101.

[2] L. Shanghe, T. Zhiliang, X. Xiaoying, W. Guanghui, and W. Zhangcheng, Study on ESD characteristics and its effect mechanism, *3rd International Symposium on Electromagnetic Compatibility*, Beijing. 2002: 493-496.

[3] M.-D. Ker, C.-H. Chuang, and W.-Y. Lo, ESD implantations for on-chip ESD protection with layout consideration in 0.18-μm silicided CMOS technology, *IEEE Transactions on Semiconductor Manufacturing*, Vol.18, No.2, 2005, pp.328-337.

[4] M.-D. Ker, W.-Y. Chen, W.-T. Shieh, and I.-J. Wei, New layout scheme to improve ESD robustness of I/O buffers in fully-silicided CMOS process. *Electrical Overstress / Electrostatic Discharge Symposium*, California. 2009, pp.1-6.

[5] W. Liu, J.J. Liou, H.-C. Yeh, H. Wang, Y. Li, and K.S. Yeo, Bidirectional diode-triggered silicon-controlled rectifiers for low-voltage ESD protection, *IEEE Electron Device Letters*, Vol.33, No.10, 2012, pp.1360-1362.

[6] H, Fan, L. Jiang, and B. Zhang, A novel SCR structure integrated with power clamp for ESD protection at I/O pad, *IEEE International Conference on Solid-State and Integrated Circuit Technology*, Xi'an. 2012, pp.1-3.

[7] C.-Y. Lin, L.-W. Chu, and M.-D. Ker, ESD protection design for 60-GHz LNA with inductor-triggered SCR in 65-nm CMOS process, *IEEE Transactions on Microwave Theory and Techniques*, Vol.60, No.3, 2012, pp.714-723.

[8] M.-D. Ker and J.-H. Chen, Self-substrate-triggered technique to enhance turn-on uniformity of multi-finger ESD protection devices, *IEEE Journal of Solid-State Circuits*, Vol.41, No.11, 2006, pp. 2601-2609.

[9] T. Yazaki, I. Morita, and H. Tanaka, Demonstration of optical wireless USB 2.0 system with wireless power transfer, *IEEE International Conference on Consumer Electronics*, 2011, pp.11-12.

[10] T.B. Remple, USB on-the-go interface for portable devices, *IEEE International Conference on Consumer Electronics*, 2003, pp.8-9.

[11] B.W. Fon and A. Prajuckamol, Integrated solution for high speed data filtering using

package-in-package approach, *International Electronic Manufacturing Technology Symposium*, Melaka, 2010, pp.1-5.
[12] A. Jahanzeb, C. Duvvury, R. Cline, S. Sterrantino, S. Kothamasu, and A. Somayaji, High voltage ESD protection strategies for USB and PCI applications for 180nm/130nm/90nm CMOS technologies, *Electrical Overstress/Electrostatic Discharge Symposium* (EOS/ESD), 2006, pp. 222-230.
[13] Texas Instruments. System-Level ESD/EMI Protection Guide, 2012.
[14] NXP Semiconductors, AN10753 ESD protection for USB 2.0 interfaces, Rev.3, 2013.
[15] Semtech Corporation, SI08-01 Protection Design Guide for Portable Electronics, Rev.2, 2009.
[16] IEC 61000-4-2 Standard, EMC - Part 4-2: Testing and measurement techniques - Electrostatic discharge immunity test, IEC. 2001.
[17] Z. Yuan, T. Li, J. He, S. Chen, and R. Zeng, New mathematical descriptions of ESD current waveform based on the polynomial of pulse function, *IEEE Transactions on Electromagnetic Compatibility*, Vol.48, No.3, 2006, pp.589-591.
[18] Compaq, Hewlett-Packard, Intel, Lucent, Microsoft, NEC, and Philips. Universal Serial Bus Specification, Rev.2.0, 2000.
[19] S.H. Voldman, ESD Design Synthesis, New York, John Wiley & Sons, 2011.
[20] S.H. Voldman, ESD: Circuits and Devices, New York, John Wiley & Sons, 2006.
[21] M.-D. Ker, C.-Y. Lin, and Y.-W Hsiao, Overview of ESD protection designs of low-parasitic Capacitance for RF ICs in CMOS technologies, *IEEE Transactions on Device and Materials Reliability*,Vol.11, No.2, 2011, pp.207-218.
[22] A.D. Kostic, and S. W. Schwartz, Optimized acoustic microscopy screening for multilayer ceramic capacitors. *Reliability and Maintainability Symposium*, Florida, 2011, pp. 1-4.
[23] M.J. Pan and C.A. Randall, A brief introduction to ceramic capacitors. *IEEE Electrical Insulation Magazine*, Vol.26, No.3, 2010, pp. 44-50.
[24] B. Lee, An overview of ESD protection devices, *Compliance Engineering*, 2001. [Online]. Available: http:// www.ce-mag.com