Explicit Model of Cylindrical Surrounding Double-Gate MOSFET

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Abstract: - We present an analytical and continuous dc model for undoped cylindrical surrounding double-gate (CSDG) MOSFETs for which the drain current and subthreshold model is written as an explicit function of the applied voltages for the wireless telecommunication systems to operate at the microwave frequency regime of the spectrum. The model is based on a unified charge control model developed for this device. This CSDG MOSFET can be used as the RF switch for selecting the data streams from antennas for both the transmitting and receiving processes. We emphasize on the basics of the drain current with drain induced barrier lowering (DIBL) and short channel effects (SCE), for the integrated circuit of the radio frequency sub-system. We analyzed that the drain current is higher, output conductance is lower which shows that the isolation is better in CSDG MOSFET as compared to double-gate MOSFET and single-gate MOSFET. The proposed explicit model satisfies the conformity with the numerical exact solution obtained from the charge control model.

Key-Words: - Charge control model, Cylindrical surrounding double-gate MOSFET, CMOS switch, Double-gate MOSFET, RF switch, VLSI.

1 Introduction

The double-gate (DG) silicon-on-insulator (SOI) MOSFETs with undoped channels symbolize the most promising structure for scaling CMOS devices down to nanometer sizes [1]. Based on ITRS requirements [2], planar bulk MOSFET dimensions continue to be reduced, making the transistors scaling approaching the limit due to the increase of parasitic effects. The excellent gate control abilities of the channel, multiple-gate devices such as surrounding-gate transistors represent the most promising solution to replace conventional bulk transistors and to reach the CMOS scaling roadmap [3-5]. Furthermore, benefits are intensively expected on mobility and variability from integration of undoped or lightly doped silicon in the channel [6]. Besides, the cylindrical structure dramatically reduces corner effects [7] and the threshold voltage may be adjusted due to appropriate gate materials stacking [8]. Due to the gate length reduction, important parasitic effects, commonly known as short channel effects (SCEs), are disturbing the electrostatic behavior of the MOSFET [9]. Indeed, for channel lengths below 100 nm, threshold voltage roll-off and subthreshold swing degradation are clearly identified as major phenomena [10]. As effective models are required to evaluate performances of a specific device in term of circuit design, SCEs must be therefore considered in a compact model for short-channel transistors simulations.

In [11, 12], long channel models for the cylindrical surrounding-gate MOSFET are presented. These two approaches, based on a one-dimensional analysis, ignore short channel effects and cannot be used to model short channel devices. A two-dimensional analysis is then required to reproduce all SCEs when the channel is shrunk down. Moreover, most of published analytical models of SCEs for cylindrical GAA MOSFETs only concern highly doped devices [13], are defined as semi-analytical models [14-16] or valid in the subthreshold region [17], but none is dedicated to model SCEs in all operating regions for undoped

cylindrical surrounding-gate MOSFETs. The use of symmetric DG MOSFETs with ultrathin bodies and ultrathin gate oxides allows to suppress short-channel effects (drain-induced barrier lowering and subthreshold slope degradation), making unnecessary the conventional use of high channel doping densities and gradients. The absence of dopant atoms in the channel decreases mobility reduction by scattering and eliminates random microscopic dopant fluctuations inherent to ultra small dimensions devices which give rise to unwanted dispersion in the turn ON characteristics. Such advanced devices are being fabricated in several configurations including planar, vertical, FinFET, and various other three-dimensional geometries [18, 19]. Multiple-gate MOSFET is one of them which also have been proposed to scale down CMOS technology more aggressively [20].

The conventional scaling rules suggest that in order to minimize the short channel effects, the doping concentration of channel must be increased. However, a high doping level degrades the mobility and therefore lowers the drive current [21]. Another possible alternative necessitates the reduction of gate oxide thickness. However, the extent to which gate oxide thickness can be scaled down is limited by direct tunneling. The surrounding-gate structure [22-25], which has greater control over the channel, was proposed in order to overcome these drawbacks as well as to offer high packing density and steep subthreshold characteristics. The studies [26, 27] have shown that by reducing the thickness of Si-film of surrounding gate structure, greater short channel immunity can be achieved. However, as the thickness of the silicon pillar is reduced, the current drive decreases thus presenting a serious limiting factor to the device performance. Among these non-classical structures, double-gate and surrounding-gate MOSFETs are becoming intense subjects of very large-scale integration research.

Recently, continuous analytic drain current models have been developed for DG [28] and surrounding-gate [29] MOSFETs. Without charge sheet approximation, these two models are derived directly from the Pao–Sah integral [30] with undoped (or lightly doped) silicon body. It has been validated by numerical simulations that these models can continuously cover all the three operation regions without the need for nonphysical fitting parameters. As the device size scales down, the total number of channel dopant decreases, resulting in a larger variation of dopant numbers, and significantly impacting threshold voltage [31].

The surrounding-gate MOSFET is one of the most promising candidates for the downscaling of CMOS technology toward the nanometer channel length range. The surrounding gate allows an excellent control of the channel charge in the Si-film, reduces the short channel effects [29, 32-34]. However, the extension of the applications of the surrounding-gate MOSFET is critically dependent on the availability of compact models of these devices for circuit design and simulation. Standard compact models for bulk or even SOI MOSFETs do not seem to be valid for surrounding-gate MOSFET, since they are based on the charge sheet approximation, which assumes that only a very thin layer at near the silicon and oxide interface contributes to the channel current between source and drain. This approximation is not valid in thin-film surrounding-gate MOSFETs, where there is an inversion or an accumulation of carriers in the whole Si-film, and the whole volume contributes to the channel current.

Flores et. al. [29], presented a physics based current-voltage model for undoped (or lightly doped) SGT MOSFETs, valid and continuous through all operating regimes. Short channel effects were ignored, because the excellent gate control extends the validity of the gradual channel approximation to submicron devices. However, in this model, the current cannot be written as an explicit expression of the applied voltages, and the equations have to be solved numerically. This limits the use of this model in circuit simulation, because it leads to an increase of the simulation time, compared to explicit models.

In this paper, we have presented a design of CSDG MOSFET and its explicit dc model with details to understand the effect of device geometry as of current model. Each of the parameters is discussed separately for the operation of CSDG RF MOSFET structures by *Srivastava et. al.* [35]. This CSDG MOSFET is a replacement of SGT. It contains the two gates around the channel. The new model is based on a unified charge control model, which results from a reformulation of the previous model [29]. The channel current is written in terms of the charge densities at the source and drain ends. Analyzing with the new charge control model, the dependency of the channel charge density on the applied voltages in each operating regime, we proposed approximate explicit expressions of the channel charge densities in terms of the applied bias and infinitely continuous through all operating regions.

Therefore, the channel current becomes an explicit function of the bias. Also, we have demonstrated that our approximate explicit solution fits very well the numerical exact solution of the

charge control model in all operating regimes. Due to its infinite order of continuity, the new model provides flat transitions through all operating regions, which is much desirable in circuit simulation.

The main idea of a CSDG MOSFET is to control the Si channel very efficiently with selecting the channel width to be very small and by applying a gate contact to both sides of the channel. This concept helps to suppress the SCE and leads to higher drain currents as compared with a MOSFET having only one gate. This also provides the low subthreshold slope due to large control over the channel region. Impressive compact and analytical models for the DG MOSFETs, which account for quantum, volume-inversion, short channel effect, DIBL and non-static effects have been proposed by *Ge and Fossum* [36].

Ge and Fossum [36] also suggest that quantum mechanical effects have are negligible for Si-films thicker than 10 nm (means the radius >5 nm), so we did not considered this effect in the proposed model. For films thinner than 10 nm, quantum confinement should be considered. It leads to a reduction of the channel charge density and an increase of the threshold voltage. The organization of the paper is as follows: The CSDG RF MOSFET model is presented in the Section 2. The explicit model of CSDG MOSFET is discussed in the Section 3. The drain induced barrier lowering and Gate leakage current noise model are discussed in the Section 4. Finally, the Section 5 concludes the work.

2 Design of Cylindrical Surrounding Double- Gate (CSDG) MOSFET

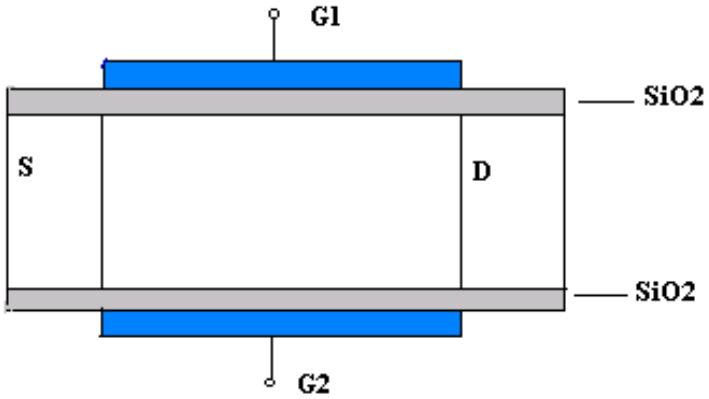
The double-gate MOSFETs, in which a second gate is fabricated opposite to the traditional (first) gate, have been recognized for their potential to better control short channel effects. Such short channel effects limit the minimum channel length at which a MOSFET is electrically well behaved [37, 38]. Figure 1 schematically illustrates the DG MOSFETs. As the channel length of a MOSFET is reduced, the drain potential begins to strongly influence the channel potential, leading to an inability to shut off the drain current with the gate. This short channel effect is mitigated by use of thin gate oxide (to increase the influence of the gate on the channel) and thin depletion depth below the channel to the substrate, to shield the channel from the drain. Gate oxide thickness has been reduced to the point where, at 45 nm CMOS technology, the power drain from gate leakage is comparable to the power used for switching of circuits. Thus, further reduction of the thickness would lead to unreasonable power increase [39].

The DG MOSFET as shown in Fig. 1(a), is a natural extension from a disparage SOI devices. This design reveals the n-type DG MOSFET, similarly we can design p-type DG MOSFET. The double-gate has increased transconductance and a lower threshold voltage. Here we design symmetrical type of device, means the thickness of back-oxide layer is identical as of front-oxide and identical gate materials are used, which allows both gates to control the operation of the device. Since with the symmetrical gate design, the channel area is raised to increase the saturation current and the Si body control is enhanced to reduce the short channel effects.

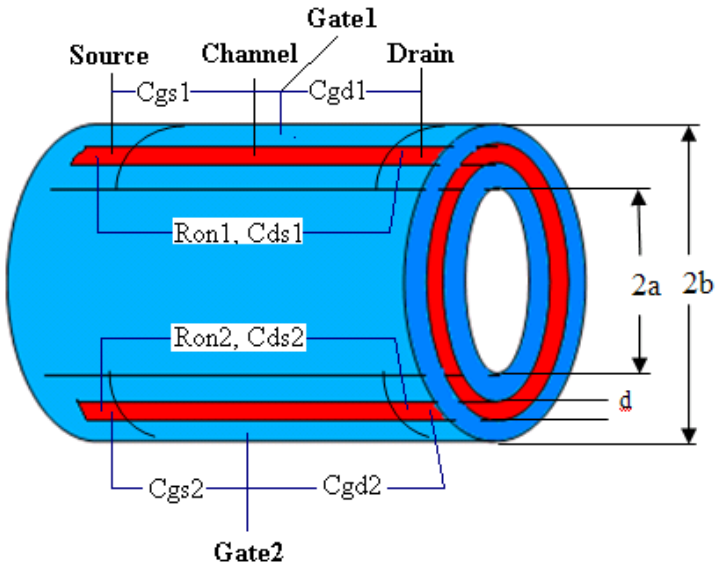
In the DG MOSFET as shown in the Fig. 1(a), when voltage is applied to the gates of device, the active Si region is so thick that the control region of the Si remains controlled by the majority carriers in the region. This causes not one but two channels to be formed. One channel is near the top boundary between Si and the Si insulator and the other one is like wise at the bottom interface. These two channels are separated by enough distance as to be independent of each other. This creates two independent transistors on the same piece of silicon.

Each gate as front-gate (G_1) and back-gate (G_2) can control one half of the device and its operation is completely independent to each other. The total current through the device is equal to the sum of the currents through the separates channels under G_1 and G_2. The relative scaling advantage of the DG MOSFET is about two times. The performance of the symmetrical version of the DG MOSFET is further increased by higher channel mobility compared to a bulk MOSFET, since the average electric field in the channel is lower, which reduces interface roughness scattering according to the universal mobility model [40].

For the design of CSDG MOSFET, we convert the Fig. 1(a), with a circular rotation along any one gate to find a form of cylinder. Then we found the compact model of CSDG MOSFET as shown in Fig. 1(b), which is used for the characterization of resistance, capacitance, electrostatic potentials and current of the doped device. The ultrathin CSDG MOSFET with 5 nm thick body, with $N_A = 10^{20}$ atoms/cc, internal radius, a = 10 nm and external radius, b = 15 nm. It is expected that the saturation current of a surrounding-gate MOSFET should be larger than that of a double-gate MOSFET.



(a)



(b)

Fig. 1. Schematic of the (a) Basic DG n-MOSFET, and (b) CSDG MOSFET.

3 Explicit Model of Cylindrical Surrounding Double-Gate MOSFET

Assuming the gradual channel approximation in an undoped (lightly doped) n-type CSDG MOSFET (Fig. 1b) the Poisson's equation takes the following form:

$$\frac{d^2\psi}{dr^2}+\frac{1}{r}\frac{d\psi}{dr}=\frac{qn_i}{\varepsilon_{si}}e^{q(\psi-V)/kT} \tag{1}$$

where q and n_i are the electronic charge and intrinsic carrier concentration respectively, ε_{Si}, V and ψ are the permittivity of silicon, electrostatic potential, and electron quasi-Fermi potential respectively. It has been assumed that the hole density is negligible compared with the electron density. Equation (1) satisfies the following boundary conditions:

$$\left.\begin{aligned}\frac{d\psi}{dr}(r=0)&=0\\ \frac{d\psi}{dr}(r=a)&=\psi_{\text{int}-surface}\\ \frac{d\psi}{dr}(r=b)&=\psi_{ext-surface}\end{aligned}\right\} \tag{2}$$

where $\psi_{\text{int-surface}}$ and $\psi_{\text{ext-surface}}$ are the internal gate surface potential and external gate surface potential respectively. The current mainly flows along the direction of channel for both the gates. Therefore,

we can assume that is constant along the direction. Equation (1) can be analytically solved as [41, 42]:

$$\psi(r) = V + \frac{kT}{q}\log\left(\frac{-8AkT\varepsilon_{Si}}{q^2 n_i (1+Ar^2)^2}\right) \quad (3)$$

A is related to ψ through the boundary conditions as discussed in the Equation (2). The total mobile charge (per unit gate area) in the proposed model is:

$$Q = C_{ox}[V_{gs} - \Delta\varphi - (\psi_{\text{int}-surface} + \psi_{ext-surface})] \quad (4)$$

where $C_{ox} = \varepsilon_{ox} / R\ln(1+\frac{t_{ox}}{R})$ and $\Delta\varphi$ is the work-function difference between the gate electrode and intrinsic silicon. From Gauss's law, the following relation holds:

$$Q = C_{ox}[V_{gs} - \Delta\varphi - (\psi_{\text{int}-surface} + \psi_{ext-surface})] = \varepsilon_{Si}\left.\frac{d\psi}{dr}\right|_{r=b} - \varepsilon_{Si}\left.\frac{d\psi}{dr}\right|_{r=a} \quad (5)$$

Substituting (3) into (5) leads to:

$$\left.\begin{aligned}\frac{q(V_{gs}-\Delta\varphi-V)}{kT} - \log\left(\frac{8kT\varepsilon_{Si}}{q^2 n_i a^2}\right) + \log\left(\frac{(1+Aa^2)^2}{Aa^2}\right) + \frac{Aa^2}{1+Aa^2} = 0\\ \frac{q(V_{gs}-\Delta\varphi-V)}{kT} - \log\left(\frac{8kT\varepsilon_{Si}}{q^2 n_i b^2}\right) + \log\left(\frac{(1+Ab^2)^2}{Ab^2}\right) + \frac{Ab^2}{1+Ab^2} = 0\end{aligned}\right\} \quad (6)$$

For a given V_{gs}, A can be solved from (6) as a function of V. Here V varies from the source to the drain, being V = 0 at the source end, and V = V_{ds} at the drain end. From this analysis we obtained a charge control model relating the carrier charge density with the bias. For the clarity of working condition of the CSDG MOSFET we discussed it in the following three regions of linear, saturation and subthreshold region.

To obtain a compact drain current model, individual drain currents are obtained in the inner channel and outer channel region near the source end and near the drain end, using the charge density in each part and finally an expression for drain current in linear region is obtained. In the strong inversion region, the drain current is pre dominantly given by the drift tendency and can be expressed as [43]:

$$I_{ds}(x) = 2\pi RQ\frac{\mu_n E_x}{1+\frac{E_x}{E_{sat}}} \quad (7)$$

where $R = a + b$ is the total gate radius of the device due to internal and external surfaces, E_x and E_{sat} are the electric field along the x direction and the critical field respectively, Q is given by (4). To obtain the complete drain current in the linear region, the expression for the drain current Eq. (7) in the gate metal near the source end and the drain end are simplified as:

$$I_{ds} = I_{ds-\text{int}} + I_{ds-ext} \quad (8)$$

where the drain current in terms of the carrier charge densities is calculated as:

$$\left.\begin{aligned}I_{ds-\text{int}} &= \mu\frac{2\pi a}{L}\int_0^{V_{ds}} Q(V)dV\\ I_{ds-ext} &= \mu\frac{2\pi b}{L}\int_0^{V_{ds}} Q(V)dV\end{aligned}\right\} \quad (9)$$

In the saturation region, an expression for the drain current for the CSDG MOSFET is given as [43]:

$$I_{ds}(x) = 2\pi RQ_{sat}v_{sat} \quad (10)$$

where, Q_{sat} is the inversion charge at V_{ds}=V_{sat} . Since both gates are symmetrical so V_{sat} is same for both the gates and it can be written from (4) as:

$$Q_{sat} = C_{ox}(V_{gs} - V_{th} - V_{sat}) \quad (11)$$

Using Eq. (11) in Eq. (10) drain current at saturation region become

$$I_{ds}(x) = 2\pi RC_{ox}(V_{gs} - V_{th} - V_{sat})v_{sat} \quad (12)$$

where v_{sat} is the saturation velocity.

The sub-threshold current is the leakage current that affects the dynamic circuits and determines the standby power consumption in VLSI. It is important to mention that despite its composition of both terms of drift and diffusion currents and due to the weak inversion region the diffusion one dominates. In this case, the current is proportional to the electron concentration at the virtual cathode. By adopting in a similar way the methodology proposed for CSDG MOSFET, an explicit analytical subthreshold drain current equation is derived using the minimum surface potential [44], as follows:

$$I_{ds} = \frac{2\pi R\mu C_{ox}}{L}(V_t^2)e^{(V_{gs}-V_{th})/2V_t}(1-e^{-V_{ds}/V_t}) \quad (13)$$

The sub-threshold regime mainly describes the switching behaviour of the device and is particularly important for low power applications.

4 Drain induced barrier lowering and Gate leakage current noise model

As the channel length reduces, short channel effects such as drain induced barrier lowering (DIBL) adversely affect the device behaviour. DIBL causes the channel charge in short channel devices to be partially controlled by the drain potential rather than the gate potential and this causes threshold voltage roll-off and deteriorates the device performance. Therefore, it becomes necessary to incorporate DIBL effect in the CSDG MOSFET in order to develop an accurate drain current model. DIBL for the CSDG MOSFET is defined as [44]:

$$DIBL = V_{th_1}(at\ V_{ds_1}) - V_{th_2}(at\ V_{ds_2}) = V_{th(Linear)} - V_{th(Saturation)} \quad (14)$$

In the proposed CSDG MOSFET device with ultrathin gate oxide, direct tunnelling is dominant mechanism of gate-leakage current. This current can be divided into six major (three due to internal gate and three due to external gate) contributions: the gate to inverted channel current (I_{gc1} and I_{gc2}), the gate to source (I_{gs1} and I_{gs2}) and the gate to drain (I_{gd1} and I_{gd2}) components due to the path through the source and drain overlap regions. The gate-leakage current noise performances of a CMOS device can be characterized in terms of the gate noise current spectrum, which can be modelled by [45, 46]:

$$S_P^2 = S_w^2 + \frac{A_f}{f^{\alpha_f}} \quad (15)$$

where S_w describes the white noise component of the spectrum and A_f is a power coefficient of the 1/f noise, α_f determines the slope of this low frequency noise contribution, this second term shows the Flicker noise. The term S^2_w in (15) can be expressed by means of the shot noise law $S_w^2 = 2q(I_{g1} + I_{g2})$, where I_{g1} and I_{g2} are the sum of the absolute values of each gate current contribution for a given bias condition [47, 48]. The thermal noise associated with the substrate resistance can produce measurable effects at the main terminals of the device. The thermal noise produced by the substrate resistance R_{sub} modulates the potential of the back-gate, contributing some noisy drain current of a MOSFET is given by:

$$i_{nd,sub}^2 = 4kTR_{sub}g_{mb}^2\Delta f \quad (16)$$

But for the proposed CSDG MOSFET, bulk/substrate is not present, so $R_{sub} = 0$ which provides $i_{nd,sub}^2 = 0$.

Hence no noise is produced by the substrate resistance. In addition to the drain current noise, the thermal agitation of the channel charge has another important consequence as gate noise. The fluctuation channel potential couples capacitive into the gate terminal, leading to a noisy gate current. The noisy gate current may also be produced by thermally noisy resistive gate material. Although this noise is negligible at low frequencies, it can be dominate at radio-frequencies. The conventional scaling rules suggest that in order to minimize the short channel effects, the doping concentration of channel must be increased. However, a high doping level degrades the mobility and therefore lowers the drive current.

Another possible alternative necessitates the reduction of gate oxide thickness. However, the extent to which gate oxide thickness can be scaled down is limited by direct tunnelling [49-51]. The CSDG MOSFET, which has greater control over the channel, was proposed in order to overcome these drawbacks as well as to offer high packing density and steep subthreshold characteristics. By reducing the thickness of Si-film of CSDG MOSFET, greater short channel immunity can be achieved. However, as the thickness of the silicon pillar is reduced, the current drive decreases thus presenting a serious limiting factor to the device performance.

5 Conclusions

We have presented an analytical model for undoped CSDG MOSFETs and provide the explicit solutions for the intermediate parameters that were used in previous DG MOSFETs models, which can be verified by numerical simulations. The model is based on a unified charge control phenomena from which we derived a channel current expression in terms of the channel charge densities at the source and drain ends of the channel.

The model becomes explicit by using appropriate expressions for the channel charge densities in terms of the applied voltages. The channel charge distribution in the Si-film is adequately accounted for the charge control model. Besides, the channel current expression presents an infinite order of continuity over all operating regimes, which makes the model very promising for circuit simulation.

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