A proposed eleven-transistor (11-T) CMOS SRAM cell for improved read stability and reduced read power consumption

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Abstract: Due to scaling of MOS devices, SRAM read stability imposes a serious concern for future technology. The conventional 6T cell becomes more vulnerable to external noise due to voltage division between the access and the pull-down transistors in the inverter. This paper discusses the design and implementation of 11-T SRAM cell to improve the read stability and read power reduction. During read operation storage nodes are completely isolated from the bit lines. The average read power consumption reduces approximately 12% compared to the 6T cell due to lower discharging activity at read bitline and low leakage current. The standby power consumption in the proposed cell is larger than the 6T cell which can be reduced by using minimum size transistors. The read signal noise margin (RSNM) is enhanced by 2x compared to the 6T cell due isolation of read and write circuits. The proposed cell is capable of operating at a supply voltage as low as 330mv and can be used in ultra-low power circuit applications.

Key words: SRAM cell, read stability, SNM, power consumption, read/write access time, leakage current

I. Introduction

Due to advancement in technology, it is possible to design chips for higher package density, low power consumption and higher performance [1][2][3]. One has to scale down the feature size of the CMOS devices to meet these objectives. Technology scaling results in a significant increase in leakage currents in CMOS device. Leakage power consumption is a major contributor for power consumption [4][5][6] and has become a serious concern in SRAM cells [7][8][9][10][11][12]. In the modern technology when the feature size is reduced drastically, supply voltage and threshold voltage must be also reduced in the same pace. The decrease in power supply reduces the power consumption quadratically at the cost of degraded stability and access delay. The cell stability (read stability plus write-ability) in SRAM cell is studied in detail because it is an important design criterion [13][14]. The read stability is measured in terms of static noise margin (SNM) which is defined as the minimum noise voltage necessary to flip the state of an SRAM cell [15]. The read stability of the conventional 6T SRAM cell is degraded and the external noise can easily destroy the stored data in the 6T SRAM cell due to direct

access paths from bitline to storage node. To overcome this problem, various SRAM cells have been proposed [16][17][18][19][20]. Each proposed cells have their own limitations. For example, the proposed cells in refs [18][19][20] have hardware burden which gives extra cost. In the novel 9-T cell [16] due to leakage path during read operation, the read power consumption has not reduced significantly. In this paper a new 11-T SRAM cell is proposed to improve the read stability and to reduce the leakage power consumption during read operation. The proposed SRAM cell uses separate circuits for the write and read operations. The storage nodes are completely isolated from bitlines during read operation and hence improve the stability. Since the discharging activity factor of the proposed cell is lower than 1, the average read power consumption is approximately 12% less compared to the 6T cell. The leakage power consumption in the proposed cell is reduced 33.33% compared to the novel 8T cell for minimum transistor width. The proposed cell can be used in extremely rough conditions ($T=120^0C$ and $T=-20^0C$) with minimal read power consumption.

The rest of the paper is organized as follows: Section II presents the architecture and read/write operation of the proposed SRAM cell. Section III describes the impact of the proposed cell on the cell stability, read power, read delay and cell area. The simulated results were compared with the published cells and the conventional 6T cell. A brief conclusion is provided in the section IV.

2. Architecture of the proposed 11-T SRAM cell

The architecture of 11-T SRAM cell is shown in Fig.1. The upper part of the circuit (encircled with dotted line) is essentially 6T cell and is used to perform write operation. Transistors M8, M9 and M11 are used for reading the content of the storage nodes (Q, nQ). Read access is single ended and occurs on the separate bitline (RBL). The read wordline RWL is distinct from the write wordline (WL). To store the data at the storage nodes Q and nQ, the read wordline RWL is set to be low. Transistors M7 and M10 are used to decouple the storage nodes (Q and nQ) from read bitline during write operation and standby mode so that proposed cell has distinct write and read ports. Due to separate read and write circuits, the previously stored data remains intact in the cell during next write operation as long as RWL=0. The switching behavior of the transistors M8 and M9 is decided by the voltage at the storage nodes. Since no current flows between storage nodes and bitlines, the read SNM is almost equal to ideal hold SNM. Now, we will consider the read and write operations of the proposed cell separately.

2.1Write Operation

During write operation RWL is set to low (RWL=0). The write operation in the proposed cell is performed by setting the bitlines (BL and BLB) to the desired logic before asserting $WL=V_{dd.}$Thewrite circuit of the proposed cell is similar to the conventional 6T cell.

2.2Read Operation

The read operation in the proposed SRAM cell typically involves precharging of the read bitline ($RBL= V_{dd}$) followed by reading the content of the cell through the read access transistor M11. Now, consider two read cases; when node "Q" stores data "1", transistor M8 turns ON and transistor M9 turns "OFF". The ON transistor M8 connects the node N to reference voltage V2 ($=V_{dd}$). Now set RWL=high. Since read bitline (RBL) and node N are almost at the same voltage level, RBL does not discharge appreciably in this case. This is equivalent to read "1" operation. When stored data at node "Q" is zero, transistor M8 turns OFF and transistor M9 turns ON. The ON transistor M9 connects the read path to the ground and RBL discharges through transistors M11 and M9. This effect builds a voltage difference between RBL and local reference line which can be sensed by high speed single-ended differential current sense amplifier and interpreted as logic "0". Since storage nodes Q and nQ are completely isolated from bitlines BL/BLB; the logic at the node Q is strictly maintained at the ground level.

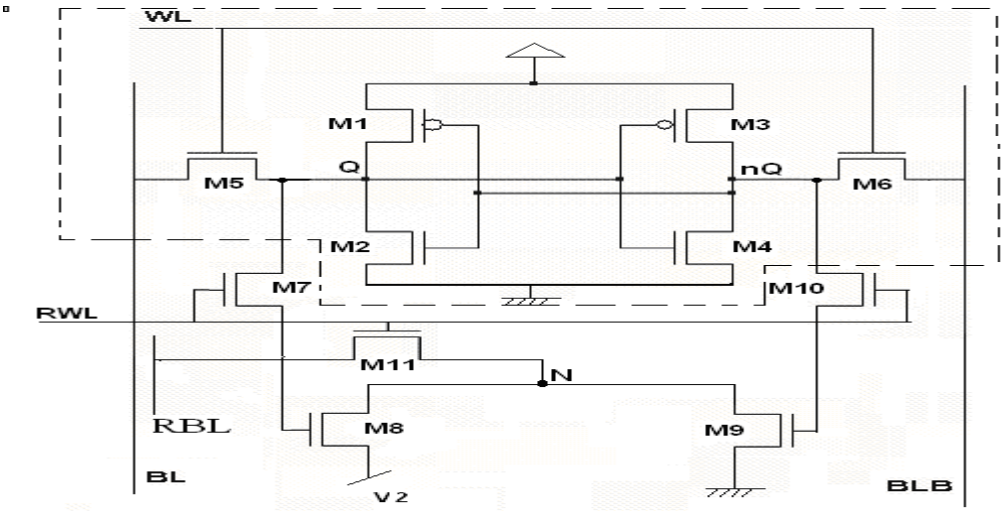

Fig.1: Architecture of the proposed 11-T SRAM cell

3. Simulation Results and Discussion

The layout of the proposed cell and the 6T cell, as shown in Fig. 2, are drawn with the help of MICROWIND3 tool for 90nm CMOS technology. We have performed the SPICE simulation with the help of BSIM4 based transistor model in terms of the read stability, read power consumption and read delay for parameters $V_{th(n)}$=$|V_{th(p)}|$=350mV, V_{dd}=1V.

In this paper, read access delay (excluding the peripheral devices) is defined as the time elapsed from asserting RWL=high to sufficient-voltage drop between bitlines for correct data sensing. Similarly, write access delay (excluding peripheral devices) is defined as the elapsed time from which asserting WL=high to the states of both nodes Q and nQ become steady.

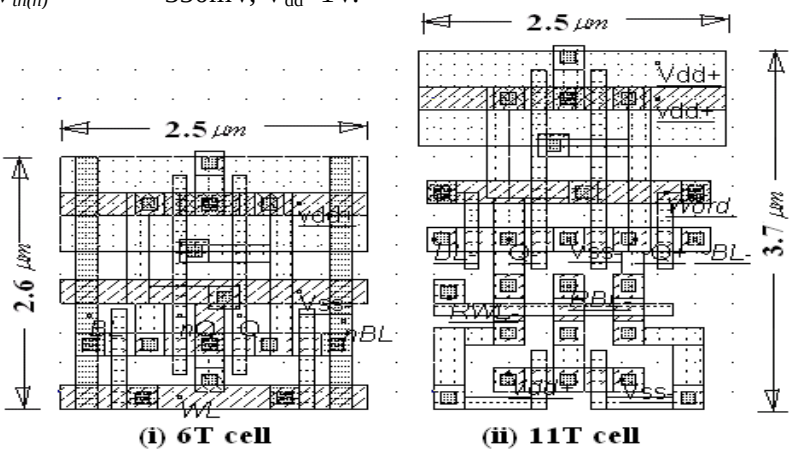

Fig.2: Layout of the conventional 6T SRAM cell and proposed 11-T SRAM cell

Table 1 gives the average write power consumption and delay for the proposed cell, the conventional 6T SRAM cell and other published cells in the literature. Due to larger bitline capacitance the average write power consumption and write access delay of the proposed cell is larger than the 6T cell and 130mV cell.

Table1: Write power consumption and write delay

Type of SRAM cell	Average write delay (ps)	Average overall power consumption (µWatt)
6-T cell	46	1.354
10-T Subthreshold-[17]]	16	2.091
130mV[20]	42	0.893
11-T cell	47	1.632

The power dissipated in bitlines (due to increase in height of the proposed cell) is only a part of the total cache power consumption. The increased power consumption in switching the wordline can be compensated by equalizing the width of the proposed cell and the 6T layouts.

Table 2 gives the leakage power consumption during standby mode (RWL=0=WL) in the proposed cell and the 6T cell. The proposed cell consumes 1.75x more power compared to the 6T cell. The reason for this larger power consumption is; when transistors M11 and M7 are off, the gate voltage of transistors M8 and M10 will remain at their last driven values for a fair bit of time. Hence, it is possible that the internal node N remains at ground through ON transistor M9 (after read 0 operation) and creates worst case leakage condition on the read bitline. Since in the proposed cell, the read and write circuits are isolated from each other, minimum size transistors can be used. The leakage power consumption can be reduced by scaling the transistors M7, M8, M9, and M10 to (W/L) =1 as reported in table 2.

Table 2: Leakage current in 11T cell and 6T cell during hold mode

Types of SRAM cell	Leakage Power Consumption (nW)	
	(W/L)=2 for all transistors in both cells	(W/L)=1 for M7, M8, M9, M10 in proposed cell. (W/L)=2 for all transistors of the 6T cell
6-T cell	4	4
11-T cell	7	3

Fig. 3(a) shows the read “0” power consumption at different oxide thickness for 6T cell, proposed cell and other cells. It is observed that proposed cell consumes lower power than the other cells except D2AP cell which confirms lower gate tunneling leakage current in the proposed cell. Due to lower leakage current and lower discharging activity at the read bitline power consumption in the proposed cell is lower irrespective of the technological node. The average read power saving is approximately 12% compared to the 6T cell for 90nmCMOS technology. The read power saving is 86.65% in the proposed

cell compared to 84% in the 6T cell as the technology scale down to 65nm from 120nm (Table 3(b)). This shows that the proposed cell is effective to restrict the leakage current even at lower process technology.

Fig. 3(b) shows the variation of read 1 power consumption at different power supply for 90nm CMOS technology. As the V_{dd} reduces power consumption reduces for all the cells. Irrespective of the power supply, the proposed cell consumes lower power than the other cells. The reduction is more at larger power supply due to lower leakage current and discharging activity at RBL.

The bitline power consumption in the proposed cell varies slightly compared to other cells as the read bitline capacitance increases (Fig. 3(c)). This is due to lower discharging activity at the read bitline.

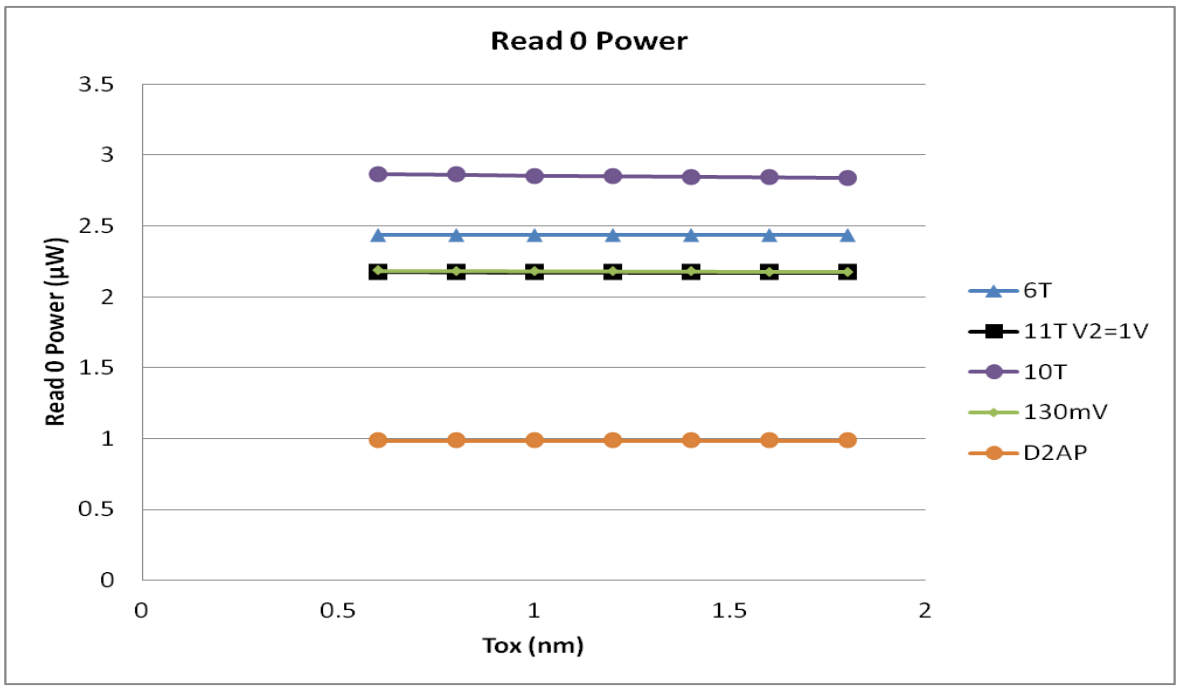

Fig. 3(a): Read 0 power consumption at different oxide thickness.

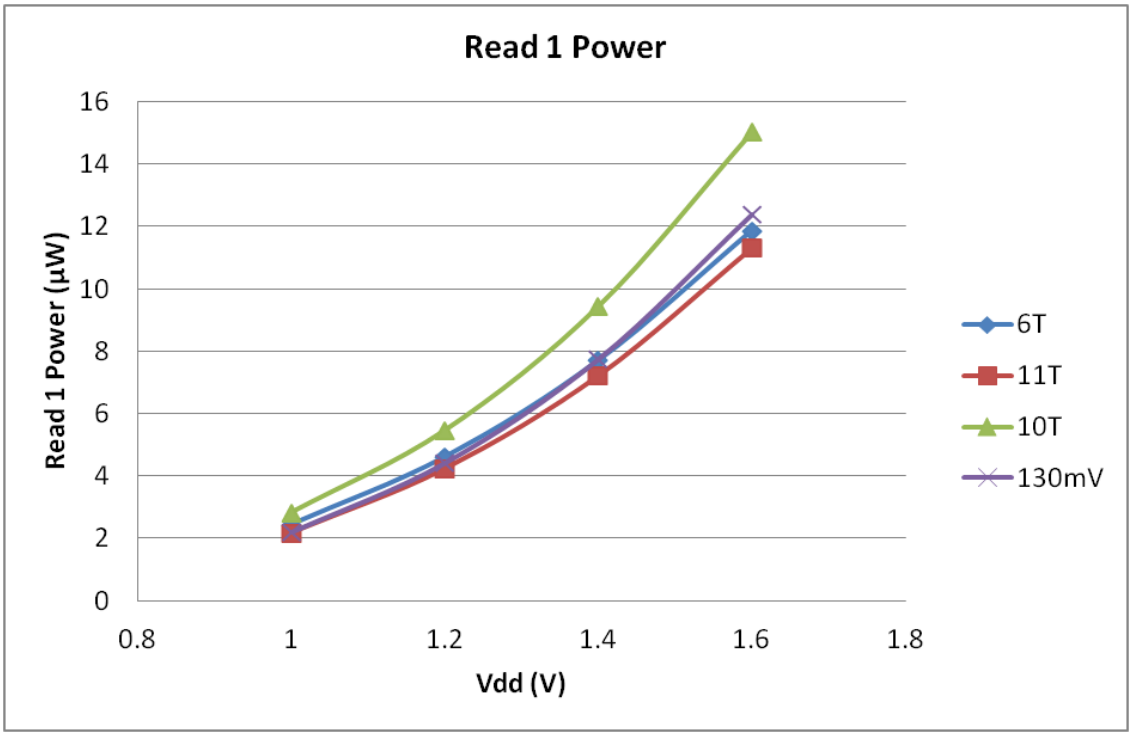

Fig. 3(b): Read"1" power consumption at different power supply.

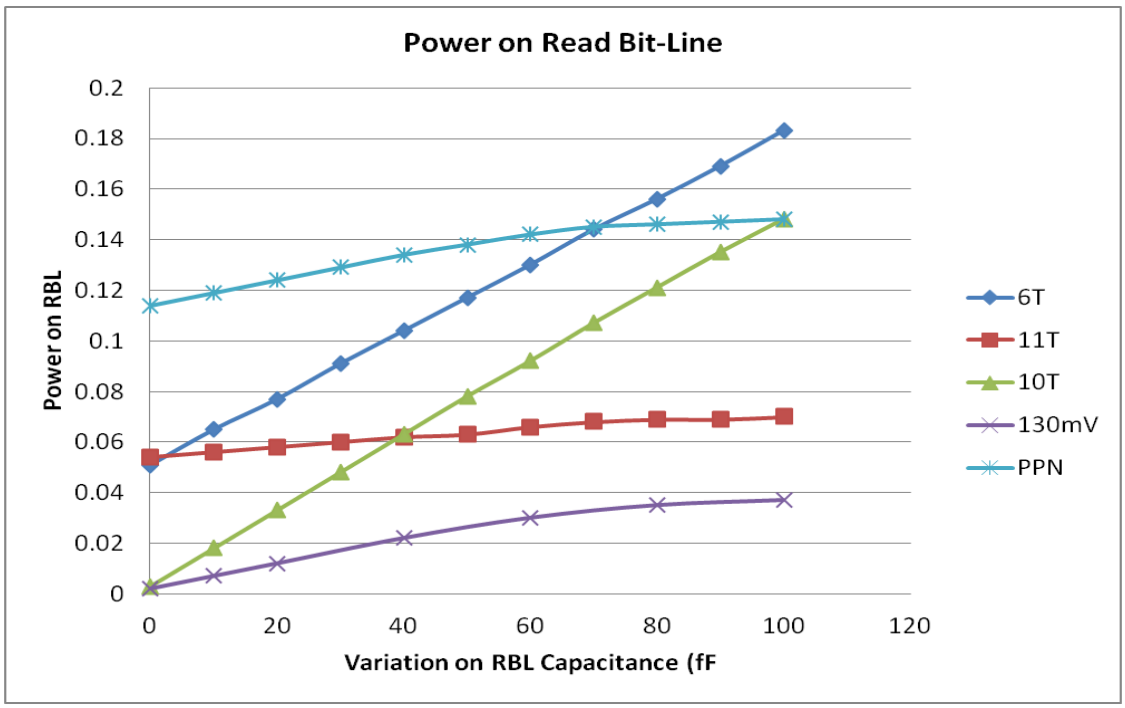

Fig. 3(c): Read power variation with read bit-line capacitance

Table 3: (a): Average read power consumption

SRAM cells	Average read Power Consumption (μW)
6T	2.423
10T subthreshold[17]	2.836
130mV---[20]	2.173
P-P-N- based [19]	0.114mW
Proposed 11-T	2.172

Table 3(b): Average read power consumption at various process technologies

Process Technology (nm)	Average Read Power Consumption (μW)	
	6T SRAM cell	Proposed 11-T SRAM cell
120	28.496	22.399
90	13.532	12.068
65	4.537	2.989

Table 4, gives the current flows through various transistors (W/L=2) in the 6T cell and 11-T cell during read operation. The leakage current through OFF transistors in the proposed cell is lower than the 6T cell which results in the overall power consumption reduction.

Table 4: Current through each transistor during read "0" operation

SRAM cell	Transistors	Current (A)
6T cell	P1	$3.12x10^{-10}$
	N1	$0.043x10^{-3}$
	N3(access transistor)	$0.043x10^{-3}$
	P2	$34.27x10^{-10}$
	N2	$3.12x10^{-10}$
	N4(access transistor)	$3.12x10^{-10}$
11-T cell	M1	$4.27x10^{-10}$
	M2	$3.12x10^{-10}$
	M5(write access transistor)	$4.61x10^{-9}$
	M3	$3.12x10^{-10}$
	M4	$2.73x10^{-9}$
	M6(write access transistor)	$3.12x10^{-10}$
	M7	$3.12x10^{-10}$
	M11	$0.001x10^{-3}$
	M9(read access transistor)	$0.012x10^{-3}$
	M8	$3.54x10^{-10}$
	M10	$0.014x10^{-3}$

Table 5 gives the comparison of the read delay for the proposed cell and other cells for W/L=2. The proposed cell is slower for read 0 due to larger read wordline capacitance and RBL has to swing 2xmore than BL/nBL. Another reason for the larger delay during read 0 operation is due to presence of M10 transistor, the gate of M9 cannot reach to V_{dd} which degrades the driving capability of transistor M9 and results in lower read access time. The read 1 access time is lower than the other cells due to forbidden discharging at the read bitline.

Table 5: Read delay in proposed cell and 6-T cell: a comparison

SRAM cell	Read Delay(pico second)	
	Read 0	Read 1
6T cell	35	35
11-T cell	54	14
10T cell[17]	45	45
D2AP[18]	38	40
P-P-Nbased—[19]	36	36

Figs. 4(a) and 4(b) show the read "0" power consumption at different threshold voltages of PMOS and NMOS transistors. Generally, the power consumption reduces as threshold voltage increases due to lower leakage current. The power consumption for the proposed cell is always lower than the 6T and 10T cells irrespective of the threshold voltage of PMOS and NMOS. Power saving is approximately 65% in the proposed cell as the threshold voltage of PMOS increases from 0.2V to 0.35V against 58% in the 6T cell. The simulated results show slight improvement in the read "0" power saving as the threshold voltage of NMOS increases from 0.25V to 0.35V (Fig. 4(b)). This improvement is 6.11% in the proposed cell compared to 0.24% in the 6T cell.

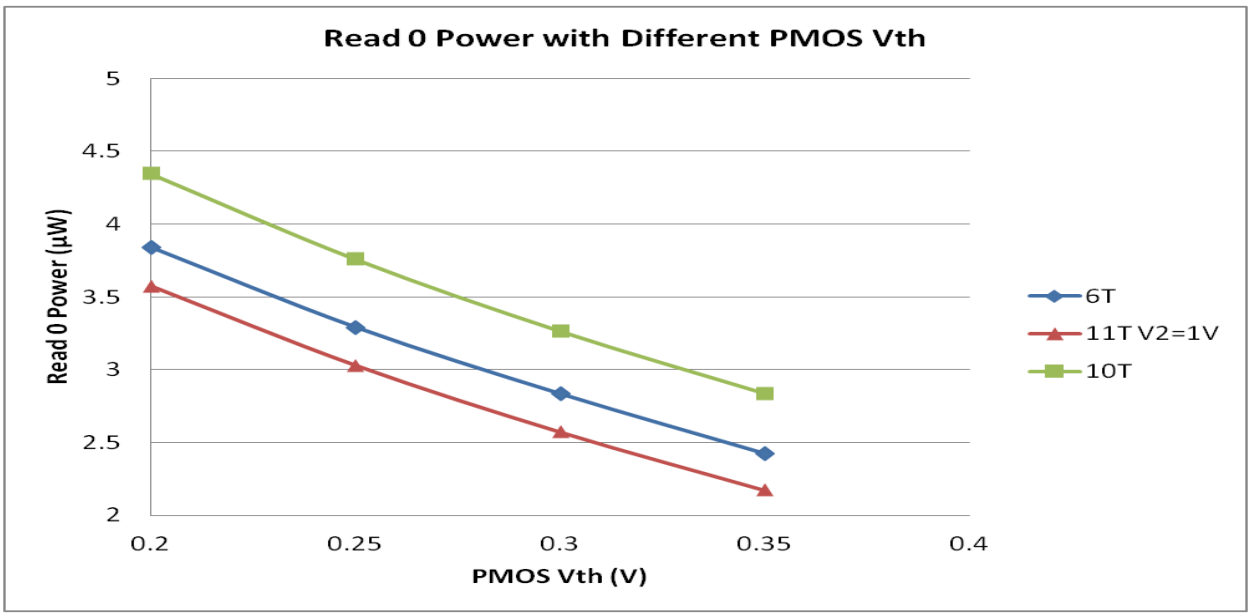

Fig. 4(a): Read"0" power at different threshold voltage of PMOS (V_{Th} for NMOS=0.35V)

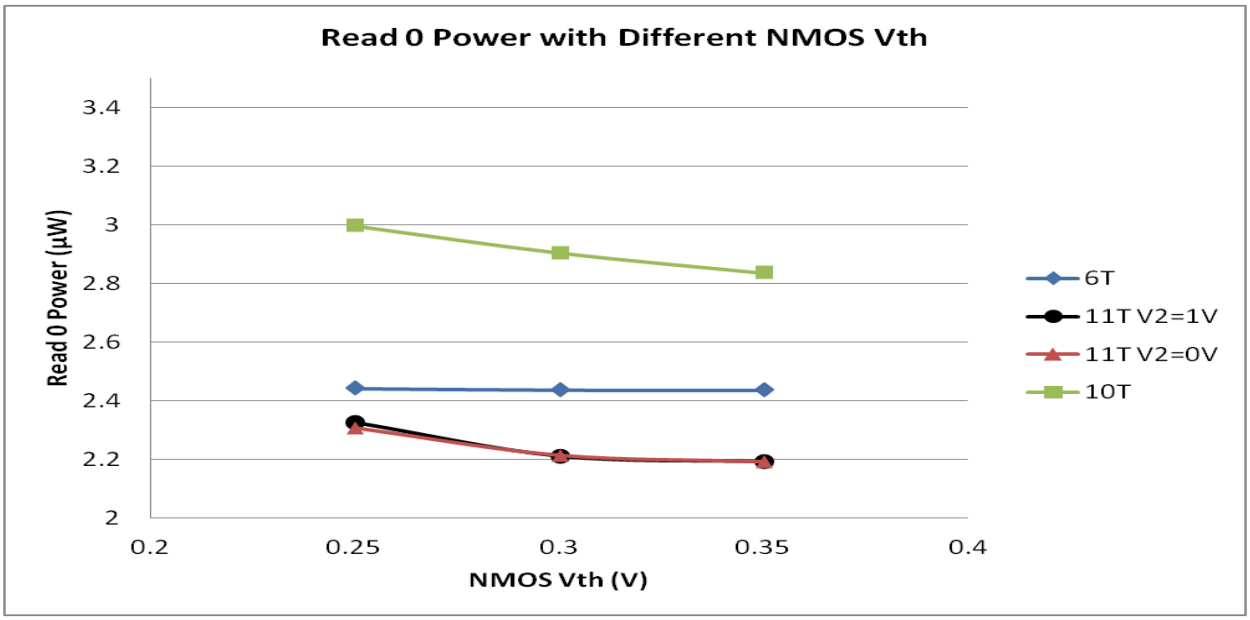

Fig. 4(b): Read "0" power variation ahgainst threshold voltage of NMOS when V_{Th} for PMOS=0.35V

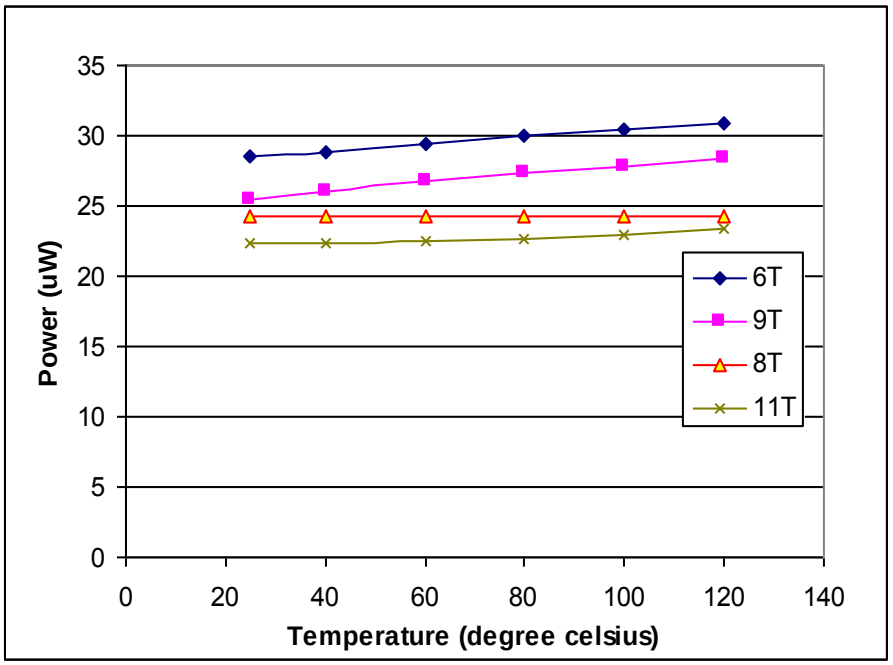

Fig. 5: Read power variation with temperature

Exponentially coupled to temperature, the leakage current poses a serious threat for applications where there is potential for high temperature operation. Generally, power consumption increases with temperature due to increase in various leakage currents. In the proposed cell, the increase in leakage power is not significant even when temperature rises to 120^0C as seen in Fig. 5. The simulation is carried out for 120nm CMOS technology at V_{dd}=1.2V.

3.1. Stability

In this paper, we have used SNM (static-noise margin) as the metric to characterize the read stability. The SNM can be graphically measured on the butterfly curve. The static voltage transfer characteristics of the 6T cell and 11-T cell during read operation are shown in Fig.6 for 120nm CMOS technology and V_{dd}=1.2V. The read SNM is the side length of the maximum nested square between voltage transfer characteristics (VTC) of the two data storage nodes. As seen in Fig. 6, when voltage at one storage node of the conventional 6T cell is 1.2V, other node rises to 300mV instead of 0V because of the voltage divider between the access transistor and pull down transistor. Due to this intrinsic disturbance, produced by direct-read-access mechanism in the 6T cell, data is more prone to external noise. In the proposed 11-T SRAM cell, read circuit is completely isolated from write circuit which enhances the read stability.

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In the proposed cell, when node nQ is 1.2V, node Q is maintained strictly at 0V (Fig.6). The read SNM of the proposed cell (397mV) is approximately 2xhigher than the SNM of the 6T cell (195mV). The robustness of the cell against threshold voltage variation during the read operation defines the dynamic stability of the cell. The use of low V_{Th} access transistor M11 and high V_{Th} transistors M8 and M9 in the proposed cell improves the read SNM to 400mV. This improvement is due to reduction in read voltage. Read stability degraded due to use of high threshold voltage access transistor. These results are given in table 6.

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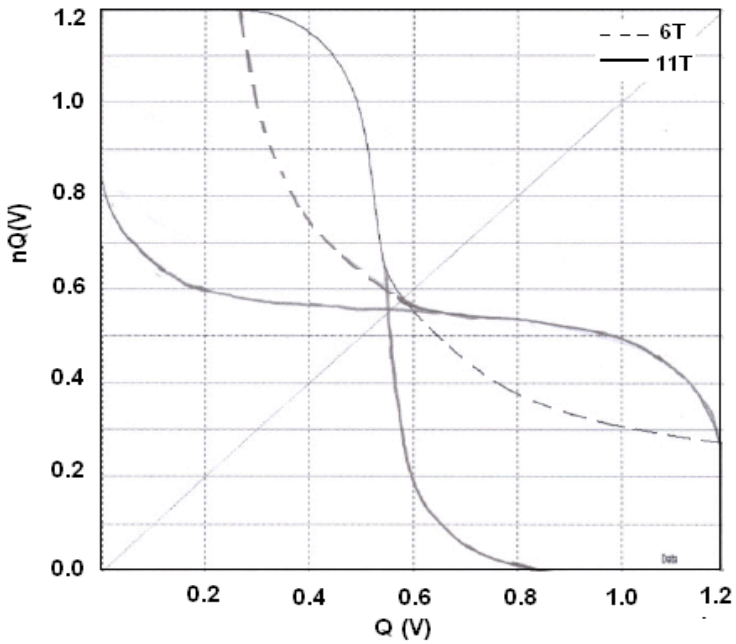

Fig. 6: Read SNM of the proposed 11-T cell and conventional 6T cell.

Due to increased change in current balance between M1/M2 and M3/M4 at high temperature, read SNM is decreased to 331mV from its room temperature. The SNM of the proposed cell improves by 4% when temperature reduces from 27^{o}C to -20^{o}C (see table 7).

As the power supply reduces, SNM of the cell decreases and at a particular voltage, VTC curve of the cell disappears and at this point, any noise can flip the state of SRAM. From Fig.7, it is clear that as V_{dd} drops below 330mV (subthreshold region), SNM curve of the proposed cell disappears which is defined as the Data retention voltage (DRV).

Table 6: Signal-noise margin of the proposed cell for different threshold voltage combination at 120nm CMOS technology

Threshold Voltage	Signal-to-noise Margin (SNM) (mV)
V_{Th}=0.4V for M11, V_{Th}=0.7V for M8, M9	400
V_{Th}=0.4V for M8, M9 and V_{Th}=0.7V for M11	312.5

Table 7: SNM of the proposed and the conventional 6T cell at different temperatures

Temperature (^{0}C)	Signal-to-noise margin (mV)	
	6T	11T
-20	NA	400
27	312.5	195
120	331	NA

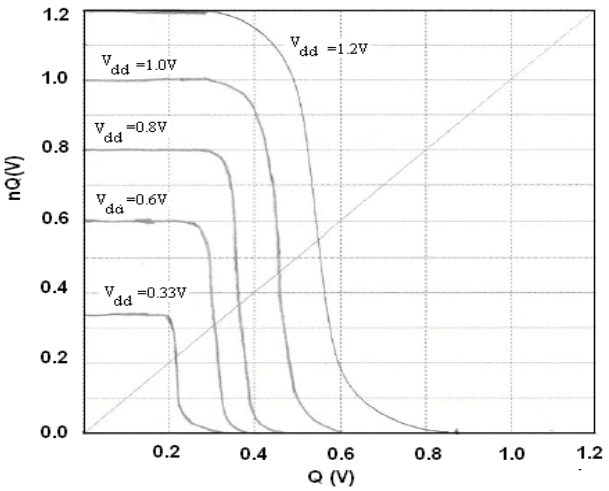

Fig.7: Voltage transfer characteristics of 11-T SRAM cell

3.2. Cell Area

The proposed cell uses 5 more transistors, one extra bit-line and one extra word line (RWL) for read operation compared to the conventional 6T SRAM cell. Due to extra read bitline, wordline, the cost of wire connection in the proposed cell is more than the conventional cell. Compared to the conventional cell, the 11-T cell area is increased from 6.5μm^2 to 9.25μm^2 and hence, the effective area overhead for the proposed cell is 42% for CMOS 120nm technology. Because, the percentage of cell array to cache area is about 70%, the overall cache overhead is roughly (42%x70%) ~29%. This area overhead can be minimized using minimum sized transistors.

3.3. SRAM Array

We have implemented an array of 128-cells using the proposed cell as well as the conventional 6T cell. The layout of these two arrays is shown in Fig. 8. The array includes the decoder and sense amplifier peripheral circuits. The simulated results in terms of power consumption and access delay are given in table 8. From results it is observed that approximately 9% power saving is observed during read operation compared to the 6T cell. This saving can be further improved by proper selection of single ended sense amplifier, decoder and minimum sized transistors. The read delay is degraded by approximately 19% due to use of single ended sense amplifier. Due to larger bitline capacitance and wiring capacitance write power consumption in the proposed cell is increased approximately 6% compared to the 6T cell. The whole simulation is carried out for 90nm CMOS technology at V_{dd}=1V.

Table8: Power consumption and access delay of the SRAM array

6T		11T	
Write	Read	Write	Read
39.685μW	39.643μW	41.947μW	34.734μW
Write	Read	Write	Read
56ps	32ps	65ps	38ps

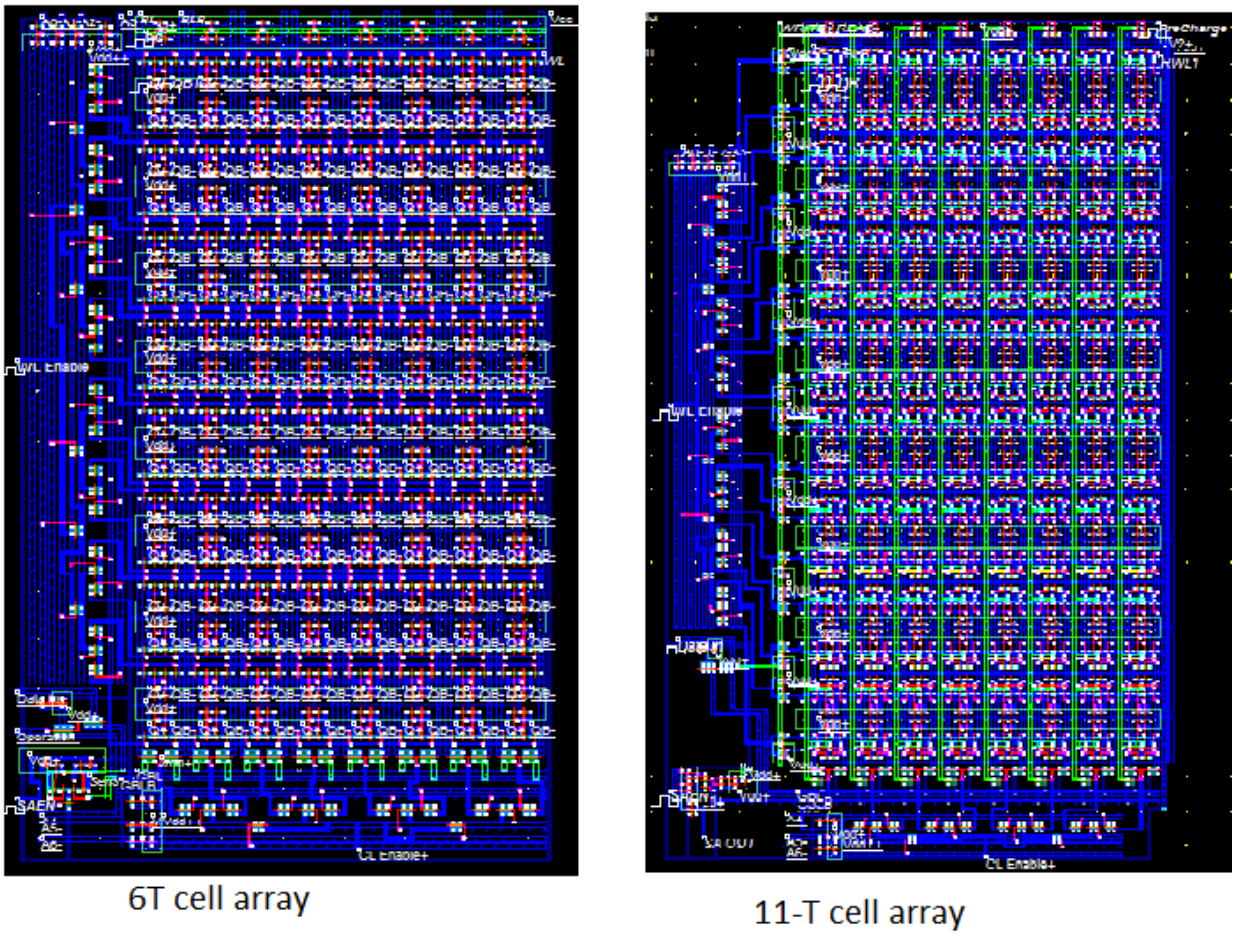

Fig. 8: Layout of the 128-cells array

4. Conclusion

The proposed cell uses separate read and write circuits which improves the read stability of the cell compared to the 6T cell. Due to no discharging activity for read 1 operation, the read bitline power consumption reduces to 12% as compared to the conventional cell. The proposed cell can be used at a supply voltage as low as 330mV and in worse condition ($T=120^0C$) with minimal power consumption. The write operation of the proposed cell is same as the conventional 6T SRAM cell. The main disadvantage of the proposed cell is its area overhead and larger read/write access delay compared to the 6T cell.

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