Low Power Heterogeneous Adder

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Abstract: - Flexibility and Portability has increased the requirement of Low Power components in fields like multimedia, signal processing and other computing applications. Adders are the essential computing elements in such applications. However the present adder architectures with hybrid/heterogeneous features provide performance variations but limits to consume less power. In this paper, low power heterogeneous adder architecture is proposed to enable flexibility to the computing applications and consume less power. 128 bit heterogeneous adder architecture is built using three low power sub-adders (ripple carry, carry look ahead and carry bypass adders). Adder variants in sub-adders block of heterogeneous adder architecture enables to select required quality metrics viz., area, timing and power, for the design. Application requirements like low power – same performance, low power – low area, variable performance can be selected. Designs are demonstrated using Verilog HDL by synthesizing with Cadence's RTL Compiler and mapped to TSMC 65nm technological library node.

Key-Words: - Heterogeneous adder, Power delay trade-off, Low Power VLSI, Digital Filter, Verilog

1. Introduction

Typical issues for VLSI designers are to reduce the area of the chip and increase its performance for computational applications like video compression, graphics, gaming consoles etc. But the development of portable devices and palm held devices, has forced the designers to optimize the power consumption of the device while still meeting the computational requirements. The wireless devices are also making their way to the consumer electronics market where the power consumption is the key design constraint. Hence the power consumption of the device needs to be addressed to increase the run time of the batteries with minimum requirements on size, durability and weight allocated to it [1].

Absence of low power architectures causes the portable devices to suffer from short battery life or require large battery pack. Increase in power consumption in the chips need expensive packaging and cooling devices, and hence it's a clear advantage of cost to go for low power devices. Addition to the cost, high power consumption leads to the issue of reliability, because the high power consumption increases the temperature and it tends to exacerbate several silicon failure mechanisms. Excessive power consumption limits the integration of more transistors on the single chip or on multi-chip modules. This is due to the heat generated from power consumption limits the feasible packaging and performance of the VLSI systems [2].

Motivation of reducing power consumption depends on the applications and how much the designer is willing to sacrifice in cost or performance to obtain the low power consumption devices. The designer might sacrifice the performance for extended battery life of the battery powered devices and suppose if both power and performance are important then the power delay product need to be minimized. Hence in this brief, low power architectures are proposed at comparable performance or negligible performance constraints for the datapath components as they are the repeatedly used blocks in any digital circuits.

Arithmetic components are responsible for the computations and they are the basic building blocks in intensive computational applications. Among the arithmetic components adders are the essential elements and are used repeatedly in any computational intense applications. This enabled many research organizations towards the development of low power computational architectures. In this brief, an effort has been attempted to develop low power heterogeneous adder architecture which consume less power and provide delay optimizations.

2. Related Work

Adder is the essential component in any digital system and many variations are introduced in the carry generation schemes for area, speed and power trade-offs. Hybrid adders were developed in the past to provide area and speed trade-off by utilizing different schemes for sum and carry logic separately. For example in [3 - 4], carry look-ahead adder was used for carry generation and carry select adder for sum generation. Several homogeneous adders were reconfigured with their bit widths to achieve variable performance and power trade-offs. Architectures reported in [5 - 8] have adder variants where larger bit system is partitioned in to smaller bits and reconfigured using additional bits. For example in [5], the author has partitioned the 64 bit Carry select adder to perform as one 64-, two 32-, four 16-, and eight 8-bit adders. Similarly in [8], a carry skip adder has been illustrated. Such adders provide the selection of the bit widths of the adders and improve efficiency of the design. An effort has been put in [9], to add the extra flexibility into the system where different adder variants of smaller bit widths are incorporated in the larger adder system to address the delay optimization under power constraints or power optimization under delay constraints. Such architectures are called as Heterogeneous adders. In this paper, we propose the low power heterogeneous adder architecture to provide power optimization with variable performance.
Limitations of the state of the art reconfigurable architectures,

a) In the regular reconfigurable architectures, static/dedicated adder architectures are utilized and multiplexer selects the required adder variant. This requires more area and consumes more power to achieve variable performance and reconfigurability between the adder variants.

b) In the state of the art heterogeneous architecture, the static sub-adder blocks consumes more power while still providing good performance.

In this paper, we address the above limitations:

- Low power adder architectures
    - Complex cells were utilized to build the adder architecture, as they eliminate the interconnect delays between the gates and helps in reducing power.
    - Elimination of inverters in the critical path reduces the switching power.
    - Complex cells reduce the leakage power of the device.
- The proposed concept is suitable for any bit widths and at any level of abstractions where the application needs different operating corners by providing the flavors of different adder variants in the same design.
- Heterogeneous adder architecture was incorporated in the adder block of digital filter.

The remaining parts of this paper are arranged as follows. Section 3 brief's about the available different adder variants. Proposed adder architecture and advantage is briefed in section 4. Heterogeneous adder architecture and its application are discussed in section 5. Results are discussed in Section 6. Section 7 gives the conclusion and references for the paper are provided in the last.

3. Adder Variants

3.1 CLA (Carry Look Ahead Adder)

CLAs reduce the computation time, by adding two binary numbers faster. They work by creating Carry Propagator 'P' and Carry Generator 'G' signals. Carry propagator propagates to the next level whereas the carry generator generates the output carry regardless of input carry [10]. The Architecture of CLA is shown in Fig. 1.

The corresponding Boolean expressions for 'P' and 'G' are given are used to construct a CLA.

$$Pi = Ai \wedge Bi \quad (1)$$
$$Gi = Ai \cdot Bi \quad (2)$$

The output of sum and carry can be expressed as

$$Sumi = Pi \wedge Ci \quad (3)$$
$$Ci+1 = Gi + (Pi\ Ci);\ \text{where } i = 0, 1\ldots n-1 \quad (4)$$

3.2 RCA (Ripple Carry Adder)

In RCA, Full Adders are cascaded in series, where the carry out from previous stage is connected to carry input of the next stage. Full Adder forms the basic building block of RCA, and it has three inputs say 'A', 'B', 'Cin' and two outputs say "Sum" and "Cout". The critical path of the RCA passes from carry-in to the carry-out along the majority gates. Carry-out expression is given by equation 5.

$$Cout = A\ B + (A + B)\ Cin \quad (5)$$

Equation 5 can be simplified to

$$Cout = A\ B + (A \oplus B)\ Cin = G + P\ Cin \quad (6)$$

Where P and G are the propagate and generate carry logics, Fig. 2 shows the 4 bit ripple carry adder, and from equation (6), the critical path of RCA consists of chain of AND- OR gates[9]. The delay of adder increases linearly with increase in number of bits.

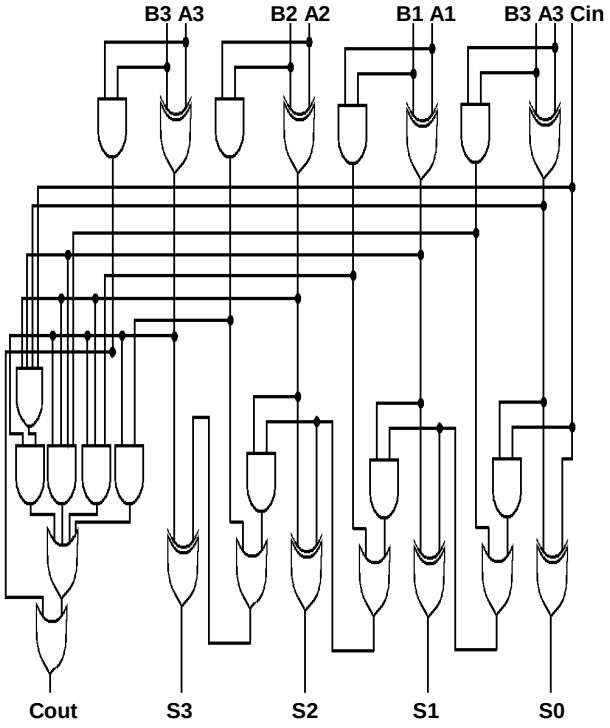

Fig. 1: Architecture of 4 bit Carry Look Ahead Adder

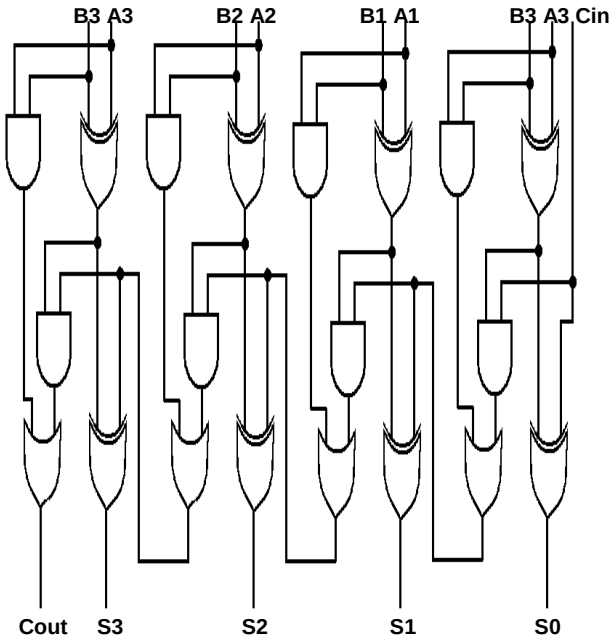

Fig. 2: Architecture of 4 bit Ripple carry adder [10]

3.3 CBA (Carry Bypass Adder)

CBA creates the groups of equal size of N-bits from the words to be added. Carry Propagate 'Pi' signals are used to accelerate the carry propagation within a group of bits, and if all 'Pi' signals of the group are equal to logic '1', then carry in "Cin" bypasses the entire group as shown in Fig. 3. This result in reduced delay compared to RCA. The worst case delay for any N bit CBA; assuming that one stage of the ripple has same delay as one skip, is given by

$$CBA = (b-1) + 0.5 + (N/b-2) + (b-1)$$

$$= 2b + N/b - 3.5 \quad (7)$$

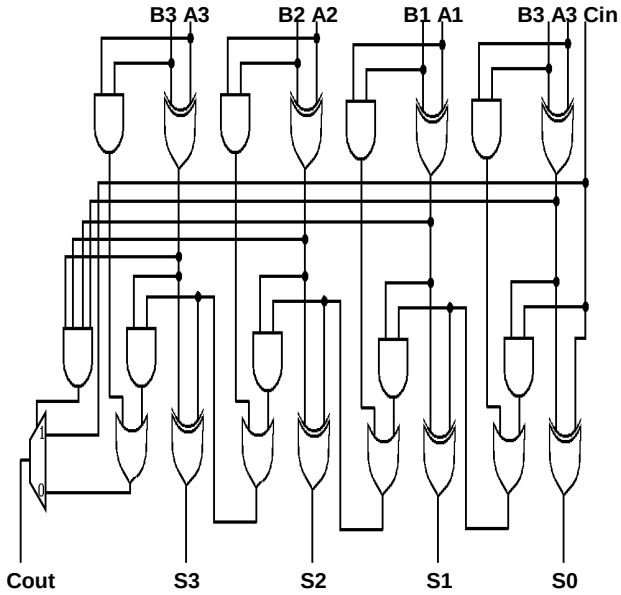

Fig. 3: Architecture of 4 bit Carry Bypass Adder

4. Proposed Adder Architecture & Advantage

The proposed adder architectures are built using complex cells and possible inverters are eliminated in the critical path of the architecture. Complex cells like AND-AND-OR (AO22) and AND-OR (AO22) are used. These complex cells have higher transistor stacks than the regular cells. As per the known fact that the higher transistor stack will have more stack resistance and helps in reducing the leakage power of the devices. It also reduces interconnects and the delay associated between the gates, which inturn reduces any associated glitches. Inverters in the critical path are eliminated by utilizing inverter free equivalent gates. In the regular adder architectures inverters are used in XOR gate implementation.

Advantages:

- Reduced Leakage power due to the higher transistor stacked complex cells
- Reduced dynamic power due to minimal interconnects
- Lesser area due to merging of smaller gates into complex cells

These concepts are incorporated in the adder variants and synthesized using RTL compiler by mapping to TSMC 65nm technological library. The proposed architectures for the adder variants are shown in Fig. 4, Fig. 5 and Fig. 6 respectively for CLA, RCA and CBA architectures. The synthesized results for the 4 bit adder variants are tabulated in Table I.

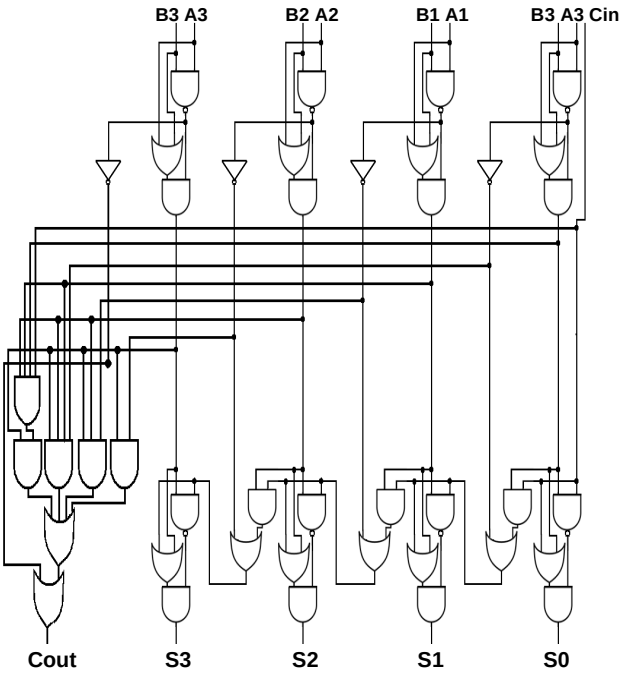

Fig. 4: Proposed architecture of 4 bit Carry Look-ahead Adder

Results from the Table 1 suggest that the proposed 4bit architectures have better efficiency than the conventional architectures. Proposed architectures have gained the area up to 18.42 %, timing by 18% and power by 11%. This proves that the proposed architectures provide the opportunity to extend the design space exploration. So that the power and area optimized results are obtained the same delay (comparing the results of proposed RCA and conventional CBA).

5. Heterogeneous Adder & Filter Application

A heterogeneous adder provides the flavor of different adder variants within the larger adder array. Heterogeneous adder architecture for 12-bit wide with 3 sub-adders of 4bit each is shown in Fig. 7.

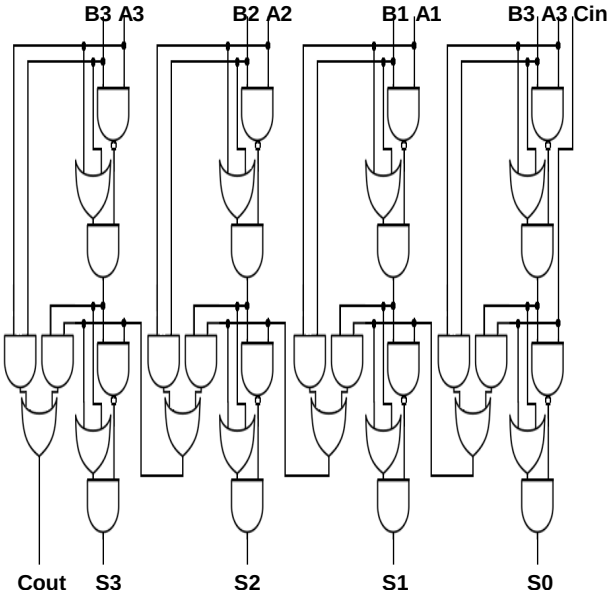

Fig. 5: Proposed architecture of 4 bit Ripple Carry Adder

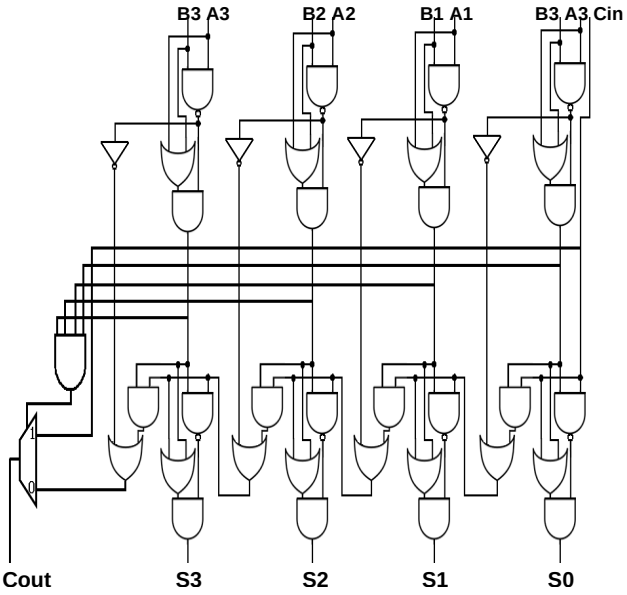

Fig. 6: Proposed architecture of 4 bit Carry Bypass Adder

It gives bigger design space within the given delay constraints. The delay cost of the Heterogeneous adder is smaller than the single type homogeneous adder. The bit positioning of the sub-adders in the heterogeneous adder plays an important role as the carry generation scheme of some adder variants like CLA or CBA can overlap the sum generation scheme. The major advantage of the heterogeneous adder architecture is that the uncovered ranges of the delay can be covered; for example the delay between the (CBA & RCA) and (CBA & CLA) architectures.

Table 1: Results of the conventional and proposed 4-bit adder architectures

Design	Homogeneous Adder								
adder variant	RCA			CLA			CBA		
	Conventional	Proposed	% gain	Conventional	Proposed	% gain	Conventional	Proposed	% gain
Area (Sq. microns)	54.72	44.64	18.42	62.64	61.2	2.30	54	52.56	2.67
Pd (nano seconds)	0.538	0.441	18.03	0.41	0.366	10.73	0.444	0.427	3.83
Dp (micro watt)	2.216	2.023	8.71	2.372	2.356	0.67	2.209	2.2	0.41
Lp (micro watt)	0.569	0.432	24.08	0.631	0.579	8.24	0.585	0.532	9.06

Note: Dp = Dynamic Power; Lp = Leakage Power; Pd = Propagation delay

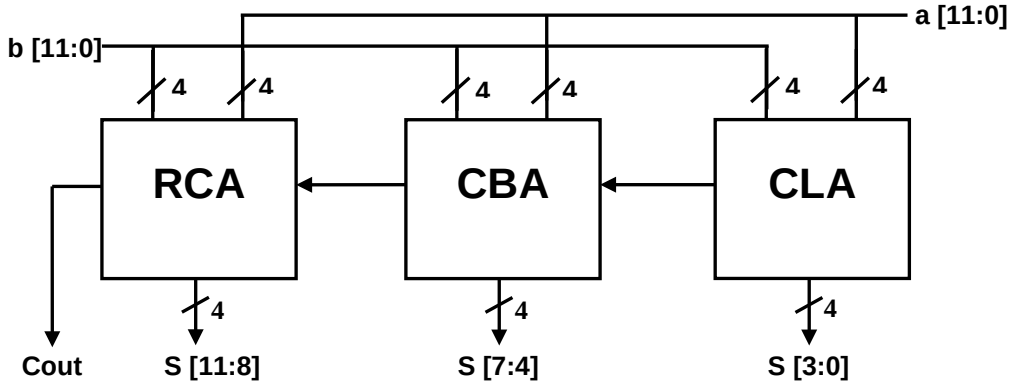

Fig. 7: 12 bit Heterogeneous adder architecture with three 4-bit sub-adders

Proposed adder architectures are incorporated as the sub-adders in the heterogeneous adder architecture. The proposed architecture provides the low power corners and increases its design space further than the conventional heterogeneous adder architecture of [9]. Proposed architecture reduces the power consumption for the given delay constraint while still requiring the lesser area at an instant.

Heterogeneous adder can be utilized in many applications like multipliers, MAC units, Squarer's, filters and etc. As an example in this brief, proposed heterogeneous adder is used in the filter implementation to provide delay optimization with power constraint and power optimization with delay constraint technological corners. A digital filter of QRS detector shown in Fig. 8 was illustrated with heterogeneous adder. Digital filter of 8bit samples with 6 bit co-efficients required the 12 bit wide adder at the final stage of addition. Hence 12 bit wide heterogeneous adder with 3 sub-adders (CLA, RCA, and CBA) was implemented for the Digital filter architecture of Fig. 8.

6. Results & Discussions

The designs were modeled and characterized as per the standard ASIC design methodology. Functionality of the designs was verified with waveform editor of Mentor graphics – Modelsim tool. Designs were synthesized with the help of Cadence RC tool. TSMC 65 nm technological library was considered for benchmarking the results. Table 1 in section 4 gives the results of the 4-bit adder variants for the proposed and the conventional architectures.

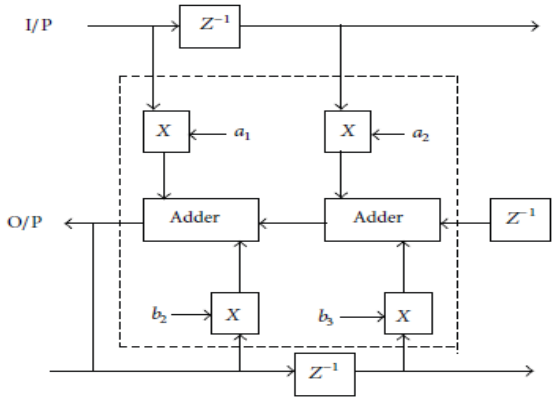

Fig. 8: Digital filter of QRS detector [11]

Table 2 shows the results for the 128 bit single type homogeneous adder architectures. The results of the analysis for the conventional 128 bit heterogeneous adder architecture of [9] and 128 bit proposed heterogeneous adder architectures are tabulated in Table 3.

Table 2: Results of the 128-bit single type homogeneous adder architectures

Design	Homogeneous Adder								
adder variant	RCA			CLA			CBA		
	[9]	Proposed	% gain	[9]	Proposed	% gain	[9]	Proposed	% gain
Area (Sq. microns)	1751.04	1428.48	18.42	2004.48	1958.4	2.30	1728	1681.92	2.67
Pd (nano seconds)	14.81	12.556	15.22	7.516	7.695	-2.38	11.35	11.925	-5.07
Dp (micro watt)	83.422	76.379	8.44	88.57	88.301	0.30	83.966	83.992	-0.03
Lp (micro watt)	18.242	13.911	23.74	20.287	18.693	7.86	18.808	17.213	8.48

Table 3: Results of the 128-bit heterogeneous adder architectures

Design	Heterogeneous Adder											
adder variant	rca8_cla120			rca16_cba112			rca52_cba76			rca88_cba40		
	[9]	Proposed	% gain	[9]	Proposed	% gain	[9]	Proposed	% gain	[9]	Proposed	% gain
Area (Sq. microns)	1988.64	1836	7.68	1730.88	1650.24	4.66	1737.36	1578.96	9.12	1743.84	1507.68	13.54
Pd (nano seconds)	7.928	7.223	8.89	11.68	12.006	-2.76	12.41	12.185	1.88	13.17	12.364	6.15
Dp (micro watt)	88.33	81.416	7.83	83.94	83.051	1.07	83.96	80.826	3.74	83.60	78.792	5.76
Lp (micro watt)	20.16	17.492	13.24	18.74	16.805	10.33	18.56	15.856	14.60	18.42	14.948	18.86

Note: Dp = Dynamic Power; Lp = Leakage Power; Pd = Propagation delay

From Table 2, it can be observed that the performance of the homogeneous adder architectures vary from 7.51 ns to 14.81 ns. And it also suggests that the performance can be improved but at the cost of power, i.e. to gain the performance by 49.25%, 6% of power has to be traded off, and also at the cost of larger area of 12% (comparing the results of conventional RCA and CLA). However from Table 2, performance is improved at larger rate but the trade-off is also too high. For example there is no performance value between 7.516 ns and 11.35 ns and the power consumption is higher by 5.5% with 13.7% higher area. Hence there is need of architectures which trade-offs design's quality metrics at a negligible value or at comparable value.

Proposed architectures results in Table 2, proves that the use of higher transistor stacked complex cells has reduced the Leakage power up to 23.74%. It may also be noted that a significant amount of dynamic power is also reduced (8%). Thus the reduced power consumption enables the design to have low power architectures for the given delay and from the delay perspective it further increases the design space range before going to the heterogeneous adder architectures, i.e., we can achieve the delay of 12.55 ns which is limited with conventional architectures. Moreover further logic optimizations will lead to increase in the range of design space.

From Table 1 and Table 2, it can be observed that the optimizations of proposed architectures holds good and it can be applied to any levels in hierarchically systems. Performance of CLA at 128 bit is degraded by 2% which is due to the higher Fan-out in the cascaded stages resulting in the higher drive strength requirement. But results of other parameters like area and power are appreciably at the same impact as in the 4bit architecture. This proves that the proposed architectures can be utilized as the area and power optimized architectures.

From Table 2 and Table 3, it can be stated that the Table 2 results are limited to fastest (CLA) & slowest (RCA) designs and the other speed range near to CLA with CBA. There is no choice of speed in between the (CBA & RCA) and (CBA & CLA), whereas the results from Table 3 proves that the heterogeneous architecture overcomes the availability of different ranges. But the proposed results of Table 2, suggests that the use of different adder architectures can provide the variations and power optimizations to a certain extent and increase the design space window before going for the heterogeneous architectures.

Similarly from Table 2, the Table 3 shows that the proposed heterogeneous adder architectures results better than the conventional heterogeneous adder architecture of [9]. In heterogeneous adder architectures, various combinations in the sub-adder blocks are analyzed and demonstrated to

have broader design space and select the architectures as per the requirement like low area – low power (slowest design), fastest design with larger area and high power consumption and the ranges between them.

The proposed concept will enable new corners of optimizations like "variable power" for performance optimization, "power optimization with variable performance" and "smallest area" as per the design constraints. It also enables new applications for the existing chip architectures.

6.1 Digital Filter Results

Digital filter with heterogeneous adder architectures was implemented and synthesized with 65 nm technology using Cadence RC. 12-bit wide Single type homogeneous adders and 12-bit wide heterogeneous adder with 3 sub-adders (conventional and proposed CLA, RCA, CBA) architectures were implemented and synthesized results are tabulated in Table 4(a) and Table 4(b).
Table 4 (a), gives the results when digital filter architecture of Fig. 8 implemented with conventional and proposed single type 16-bit homogeneous adders (CLA, RCA and CBA). From Table 4(a) it can be observed that the delay of the filters are static and limits the variations between 2.37 ns to 2.53 ns. Thus the homogeneous adders limit the efficiency of the digital filter architecture.

Table 4 (b), provides the result of the digital filter architecture with conventional and proposed 16-bit heterogeneous adder architectures. The results prove that the proposed adder architectures in the digital filter will impact same as it was at the adder level. Proposed architectures have provided the performance of 2.37ns with proposed RCA8_CBA4 (8bit RCA and 4bit CBA in the final 12 bit adder stage of filter) against the conventional RCA4_CLA8 (4bit RCA and 8bit CLA in the final 12 bit adder stage of filter) with 1.4% lesser area and 1.5% low power consumption. This suggests that the proposed architectures provides area and power optimizations for the same delay. It tells that the proposed architectures results of RCA and CBA can provide the performance of CLA. It can also be observed from the Table 4(b) that the proposed architectures outplay the conventional architectures for any given architecture. From this it can be said that the proposed adder architectures can be incorporated in any system level designs and similar impacts can be observed. The proposed concept of adder architectures can be extended to any bit level and at any abstractions to achieve the low power consumption.

Table 4(a): Results of the Digital filter with 12-bit single type homogeneous adder architectures

Design	FILTER								
adder variant	RCA			CLA			CBA		
	Conventional	Proposed	% gain	Conventional	Proposed	% gain	Conventional	Proposed	% gain
Area (Sq. microns)	2725.56	2691.72	1.24	2749.32	2741.4	0.29	2723.4	2715.84	0.28
Pd (nano seconds)	2.406	2.225	7.52	2.16	2.136	1.11	2.28	2.332	-2.28
Dp (micro watt)	206.326	205.316	0.49	209.241	209.807	-0.27	207.619	208.279	-0.32
Lp (micro watt)	34.517	34.026	1.42	34.704	34.478	0.65	34.564	34.338	0.65

Note: Dp = Dynamic Power; Lp = Leakage Power; Pd = Propagation delay

Table 4(b): Results of the Digital filter with proposed dynamically reconfigurable 12 bit heterogeneous adder architecture

Design	FILTER											
adder variant	RCA4_CLA8			RCA8_CLA4			RCA8_CBA4			RCA4_CBA8		
	Conventional	Proposed	% gain	Conventional	Proposed	% gain	Conventional	Proposed	% gain	Conventional	Proposed	% gain
Area (Sq. microns)	2741.4	2724.84	0.60	2733.48	2708.28	0.92	2724.84	2699.64	0.92	2724.12	2707.56	0.61
Pd (ns)	2.377	2.285	3.87	2.534	2.372	6.39	2.52	2.372	5.87	2.363	2.352	0.47
Dp (micro watt)	208.879	208.95	-0.04	207.739	206.92	0.39	207.3	206.51	0.38	207.633	207.78	-0.07
Lp (micro watt)	34.64	34.324	0.91	34.576	34.174	1.16	34.528	34.126	1.16	34.546	34.23	0.91

Note: Dp = Dynamic Power; Lp = Leakage Power; Pd = Propagation delay

7. Conclusion

A coarse grained heterogeneous architecture with different proposed adder architectures is implemented in this paper. The proposed heterogeneous adder architecture extends the design space further and provides power optimization corners. The selection of adder variants and its number of different adder variants in the sub-adder block can be selected or limited as per the application requirement for higher resolution in efficiency. Proposed architecture enables efficient design space exploration. The proposed heterogeneous architecture can be utilized where the application needs low leakage power, low area, and a balanced design quality metrics. Digital filter with proposed Heterogeneous adder architecture was implemented and efficient results were achieved with larger variations. These adder architectures are pervasive and can be implemented at various levels of hierarchical abstractions.

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