Design of class-D audio power amplifiers in 130 nm SOI-BCD technology for automotive applications

Karim EL KHADIRI and Hassan QJIDAA
Sidi Mouhamed Ben Abbellah University
Faculty of Science Dhar El Mahrez
Laboratoire d'Electronique Signaux – Systèmes et Informatique (LESSI)
Fez, Morocco
karim.elkhadiri@usmba.ac.ma, hassan.qjidaa@usmba.ac.ma

Abstract: - In this work, design of class D audio power amplifier output stage implemented in 130 nm Silicon-on-Insulator (SOI) technology is proposed for high power efficiency and low distortion. The class-D audio amplifier consists of two DMOS power transistors in a totem-pole configuration, a gate driver, a shunt regulator, a ramp generator, a comparator and an integrator. The design method proposed in this study uses two on-chip shunt regulators to provide stable on-chip supply voltages to the gate driver circuits and a second-order feedback loop to suppress supply ripple. Its performance was found to be better than previously published output stages implemented in SOI based BCD processes, which are typically more complex and costly. The proposed class-D audio amplifier was designed, simulated and layed out in Cadence using TSMC 130 nm SOI-BCD technology. The class-D audio amplifier achieves a total root-mean-square (RMS) output power of 0.5W, a total harmonic distortion plus noise (THD+N) at the 8-Ω load less than 0.06%, and a power efficiency of 93%. The final design occupies approximately 1.5mm^2.

Key-Words: - Class-D Amplifier, Output stage, SOI technology, Triangle-wave generator, Pulse-width-modulation.

1 Introduction

In recent years the interest in class-D amplifiers has shown a steady increase for automotive audio applications. The higher efficiency offered by class-D power amplifiers compared to class-AB makes them ideal for driving such loads. Their superior power efficiency means they need a smaller heat sink, which in turn means more space available for electronics in the tight space of a head unit. In addition class-D can be integrated into 60-V power distribution [1, 2].

The output voltage of a Class-D is influenced by the supply voltage, and the supply voltage in a car is not constant. Measures have to be taken for supply ripple voltage rejection. The best way to accomplish this is to use a negative feedback loop. Using a second-order feedback loop provides superior ripple rejection [3].

Electromagnetic interference (EMI) caused by switching is one of the most important Class-D problems and a very difficult one to solve. At the design level, EMI can be mitigated by phase staggering, frequency hopping, and AD/BD modulation [4, 5].

Current spikes that contribute to EMI are created as a result of the dead time between the transistors in the amplifier switching. During the dead time, a charge builds up in the body diode and this charge is released as a current spike as shown in figure 1 where the red line indicates the spike [6]. The obvious solution is to eliminate dead time. To accomplish this, Silicon-on-Insulator (SOI) technology is ideal because all components are isolated by oxide. When an output falls below ground no charge is built up in the substrate of the device, which reduces the reverse recovery time and there is no cross talk to other channels.

The supply bouncing problem of integrated high-voltage high-power class-D output stages for audio are discussed in [1, 2]. The output current switching between the high-side (HS) and low-side (LS) power switches causes large di/dt and in turn on-chip supply bouncing caused by parasitic inductances. The problem is accomplished by gate drivers featuring an on-chip regulated floating supply voltage [1, 2], but the distortion problem caused by large deadtime (100ns) has received much attention.

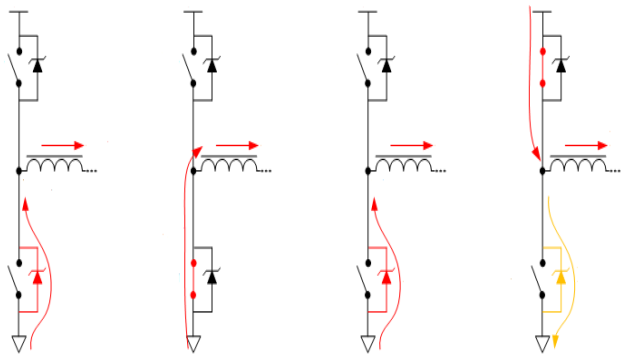

Fig.1 Dead-time induced current spikes cause EMI

In this paper we present a class D audio power amplifier output stage in 130nm SOI process without supply bouncing issue and high dynamic performance. A gate driver featuring an on-chip shunt regulator overcomes the supply bouncing, a second-order feedback loop provides superior ripple rejection, and to accomplish the distortion problem caused by deadtime we use silicon-on-insulator technology.

2 Design in SOI Based BCD

For many high voltage IC applications like in power conversion, automotive, consumer and medical, silicon on insulator (SOI) technology provides clear advantages over commonly used junction isolation technology [7, 8]. The buried oxide (BOX) enables a full dielectric isolation between handler wafer/substrate and device layer. Integrated circuit design starts with the selection of an appropriate technology. For class-D audio amplifiers a BCD process is an almost inevitable choice. The advantage of BCD technology on SOI is in the ability to have all devices fully dielectrically isolated. This technology enables latch up free solutions and SOI offers lower parasitic leakage currents at high temperature. SOI is very easy to design in. Class-D audio amplifiers use this feature together with the relatively small reverse recovery current to increase performance over bulk solutions. The bipolar transistors are indispensable for analogue circuits where noise and offset are important. The CMOS allows for integration of modest size logic circuits for interfacing and control functions. Finally, DMOS transistors are almost perfect power switches featuring high breakdown voltage and low on-resistance plus the ability to conduct current in both directions. The SOI based A-BCD processes are exceptionally suitable for switching applications. The dielectric isolation between the integrated components makes designs in A-BCD inherently free from latch-up phenomena. Consequently, the back-gate diodes of the DMOS power transistors in the switching power stage can be exploited as fly-back diodes without the need for external Schottky diodes. In conventional bulk technologies external diodes are often necessary to prevent injection of minority carriers into the substrate that can lead to latch-up. A particularly advantageous feature of A-BCD is the remarkably small reverse recovery charge associated with the back-gate diodes of the DMOS transistors. The reverse recovery charge is almost an order of magnitude smaller than that of comparable DMOS transistors in bulk technology. The small reverse recovery charge makes A-BCD especially suited for switching applications since reverse recovery is one of the major sources of EMI.

3 Architecture and Circuit Descriptions

A basic class-D power stage consists of two DMOS power transistors in a totem-pole configuration as shown in as shown in figure 2. The class-D consists of a pulse width modulated (PWM) modulator, a triangle wave generator, an output power stage, a second-order low-pass filter, a feedback network and a compensator. Each class-D audio has a controller in which the audio input signal is converted to a PWM signal. The controller drives a switching power stage that boosts the PWM signal to high power levels. The PWM output signal is feedback to the controller. The feedback loop is completely integrated on-chip. External demodulation filters are used to filter the audio content of the PWM signal and suppress the energy at higher frequencies. Usually, a second-order LC low-pass filter is sufficient. Both controllers have a differential input stage that makes single-ended as well as bridge-tied-load (BTL) operation possible.

3.1 Subsection Negative feedback control of class-D amplifier

Figure 3 shows the block diagram of negative feedback of the class-D amplifier. The Gfb is the forward gain of the closed-loop class-D amplifier and K is the feedback factor [14].
The output voltage can then be expressed as:

$$\mathrm{Vout} = \mathrm{Vin} \times \mathrm{Gff} + \frac{\mathrm{Vn}}{1 + \mathrm{Gfb} \times \mathrm{K}} \qquad (1)$$

The Gff is the forward open-loop gain of the class-D amplifier and Vn is the harmonic distortion component. We can assume the K and Gfb are constant for calculating the THD, since both β and

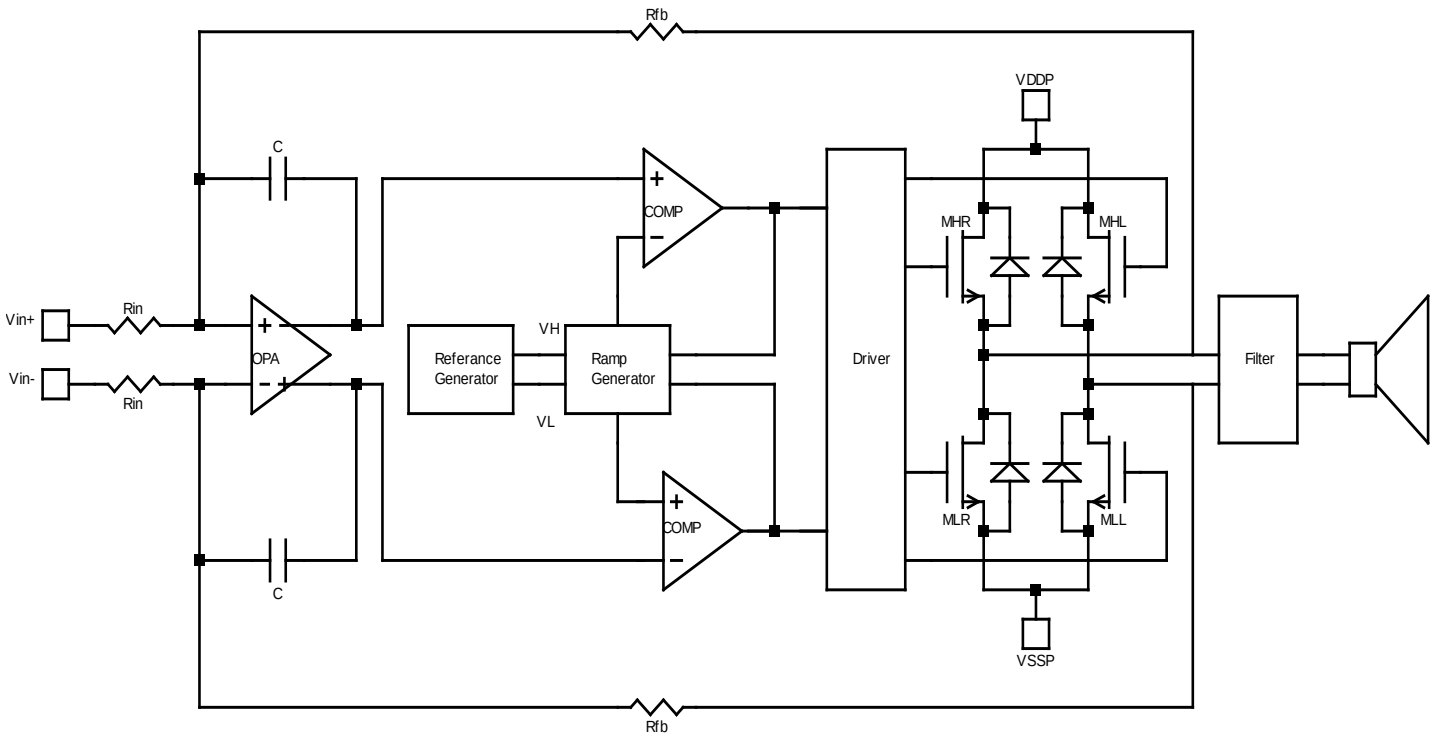

Fig.2 The block diagram of the proposed class-D amplifier

The THD of the closed-loop can then be expressed as:

$$THD = \frac{\sqrt{\sum_{n=2}^{\infty}(Vn)^2}}{Gff \times Vin(1 + Gfb \times K)} \qquad (2)$$

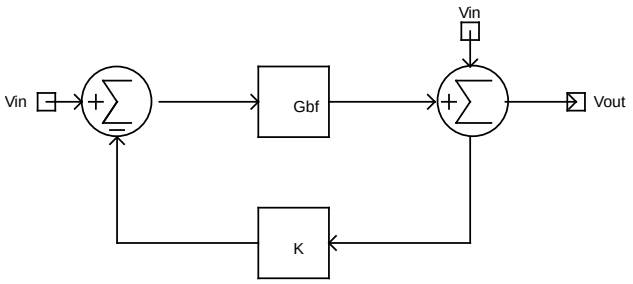

Fig.3 Block diagram of negative feedback of the class-D amplifier

This class-D amplifier employs a negative feedback technique to improve the THD problem [9].

The class-D amplifier circuit diagram is shown in Fig. 2. The loop filter has been designed as active-RC one-pole system. If Vin=0, the class-D amplifier closed-loop transfer function can be expressed as:

$$H(s) = -\frac{\frac{G_{pwm}}{R_1 C_{F1}}}{s + \frac{G_{pwm}}{R_1 C_{F1}}}$$

$$H(s) = -\frac{R_{F1}}{R_1}.\frac{G_{pwm}}{sR_{F1}.C_{F1} + G_{pwm}} \qquad (3)$$

With $G_{pwm} = \frac{V_p}{V_{pwm}}$ (4)

Where G_{PWM} is the gain of PWM modulator, VP is the power supply voltage of amplifier, and V_{PWM} is the triangular-wave peak–peak voltage.

The gain of the feedback amplifier can be obtained through (3).

$$H(s) = \frac{A(s)}{1 + A(s).K} = -\frac{\frac{G_{pwm}}{sR_1 C_{F1}}}{1 + \frac{G_{pwm}}{sR_1 C_{F1}}} \qquad (5)$$

With $A = -\frac{G_{pwm}}{sR_1 C_{F1}}$, $K = -\frac{R_1}{R_{F1}}$ (6)

Where A and K represent the open-loop gain and feedback factor. The THD can be reduce (1+A K) by negative feedback.

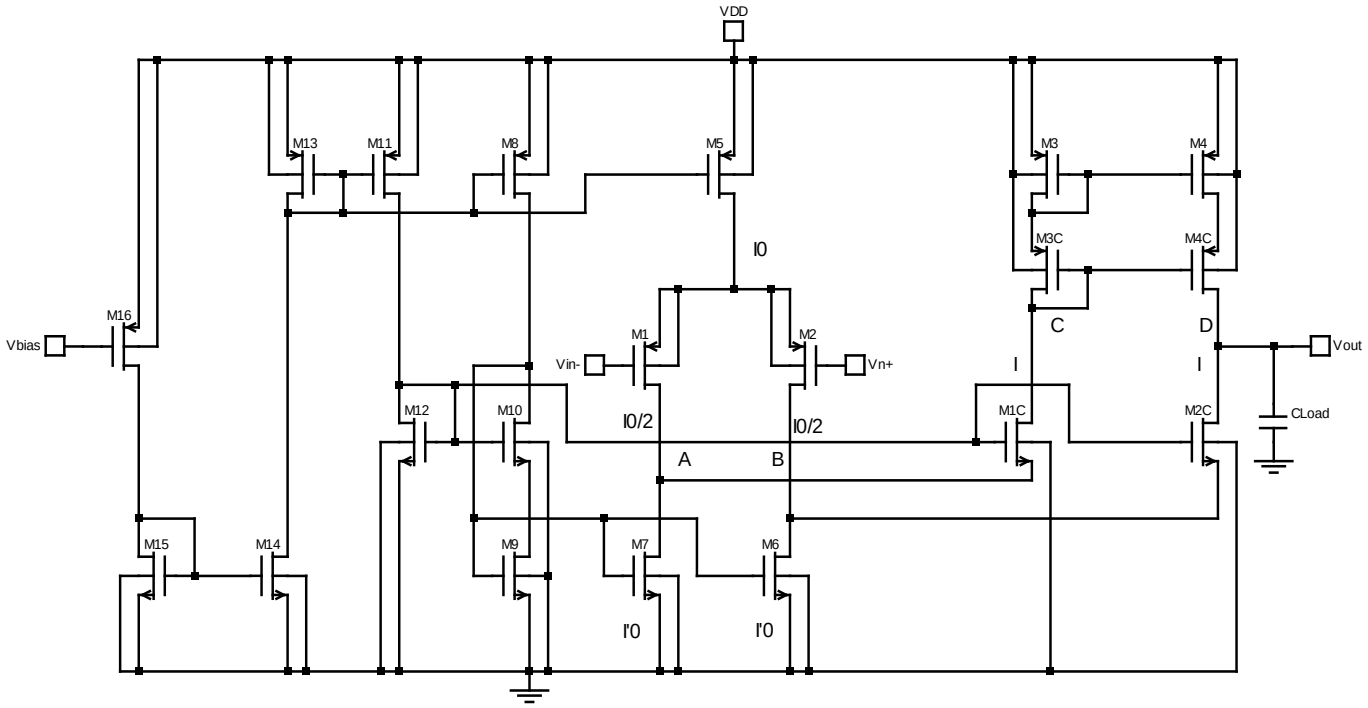

Fig.4 The folded-cascode operational amplifier

3.2 Folded-cascode operational amplifier

The circuit diagram of a folded-cascode operational amplifier circuit is shown in figure.4. The basic operation of the circuit is as follows [15]. The dc current I_0 of the current source M7 is shared equally by M1 and M2. Also, the matched sources M5 and M6 draw equal bias currents I'_0 form nodes A and B. Hence M_{1C} and M_{2C} also carry equal bias currents I'_0 $-I_0/2$. A difference input voltage $\Delta v_{in}^{+} = \Delta v_i /2$ and $\Delta v_{in}^{-} = -\Delta v_{in}/2$ applied to the gate of M1 and M2 will offset their drain currents by $\pm\Delta I_0 = \pm g_{mi}\Delta v_{in}/2$. Since the currents I_0' of M5 and M6 remain unchanged, the currents of M_{1C} and M_{2C} will also be change by $\pm\Delta I_0$. The currents mirror M3, M4, M_{3C} and M_{4C} transfers the current change in M3 and M_{3C} to M4 and M_{4C}. Hence the output voltage increment in $g_{mi}\ R_0\Delta v_{in}$, where R_0 is the output impedance at node D. It can be shown that

$$R_0 \approx (r_{d4}r_{d4c}g_{m4c})\ |||[(r_{d2}||r_{d6})r_{d2c}g_{m2c}] \quad (7)$$

The increment gain is than

$$A_{dm} = -g_{mi}\ R_0$$

$$A_{dm} = -(r_{d4}r_{d4c}g_{m4c})\ |||[(r_{d2}||r_{d6})r_{d2c}g_{m2c}]g_{mi}$$

We carried out PSPICE simulation for the circuit illustrated in figure. 4 and obtained the curves shown in figure.5. The voltage gain is about 72 dB is gained for the voltage of the operation amplifier with a bandwidth of about 102 KHz. The phase response is shown as the red curve in the middle has a phase angle of 65°.

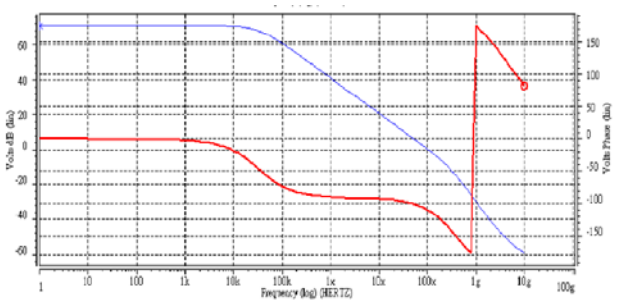

Fig. 5. Simulation results for the proposed folded-cascode operational amplifier

3.3 Triangular-wave generator circuit

The triangle-wave generator is shown in figure. 6. The triangular-wave generator contains current generator, tow switch and two transmission gate (TG). V_H and V_L are obtained from the bandgap reference to supply stable voltage, so it is independent of PVT variations. The transmission gate control method is to build constant frequency architecture to provide better linearity.

When clock signal V_{CLK} can be considered as logical low, the transistor MP1 and MN1 are on and MP2 and MN1 are off, the current Ichg will charge the capacitor Ctri. Similarly, when the clock signal V_{CLK} can be considered as logical high, the transistor MP1 and MN1 are off and MP2 and MN1 are on, the Idchg will discharge the capacitor Ctri.
We obtained a triangle carrier signal with the resulting period given by

$$T_{TRI} = C_{TRI} \cdot (V_H - V_L) \cdot \left(\frac{1}{I_{Chg}} - \frac{1}{I_{DChg}} \right) \quad (8)$$

Simulation result for voltage ramp generator output voltage waveform is shown in figure 7. Ramp wave at the desired frequency can be achieved by adjusting the frequency of CLK or the value of capacitance.

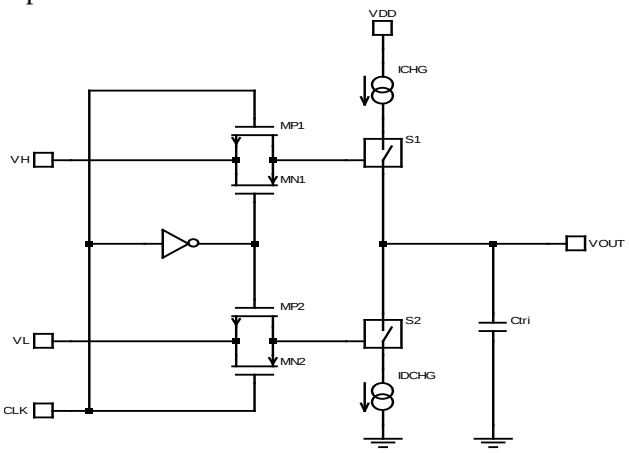

Fig.6 Triangle generator

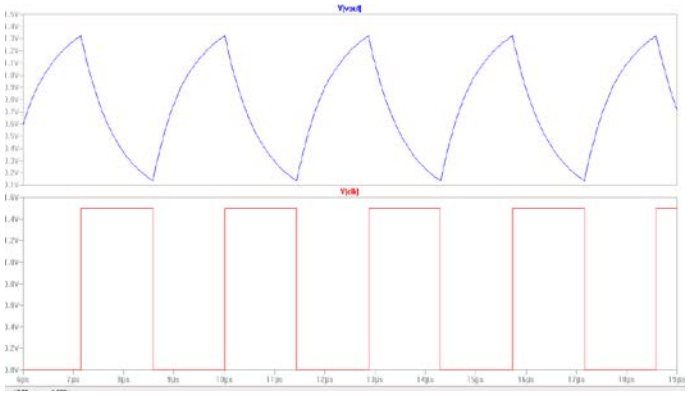

Fig.7 Triangular-wave generator circuit

3.4 Comparator circuit

The comparator used in the design is shown in figure 8. This comparator is implemented by a source-coupled differential pair with positive feedback to provide a high gain [10].The gain of the positive feedback gain stage is given by

$$A_V = \sqrt{\frac{\mu_p \left(\frac{w}{l}\right)_1}{\mu_p \left(\frac{w}{l}\right)_3}} \times \frac{1}{1-\alpha} \quad (9)$$

Where $\alpha = (W/L)_5/(W/L)_3$ is the positive feedback factor.

The transistors of M_7, M_8, M_9, and M_{10} constitute the second stage. This stage mainly contributes some gain in whole circuit. The gain of the second stage is as following

$$A_{V2} = g_{m10} \times (r_{ds7} \,//\, r_{ds10}) \quad (10)$$

The third stage constituted by the inverter chain M_{12}, M_{13}, M_{14}, and M_{15}, are used to increase the response of output signal. With the usage of this stage, the size of M_9 and M_{10} can be reduced to achieve same performance and due to the reduction of M_9 and M_{10}, the effect of the parasitic capacitance at gates of M_7 and M_8 is decreased which results in a faster response. The resulting simulation results for the waveforms of comparator are shown in figure.9.

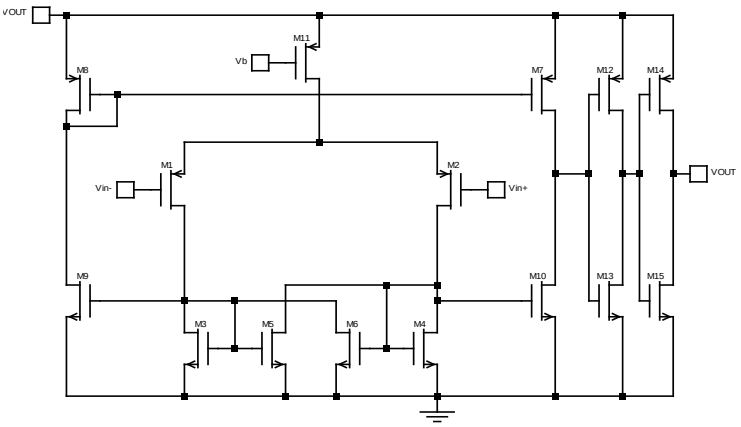

Fig .8 Schematic of the comparator

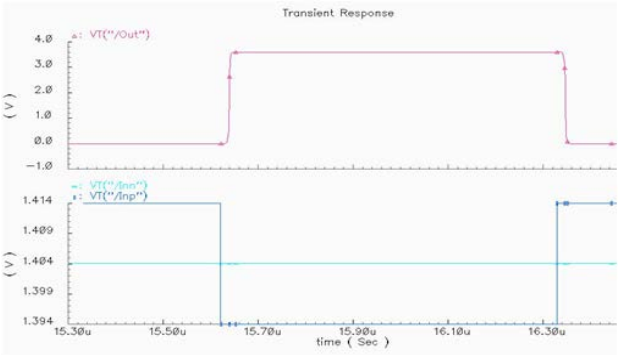

Fig. 9 Simulation results for the comparator

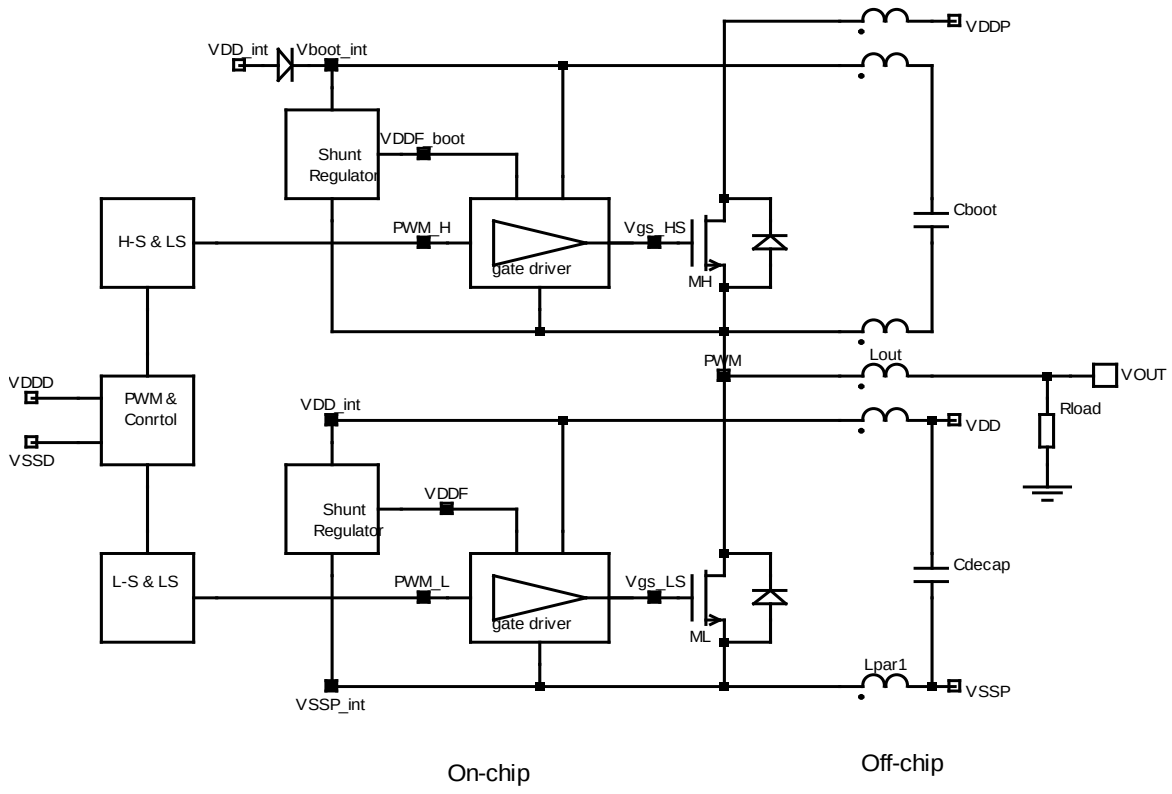

Fig.10 Proposed power stage topology

4 Power Stage Design

The performance of any class-D amplifier is limited by the quality of the switching power stage. In IC technology the output power transistors are typically implemented using two identical DMOS transistors in a totem-pole arrangement. They are preferred because of their R_{ON} x Area product and low R_{DS} value, but require additional components and complexity in order to drive the high-side NMOS transistor transitions as shown in figure 10. Since a voltage level higher than the power supply is necessary in order to turn M_H on (Vgs = Vg-Vout > Vth), an additional bootstrap capacitor, C_{Boot}, serves as a floating power supply for the high side gate driver. This technique is known as bootstrapping technique [11]. The bootstrap capacitor is recharged when the output V_{OUT} switches to the LS through an integrated diode D_{BOOT} connected to V_{SHUNT}. The switch control block translates the input signal PWM into appropriate signals for the HS and LS gate drivers.

To accomplish the supply bouncing issue and distortion problem caused by deadtime and supply-voltage modulation, we proposed a new power stage topology figure 10 supply bouncing influence on the functionality of the gate driver is eliminated by the on-chip shunt regulator gate-driver supply and the distortion caused by deadtime as well as supply voltage modulation are effectively suppressed by the feedback loop of the amplifier. Distortion is in a way related to electromagnetic compatibility (EMC) performance. Good distortion figures are hardly possible when the EMC performance is poor.

4.1 Gate driver

For superior output power and efficiency, the output power transistors devices must be large. Since these devices are very large, with widths in millimeters, there are large parasitic capacitances that must be driven. The task of driving these large capacitances is not trivial. The output of the comparator is not able to drive these capacitances; therefore it is necessary to devise a scheme that will effectively increase the input signal to the output transistors.

To overcome the on-chip driver supply bouncing issue without sacrificing on the efficiency during switching transitions, a gate driver topology with on-chip shunt regulator floating supply is proposed in this paper. The detailed gate driver circuit is shown in figure.11, the circuit used to invert the

signal and bring the output rail from 3.3V to 12V. This circuit is a bootstrap inverter. When Vin is high, transistor M_1 is on. M_2 is on, but weakly, resulting in Vgs,LS being pulled low. If Vin drops to a low voltage, M_1 turns off and all the current going across M_2 now charges C_0 and Vout increases slowly. M_2 remains on until Vgs, LS reaches VDDF, and M_2 turns off. To get a large boost on V_x to drive the gate to 12V, C_1 must be much larger than C_2 because Vx experiences a gain of C_1/C_1+C_2.

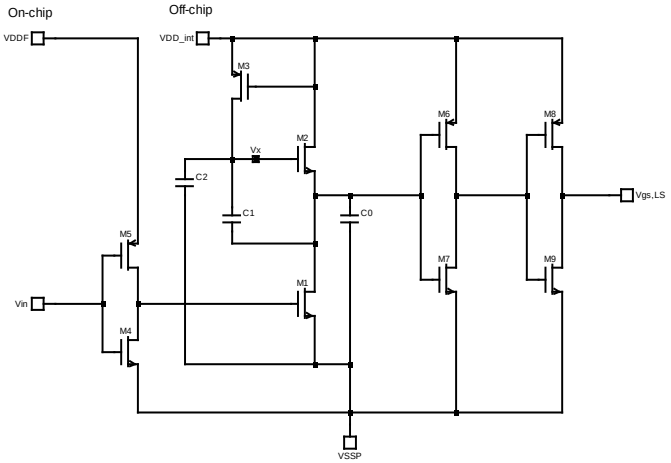

Fig.11 Detailed gate driver structure

4.2 On-chip shunt regulator

Figure 12 illustrates the block diagram which is the circuit structure of the on chip shunt regulator for both HS and LS, the shunt regulator is supplied energy by current supply [12]. The power supply of the controlled circuit, which are Gm-and Rm-stages, is written below as

$$VDDC \cong IDD \times Req \qquad (11)$$

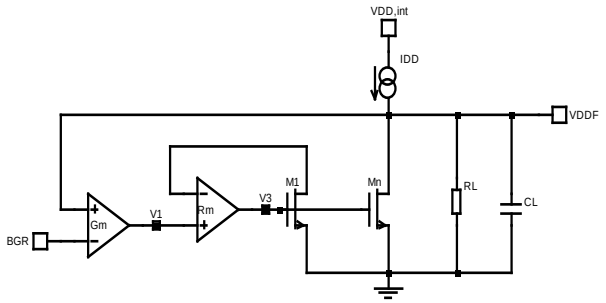

Fig.12 Block diagram of on-chip shunt regulator

The R_{eq} equals the parallel resistance of R_L and r_{on}. The proposed shunt regulator includes an operational trans-conductor amplifier Gm-stage, an operational trans-impedance amplifier Rm-stage, a current-sense circuit M10 and a pass element Mn.

The transform function of the shunt regulator is shown below (Equation 12).

$$\frac{V_{out}}{V_{in}}(s) = \frac{A_1\left(2+\frac{s}{\omega_{p1}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \frac{A_2\left(2+\frac{s}{\omega_{p3}}\right)}{\left(1+\frac{s}{\omega_{p3}}\right)\left(1+\frac{s}{\omega_{p4}}\right)} \frac{A_3}{\left(1+\frac{s}{\omega_{p5}}\right)} \qquad (12)$$

The open loop gain of the shunt regulator AOL equals to A_1 times A_2 times A_3.

The output devices of the shunt regulator are also DMOS devices to sustain the higher 12V VDD as well as the bouncing superimposed on it.

5 Simulation Results

The circuit design of a class D audio power amplifier output stage implemented in 130 nm Silicon-on-Insulator (SOI) technology is simulated using Cadence Spectre simulator in a 130nm single-poly, four-metal, SOI process for automotive applications.

The key parameters that needed to meet specification were the output power and efficiency. The amplifier must be capable of delivering 500mW output power and be at least 93% efficient at 300mW of delivered power. A simple test circuit consisting of a resistor and inductor in series to simulate the speaker load was used measure the efficiency and output power.

5.1 Power

To measure the output power, a sinusoidal input was applied to the folded-cascode operational amplifier. Because the output signals are time varying, output power is measured by multiplying the RMS voltage across the load by the RMS current through the load, as shown in Equation 13.

$$P_{LOAD} = I_{RMSLOAD} V_{RMSLOAD} \qquad (13)$$
$$= \left[\sqrt{\frac{1}{T}\int_0^T I(t)^2 dt}\right]\left[\sqrt{\frac{1}{T}\int_0^T (V_H(t) - V_L(t))^2 dt}\right]$$

As expected, increasing the amplitude of the input audio signal increased the power to the load, as this increases the effective current through the load, which is approximately $(A_{AUDIO}/A_{SAW})*I_{MAX}$.

The maximum output power capabilities of the amplifier far exceed the 500mW benchmark. With an input amplitude 93% that of the triangle wave, the output power is 570mW. This number can be further increased if we are more aggressive with the input amplitude. Running at 90% input/triangle ratio, all switches are still registered and we deliver 680mW output power.

5.2 Efficiency

The efficiency of the output power transistors is related to how much current is delivered to the load over time. Anytime current is not delivered to the load, power is still dissipated by the R_{ON} of the output stage which further reduces efficiency. The formula for optimizing the power efficiency is given in (14).

$$\rho = \frac{P_{out}}{P_{out} + P_s + P_c + P_r} \qquad (14)$$

where Pout, Ps, Pc, Pr, are the output power at the load, the power dissipation due to short-circuit current during transitions, the power due to the parasitic capacitances of power transistors and the power due to the transistor on-resistance [13].

In our design we needed to maintain 93% efficiency at 500mW delivered power. Figure 13 shows the variation of efficiency vs. output power.

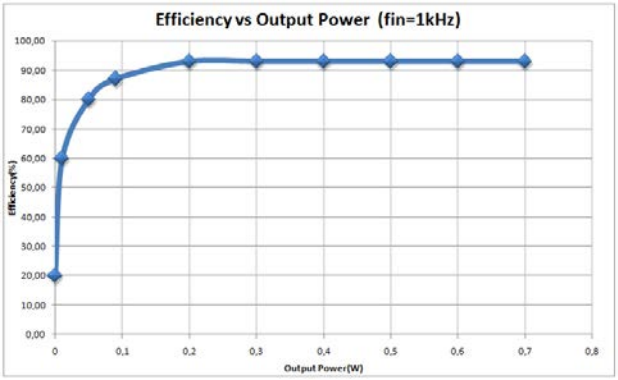

Fig.13 Plot of Efficiency vs. Output Power.

5.3 Total harmonic distortion (THD)

Another important issue for amplifiers in general is the total harmonic distortion (THD) analysis. Here the input is single tone and one measures the power contained in the output signal located at the input frequency and its harmonics. The THD itself is given by Eq.(15).

$$\%THD = \frac{\sqrt{(H_2^2 + H_3^2 + H_4^2 + \cdots)}}{\sqrt{(H_1^2 + H_2^2 + H_3^2 + H_4^2 \ldots)}} \times 100 \qquad (15)$$

Where the H2 ...Hi denote the power levels at the harmonics and H1 is the power level at the fundamental frequency. Figure 14 shows the THD+N values for different values of the output power.

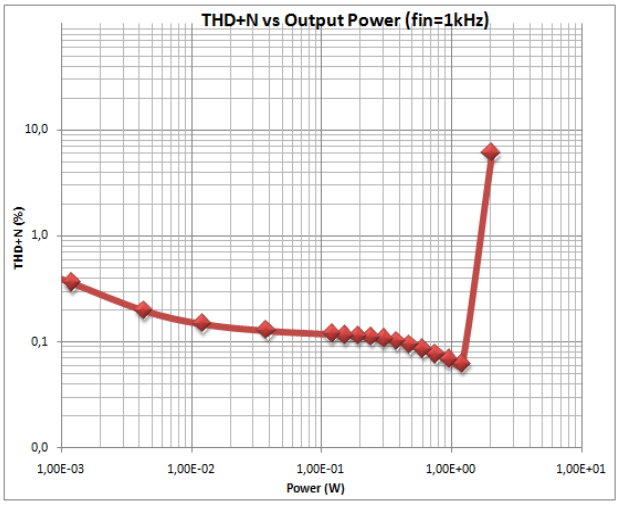

Fig.14.THD+N versus output power

5.4 Layout

The layout for the class D audio power amplifier output stage circuit is shown in figure 15. The output transistors occupy the majority of the chip area. All devices or circuits prone to produce electromagnetic interference or susceptible to interference are enclosed with double layer guard rings. The layout is done by respecting following items; design rules (DRM, MRC and Density) and designer constraints information (constraint manager, matchCat, text…). Layout is 1.2mm x 1.25mm, occupying a total area of 1.5mm^2

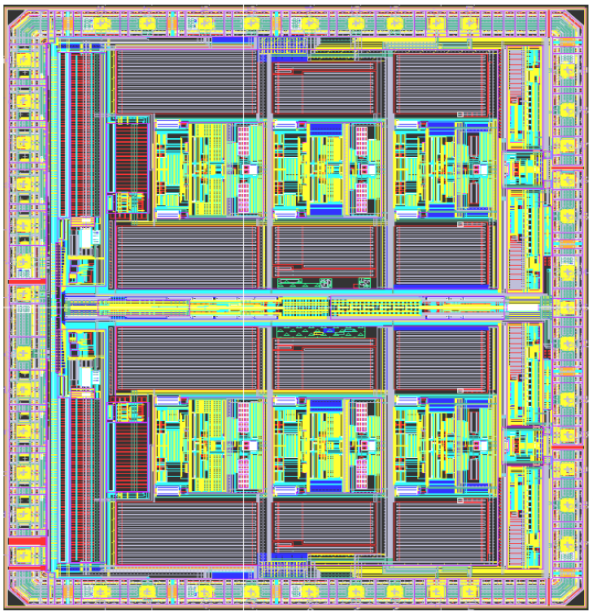

Fig.15 Layout of the proposed class-D in 130 nm SOI.

A comparison between the proposed class-D amplifier and other state-of- the art amplifier is summarized in Table 1.

Table 1 Performance summary and comparison

Reference	[1]	[2]	[4]	This Work
THD+N (%)	0.017	<0.1	0.01	0.06
Efficiency (%)	>90	94	89	93
Output power (W)	200	-	20	0.5
Load (Ω)	8/4	3	8	8
Area(mm^2)	22	-	12	1.5
Process (SOI)	-	0.14 um	0.6 um	0.13 um

4 Conclusion

In conclusion, a novel class D audio power amplifier output stage has been successfully designed in 130 nm Silicon-on-Insulator (SOI) technology. Circuit design, simulation, analysis and layout design are all included in this study. The performance of class D audio power amplifier is enhanced in this study. The proposed class-D amplifier use pulse with modulator (PWM) achieves high quality audio performance with a THD+N of 0.06%. An efficiency of 93% can be achieved with a 8-Ω load while delivering an output power of 0.5W and the total area of the class-D amplifier is $1.5mm^2$ .The results of this study show good efficiency and low distortion. The chip possesses super characteristics suitable for various applications such as automotive application.

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