Design and Analysis of 1MHz Class-E Power Amplifier

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Abstract—This paper presents the simulation and experimental of Class-E power amplifier which consists of a load network and a single transistor that is operated as a switch at the carrier frequency of the output signal. Class-E power amplifier is often used in designing a high frequency ac power source because its ability to perform the conversion efficiently even when working at high frequencies with significant reduction in switching losses. In this paper, a 10W Class-E power amplifier is designed, constructed, and tested in the laboratory with operating frequency of 1 MHz. To be specific, SK40C microcontroller board with PIC16F877A is used to generate a pulse width modulation (PWM) switching signal to drive the IRF510 MOSFET. This paper focuses on studying the effect of switching and performance analysis of the Class-E power amplifier behavior at 1MHz frequency. The performance parameter relationship of Class-E power amplifier were observed and analyzed. The theoretical calculations, simulation and experimental results at optimum operation using selected component values are compared and presented. The final result shows an output power is 9.45W with a drain efficiency of 98.44%. It is also shown that both simulation and experimental agree well with theoretical predictions.

Key-Words:- Class-E power amplifier, zero voltage switching, high frequency power amplifier

1 Introduction

Class-E switch-mode tuned power amplifier offers extremely high dc to ac conversion efficiency at high frequencies because of a significant reduction in switching losses [1-15]. The main idea behind switch-mode power amplifier technology is to operate the transistor in saturation, so that either voltage or current, depending on amplifier class, is switched on and off. Figure 1 is a block diagram of a single-ended switch-mode amplifier. The active device acts substantially as a switch when appropriately driven by the driver. The active device output is represented as a non-ideal single-pole single-throw switch. As the switch is periodically operated at the desired ac output frequency, dc energy from the power supply is converted to ac energy at the switching frequency. To obtain maximum fundamental frequency output, the switch duty ratio is made approximately 50 percent. To be specific, the switch is "on" for approximately half of the ac period and "off" for the remainder of the period. The load network may include a lowpass or bandpass filter to suppress harmonics of the switching frequency at the load, and may transform the load impedance and accommodate load reactance.

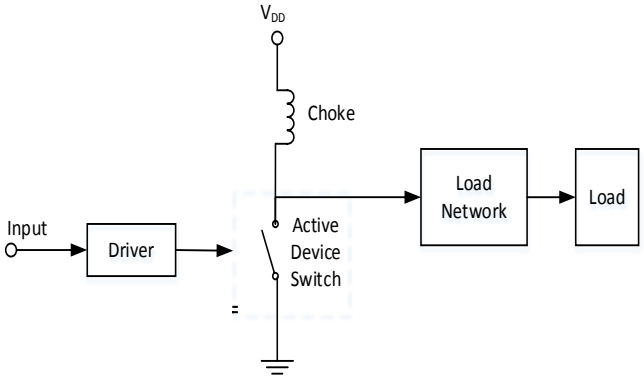


Fig. 1. Single-ended Switch-mode Power Amplifier Block Diagram

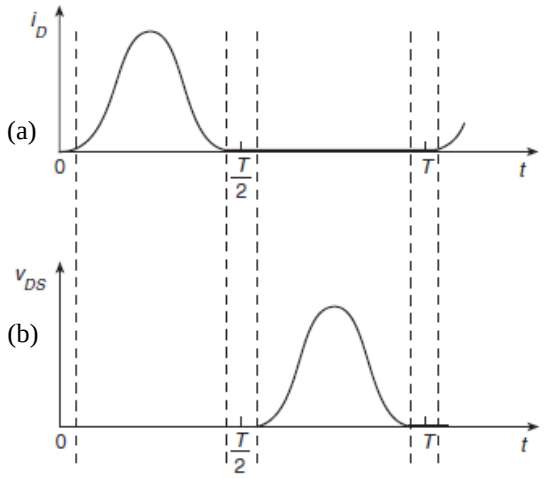


Fig. 2. (a) Current Through Switch (b) Voltage Across Switch [8]

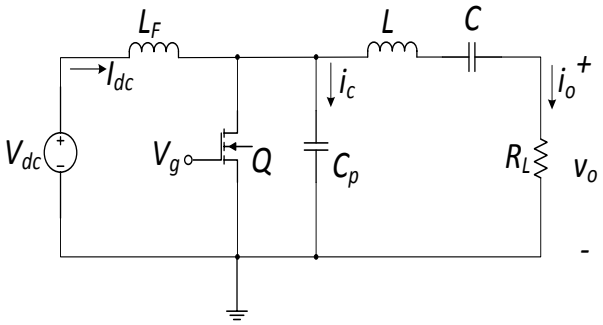


Fig. 3. Typical Class-E Power Amplifier Circuit

Figure 2(a) and (b) shows the desired current and voltage waveforms of the switch for maximum power efficiency. When the switch is open, only voltage is present over the transistor. When closed, current flows through it. Since there is no overlap in time between voltage and current, power is not dissipated and one obtains 100% theoretical efficiency. This phenomenon is known as zero voltage switching (ZVS). According to paper [4-16], Class E power amplifier is the most efficient inverter so far because of its ability to achieve ZVS.

Class-E amplification is easily differentiated from other classes of power amplification. For example, as shown in Figure 4, linear power amplifier in which the transistors is biased to an operating point and follows the indicated load line, giving rise to power dissipation and loss. In the switch-mode power amplifier such as Class-E, an output resonator helps shape the waveform by blocking harmonic components of the voltage and current. It keeps these components from reaching the load. Consequently, only fundamental current is passed to the load and only

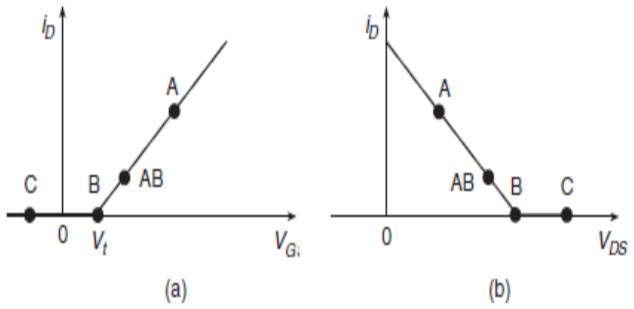


Fig. 4. Operating points for Classes A, B, AB, and C [8]

fundamental voltage is generated over the resonator. A flywheel effect is created generating sinusoidal voltage and current in the load. Theoretically, the two necessary conditions for generating a single tone with 100% efficiency in the load are: 1. zero overlap between voltage over the transistor channel and current through the channel; 2. blocking of harmonic currents to the load.

This paper presents the design and theoretical analysis for optimum operation of the Class-E power amplifier. The effect of circuit performance when the frequency, load and duty cycle varied were analyzed. The structure of this paper is arranged as follows. Section 2 explains briefly the Class-E power amplifier circuit operation. Section 3 discusses analysis of Class-E power amplifier at optimum operation. Simulation and experimental results are shown in Section 4 to verify the theoretical analysis and final conclusions are drawn in Section 5.

2 Circuit Description

The basic circuit of the Class-E power amplifier is shown in Figure 3. The details about the operating principle of Class-E power amplifier are omitted since they had appeared in [4]. This inverter is normally used for fixed output voltage. However, the output voltage can be varied by varying the switching frequency or duty cycle. The Class-E power amplifier consists of power MOSFET operated as a switch at the input frequency, and a load network which includes a shunt capacitor, and a series-resonant R_L-L-C output circuit. The choke inductor L_f is usually high enough to force a dc current, I_{dc}. To achieve ZVS condition, the operating frequency should be between the resonant frequencies f_{o1} and f_{o2} given in (1) and (2), where total equivalent capacitance $C_T = CC_p/(C+C_p)$.

$$f_{o1} = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

$$f_{o2} = \frac{1}{2\pi\sqrt{LC_T}} \quad (2)$$

The switch turns on and off at the operating frequency setting by a MOSFET gate drive. Circuit operation is determined by the switch when on and by the transient response of the load network when the switch is off. The switching pattern is defined as:

$$\text{Switch} = \begin{cases} \text{OFF state for } 0 \le \omega t < DT \\ \text{ON state for DT} \le \omega t < T \end{cases}$$

where D is the switch duty cycle and *T* is the period for one complete cycle. The MOSFET turns on and off alternately at ωt = 0 and *DT*. Therefore, the switch voltage waveform that satisfies the Class-E nominal condition, i.e., condition (3) or (4), at the switch turn on instant as a function of the duty ratio, is expressed as follows:

ZVS condition:

$$v_{ds}(DT) = 0 \quad (3)$$

Zero derivative switching (ZDS) condition:

$$\frac{dv_{ds}(\omega t)}{d(\omega t)}\Big|_{\omega t = DT} = 0 \quad (4)$$

where $v_{ds}(\omega t)$ is the switch voltage. In this case, the voltage v_{ds} across the switch and the shunt capacitance C_p is zero when the switch turns on. Therefore, the energy stored in the shunt capacitance C_p is zero when the switch turns on, yielding zero turn on switching loss.

3 Analysis of Class-E Power Amplifier

3.1 Assumptions

The analysis of the Class-E power amplifier shown in Figure 3 is carried out under the following assumptions:

1) The MOSFET and diode form an ideal switch whose on-resistance is zero, off-resistance is infinity, and switching times are zero.
2) The choke inductance is high enough so that its ac component is much lower than the DC component of the input current.
3) The loaded quality factor Q of the L,C and R_L series-resonant circuit is high enough so that the current I through the resonant circuit is sinusoidal.
4) All circuit elements are ideal.

The assumptions of the circuit are quite similar to those presented in [2, 3].

3.2 Parameters for Optimum Operation

The parameters of the circuit shown in Figure 3 are defined as follows. The derivation of all parameters are based on the papers of [1-5] and [8]. These parameters are usually required to satisfy equations (3) and (4).

The full load resistance is

$$\mathrm{R_L} = \frac{8V_{CC}^2}{(\pi^2+4)P}. \quad (5)$$

The current drawn from the DC power supply is

$$\mathrm{I_o} = \frac{P}{V_{CC}} \quad (6)$$

The component values for the load network are as follows:

$$C_p = \frac{I_o}{\omega\pi V_{CC}} = \frac{1}{\omega R\left(\frac{\pi^2}{4}+1\right)\frac{\pi}{2}}, \quad (7)$$

$$C = \frac{1}{\omega R\left(Q - \frac{\pi(\pi^2-4)}{16}\right)}, \quad (8)$$

$$L = \frac{QR_L}{\omega}. \quad (9)$$

where Q is quality factor. In order to keep the current ripple in the choke inductor stays at below 10% of the full-load DC input current I_{dc}, the value of the choke inductance must be greater than

$$L_{f(\min)} = 2\left(\frac{\pi^2}{4}+1\right)\frac{R}{f}. \quad (10)$$

In practical terms, the choke inductance value is not all that critical, as long as its impedance is at least an order of magnitude higher than the load resistance and it is not self-resonant at the first three or four harmonics. It needs to look like an open circuit to these harmonics, if possible.

4 Analysis of Class-E Power Amplifier

The design specifications used here are as follows; dc power supply, V_{cc} = 12V, operating frequency, f = 1MHz, D = 0.5, Q = 10, and Output power, P_o = 10W. Based on the design specifications and assumptions provided in Section 3, all the circuit parameters are calculated and tabulated as in Table I. Then simulations are carried out using Proteus before the real circuit is implemented. In order to validate the simulation results, the experimental work is carried out. IRF510 MOSFET is used as a switching device in the design. It is n-channel, enhancement mode and designed especially for high speed applications. Based on Table I, the peak switch voltage and current are 42.74V and 2.39A respectively. This confirms that the IRF510 MOSFET is suitable to be used in a class-E power amplifier circuit in practical applications.

In Figure 5, the SK40C microcontroller board with PIC16F887A is used to generate a 1MHz switching control signal at 50% duty cycle for the MOSFET gate. However, the microcontroller output voltage, typically. 5V is not sufficient to turn on the IRF510 MOSFET that requires at least 10V to operate in safe operating area. Therefore, an IC gate drive TC4422 is used here to provide sufficient gate voltage or charge to drive the IRF510 MOSFET.

4.1 Simulation Results

Figure 6 shows the waveforms that are obtained from the Proteus simulation. Based on the result in Figure 6(a), the maximum voltage across the MOSFET and the shunt capacitor during turn off is; $V_{ds(peak)}$ = 42.74V, which is almost three times larger than V_{CC}. Meanwhile, during turn on, $V_{ds(peak)}$ = 4.5V, nearly 11% of the peak voltage. In an optimum design yielding the maximum drain efficiency, the switch voltage V_{ds} at the switch turn on time is usually 10% to 50% of the peak switch voltage, which is a nonzero voltage switching condition. In addition, the switch voltage derivative at the switch turn on time is zero or slightly positive or negative.

Refer to Figure 6(b), the switch current, $I_{ds(peak)}$ = 2.1A, increases gradually from zero after the switch is turned on because the derivative of v_{ds} is zero at the time the switch turns on. It should be noted that both the switch voltage and the switch current are positive for optimum operation. Therefore, there is no need to add any antiparallel diode to the switch [8].

According to the theoretical predictions, the output voltage is sinusoidal at high Q. Based on Figure 6(c), peak output voltage, $V_{RL(peak)}$ = 12V at optimum load.

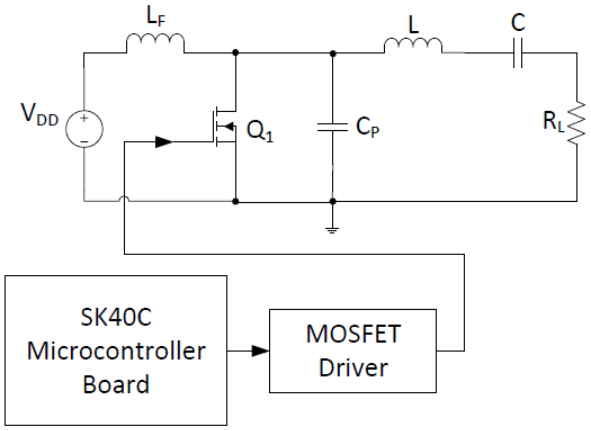


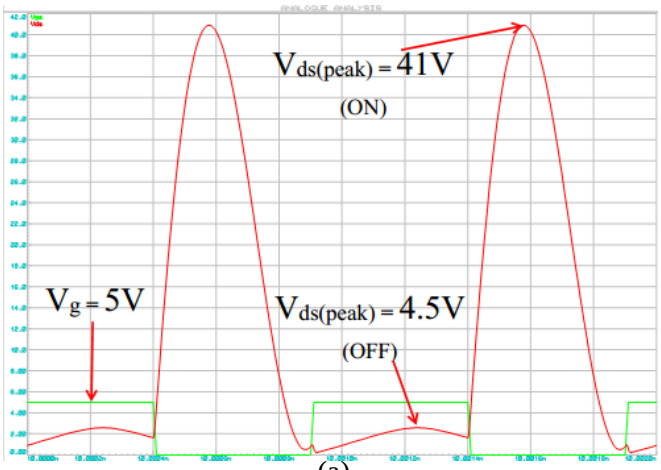
Fig. 5. Class-E Power Amplifier Experiment Circuit

TABLE I
CLASS-E POWER AMPLIFIER SIMULATION RESULTS

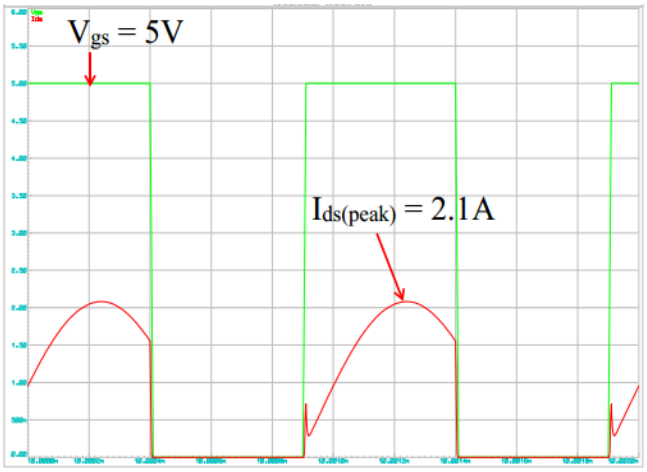
Frequency		f = 1MHz		
Result		Theoritical	Simulated	Difference (%)
R_L	Ω	8.31	8.31	0.00
Cp	nF	3.52	3.52	0.00
C	nF	2.17	2.17	0.00
Lf	uH	57.60	57.60	0.00
L	uH	13.22	13.22	
$V_{RL(peak)}$	V	12.89	12.00	6.90
$V_{ds(peak)}$	V	42.74	41.00	4.08
I_{dc}	A	0.83	0.82	1.56
$I_{RL(peak)}$	A	1.55	1.44	7.22
$V_{c(peak)}$	V	114.03	112.00	1.78
$V_{L(peak)}$	V	128.89	122.00	5.34
$I_{s(peak)}$	A	2.39	2.10	11.95
$I_{s(rms)}$	A	1.28	1.26	1.63
$P_{o(ac)}$	W	10.01	8.62	13.91
$P_{i(dc)}$	W	10.00	9.84	1.56
η	%	100.12	87.56	12.55

The dc power input is $P_{i(dc)} = V_{CC}x\ I_{dc}$= 9.84W. The simulated ac output power, $P_{o(ac)} = (I_{RL(rms)})^2$*RL = 8.62W. In term of efficiency, it can be seen that the circuit produces 86.16% efficiency, slightly lower than the calculated value. However, the simulation results are consistent with the theoretical ones. In fact, all results in this section show that the Class-E power amplifier circuit satisfies the ZVS conditions since there is no overlap in time between voltage and current.

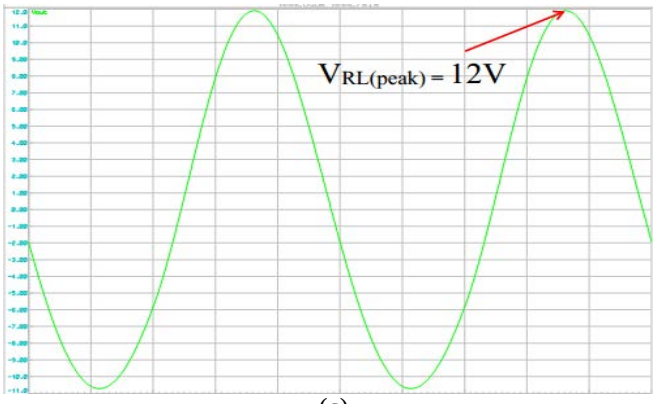
4.2 Experimental Result



(a)



(b)



(c)

Fig. 6. PROTEUS Simulation Waveforms: (a) Vgs versus Vds at 1MHz (b) Vgs versus Ids at 1MHz (c) Output Voltage Across R_L,V_{RL}

Figure 7 shows the experimental setup for 1MHz Class-E power amplifier circuit. Figure 8 shows the waveforms obtained from laboratory circuit experiment. As shown in Table II, the measured value of the resonance frequency is 1MHz. The peak output voltage, $V_{RL(peak)}$ =

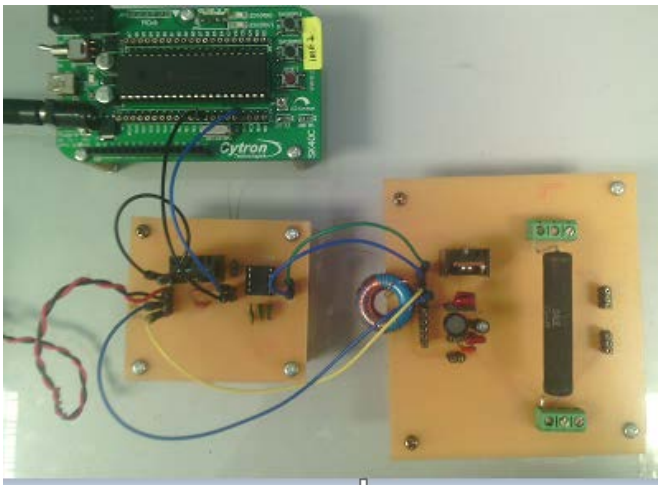


Figure 7: 1MHz Class-E Power Amplifier Experimental Setup

TABLE II
CLASS-E POWER AMPLIFIER EXPERIMENT RESULTS

Frequency		f = 1MHz		
Result		Theoritical	Measured	Difference
R_L	Ω	8.31	8.4	-1.08
Cp	nF	3.52	3.60	-2.33
C	nF	2.17	2.20	-1.57
Lf	uH	57.60	100.00	
L	uH	13.22	13.30	-0.61
$V_{RL(peak)}$	V	12.89	12.50	3.02
$V_{ds(peak)}$	V	42.74	39.00	8.76
I_{dc}	A	0.83	0.80	3.96
$I_{RL(peak)}$	A	1.55	1.50	3.35
$V_{c(peak)}$	V	114.03	108.50	4.85
$V_{L(peak)}$	V	128.89	125.50	2.63
$I_{s(peak)}$	A	2.39	2.30	3.56
$I_{s(rms)}$	A	1.28	1.20	6.40
$P_{o(ac)}$	W	10.01	9.45	5.58
$P_{i(dc)}$	W	10.00	9.60	3.96
η	%	100.12	98.44	1.68

12.5V which is 3.02% lower than the theoretical value. The experimental value for the maximum voltage across the MOSFET during turn off is $V_{ds(peak)}$ = 39V which is 8.76% lower than the theoretical ones. The dc power input is $P_{i(dc)} = V_{CC}x\ I_{dc}$= 9.6W. The simulated ac output power, $P_{o(ac)} = (I_{RL(rms)})^2$*RL = 9.45W. In term of efficiency, it can be seen that the circuit produces 98.44% efficiency, which is 1.68% lower than the theoretical value. There are slightly differences in

measured values due to power amplifier losses occurred in the parasitic resistance of each components, switching losses and dissimilarity in component selections.

The main reason is the difference value of the load resistor. Since the measured load resistance is 1.08% greater than the theoretical value ($R_L > R_{opt}$), the optimum operation cannot be achieved. The amplitude of the current through the L-C R series resonant circuit is lower than that optimum operation, the voltage drop across the shunt capacitor C_p decreases, and the switch voltage V_{ds} is not equal to zero at turn on. Therefore, the energy stored in C_p is dissipated in the MOSFET as heat after the switch is turned on, resulting in a turn on switching loss.

In order to transfer a specified amount of power P_o at a specified dc voltage V_{dc}, the load resistance must be of the value determined by equation (5). However, in practical applications, the load resistance is available and sometimes the practical load resistance is different from that given in (5). Therefore, there is a need for matching circuits that could provide impedance transformation in order to increase the measured efficiency near to the theoretical ones. This impedance transformation can be accomplished by tapping the resonant capacitance, parallel with the load resistor. Furthermore, in real circuit implementation, a transistor is not an ideal switch, overlap does happened and limit the efficiency.

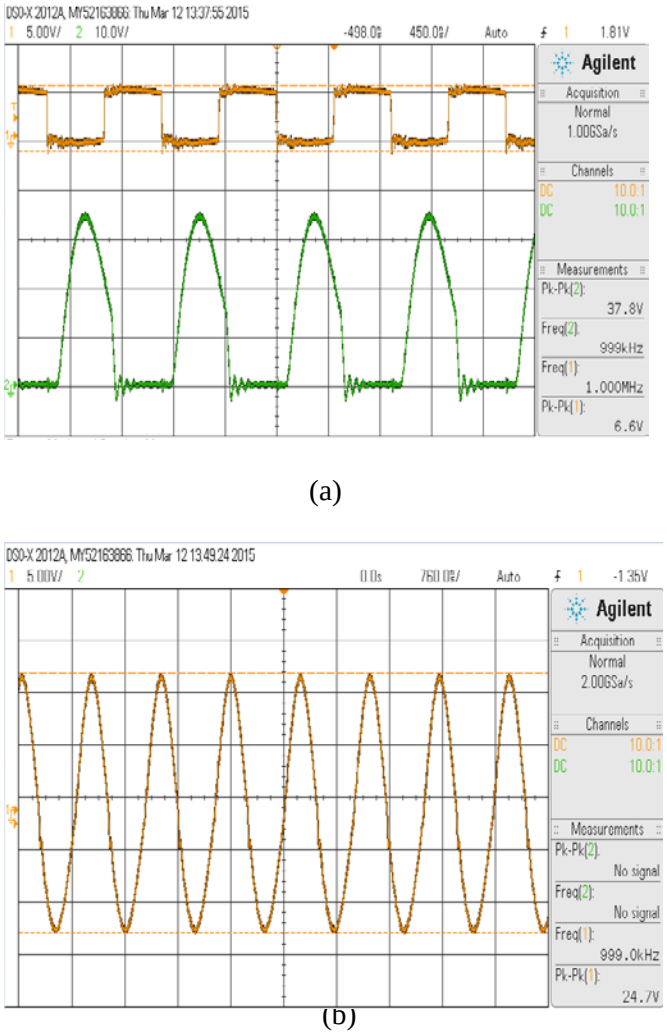


Fig. 8: Experimental Waveforms: (a) Switch Voltage and Gate Voltage (b) Output Voltage Across R_L,V_{RL}

5 Conclusion

An analysis of the Class-E power amplifier operation has been presented in this paper. The switch control signal for IRF510 MOSFET using microcontroller PIC16877A has been proposed and the results indicate that ZVS condition can be achieved successfully. In the laboratory experiment, the Class-E with optimum load and D = 0.5 has achieved 98.44% efficiency at 10W output power for 1MHz operating frequency. Moreover, the agreement between experiment performance and theoretical performance can still be considered excellent. For future development, this circuit will be applied at the transmitter side of a capacitive power transfer system.

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