Single-phase M-channel interleaved and N-switch Paralleled power factor corrector using EL model passivity control

WANG Nan[1], LU Fei[1], YANG Xi-jun[1], LIU Ming-lin[2], LEI Huai-gang[2]
([1]Key Laboratory of Control of Power Transmission and Conversion, Ministry of Education
(Department of Electrical Engineering, Shanghai Jiao Tong University), Shanghai 200240, China)
([2]shanghai Ruking Electronic Technology Co. LTD, Shanghai 200072, China)

Abstract: For high-power home inverter air conditioners and other electrical equipment which are supplied by single-phase AC power source, single-phase power factor correction (APFC) is needed. For example, multi-level interleaved APFC or single-level APFC with multiple power devices in parallel. This paper proposes a new single-phase M level and N power devices in parallel PFC which is driven by shift phase control method. Then the paper analysis its circuit structure and working principle, including voltage transformation ratio, ripple current, driving method and control methods. This MN APFC can transmit high power and reduce the switching frequency of the power devices. This circuit structure simplifies the selection of power devices. Meanwhile, it can also maintain the operating frequency of the boost inductor unchanged or maintain the switching frequency of the power device constant. This control method improves the operating frequency of the boost inductor several times and simplifies the inductor design. This paper establishes the EL (Euler-Lagrange) mathematical model of MN PFC which is working in continuous conduction mode (CCM) based on its power circuit. The passivity of MN PFC is proved and passivity-based controller using stated variables feedback, damping injection method is designed in this paper. The proposed control scheme which don't need proportion integral controller has strong robustness on disturbance of input voltage, load and parameters of system components. Especially in applications of wide range load, the dynamic response of input current is very fast and the output voltage almost has no changes so that the power factor correction and constant DC output functions of PFC are realized. Meanwhile, MN PFC employing passivity-based controller has a good effect on current sharing. Then, as 2x2 PFC for example, this method is simulated and analyzed by MATLAB/SIMULINK. Simulation results show that the passivity-based controller has a superior performance and the method is feasible.

Key words: Power factor correction, two-channel interleaved, two-device paralleled, phase-shifted driving, passivity-based control, current sharing

1 Introduction

Single-phase active power factor corrections (APFC) can eliminate harmonic currents and gain unitary power factor at mains, which can make electric equipment fed by single-phase power supply meet the harmonic current standards[1~2]. It has been extensively applied to inverter household appliances and communication power supplies. APFC has made great progress in circuit topology, control strategy, modulation algorithm, analyses approach and implementation technology. In terms of circuit topology, quite a lot of different circuit structures arise, inclusive of bridged APFC and bridgeless APFC[3], single-channel APFC and interleaved APFC[4~7], two-level APFC and three-level APFC[8~11], and so on.

In the field of inverter air-conditioner, in order to increase power ratings, to facilitate the select the power devices and mounting and to decrease the overall cost, multi-channel interleaved APFC (IPFC) are employed gradually. Though the boost inductors can be mounted on the print circuit board (PCB), the equivalent ripple frequency of inductor current equates that of power devices, which causes complicated design and control with high number of channel. Only if multi-device paralleling method and synchronous driving are used in single-channel APFC, which can raise the power stage, however it is difficult to mount the inductors on board and makes design complicated due to excessive power devices. Therefore, in this paper, a novel control idea are presented, that is, on the basis of principle of multi-channel interleaved APFC and multi-device paralleling method, a phase-shift driving method is utilized to drive power devices,

---

This paper is supported by the China national natural science funds (60934005), and supported by 2011 Minhang district technology innovation project: enterprise-university cooperation.

aiming at increasing the power rating, improving the selection and design of boost inductor and power devices.

In general, interleaved APFC operates as follows: to sample the instantaneous output voltage, the inductor currents and the rectified AC voltage in advance, then to control its operation by adopting linear control theories[12~14]. It is evident that linear control theories bring about a slow response of inductor current and an inferior dynamic performance, which leads to an unsatisfactory control effect under a widely varying load. In terms of switching characteristics of APFC, it is periodic time-varying structure system, so advanced non-linear control strategies can benefit the control effects. Passivity control is a kind of energy control in essence, which is widely used in controlled rectifier [15~16], DC-DC converters [17~18], active power filter, etc. playing a very good role and showing promotion value. In the process of design of controller, the energy function can gain accelerated convergence by injecting appropriate damping, meanwhile the stability of control system can be guaranteed [19~21]. Considering all of that, in the paper, take two-channel interleaved and two-switch paralleled power factor corrector (2x2 APFC) for instance, the modulation principle and Euler-Lagrange (EL) mathematical model are analyzed, then the passivity controller is designed using state feedback and damping injection, in order for fast current response, stable DC voltage, excellent current-sharing, better resistance to disturbance ability, etc.

2 Circuit topology and modulation principle

The general M-channel interleaved and N-switch paralleled power factor corrector (MxN APFC) is shown in Fig.1, which is powered by single-phase AC power supply and produces DC voltage at output and sinusoidal current at input. It consists of diode rectifier B1 (D1~D4), boost inductors (L1~LM), fast recovery diodes(FRD, D1~DM), power devices (S11~S1N,… SM1~SMN), electrolysis capacitor (E1), filtering capacitor (C1) and stabilizing resistor (R1), where L1, D1 and S11~S1N Constitute the first-channel APFC, LM, DM and SM1~SMN Constitute the M-channel APFC. There all N power switches in each-channel APFC.

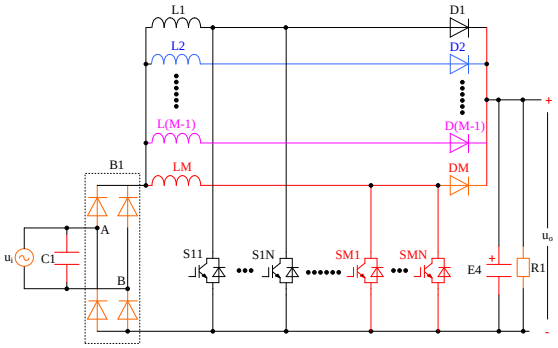

Fig.1 Power stage of MxN APFC

2.1 M-channel single-device APFC

The M-channel interleaved APFC is shown in Fig.2, where each-channel APFC shares the output voltage control signal from voltage control outer loop, and current control inner loop can employs all of the existing control methods. In contrast, power devices belonging to each-channel interleaved APFC are driven in a staggering manner of phase-shift of 360°/M or time-shift of switching-period/M. Assuming the carrier frequency is f_s, then the switching frequency of each power switch is f_s, the current ripple frequency of boost inductor is f_s, and the synthesis current ripple frequency of M inductors is Mf_s. Considering each-channel APFC shares voltage control outer loop, then the voltage transfer-ratio caused by each-channel APFC between output side and input side is written as below:

$$U_{dc} / |u_{in}| = 1/(1-D) \qquad (1)$$

where U_{dc} represents output DC voltage, $|u_{in}|$ represents absolute AC input voltage, D represents duty cycle of power device, D falls into the interval [0, 1]. In practice, the valid upper limit of duty cycle is about 0.95.

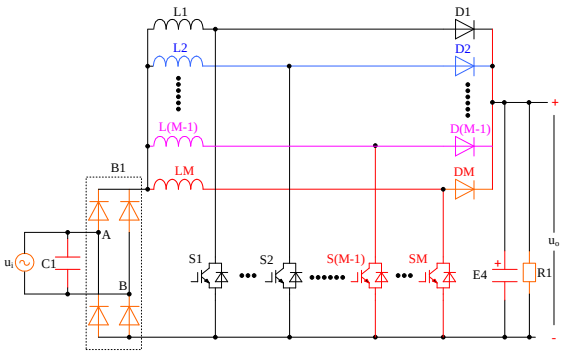

Fig.2 Power stage of M-channel APFC

Since each-channel of APFC works independently, then it undertakes the delivered power of P_o/M, where

P_o is the total delivered power. The conduction currents of power device and boost inductor are identical, and current stresses of power device are reduced by M times.

2.2 N-power device paralleled (Driven in synchronous manner)

Single-channel N-device paralleling APFC is shown in Fig.3. Considering the N devices use the same driving signal, they can be treated as only one device. Also assuming the carrier frequency is f_s, then the switching frequency of each power switch is f_s, and the current ripple frequency of boost inductor is f_s. The voltage transfer ratio of single-channel APFC between output side and input side can be written as equation 1. The maximum duty cycle of power device approaches one, and the valid upper limit of duty cycle is about 0.95.

Given power devices connected in-parallel have the same switching characteristics, then each of them undertakes the delivered power of P_o/M, so the conduction current of power device is 1/N of the current of boost inductor. Because these power devices are employed in discrete design, the problem of current sharing among N devices ought to be especially considered. The larger N is, the more complicated the design is.

2.3 N-power device paralleled (Driven in phase-shift manner)

Single-channel N-device paralleling APFC is shown in Fig.3, where the N devices are driven in phase-shift manner. Assuming the carrier frequency is f_s, then the switching frequency of each power switch is f_s, and the current ripple frequency of boost inductor is Nf_s.

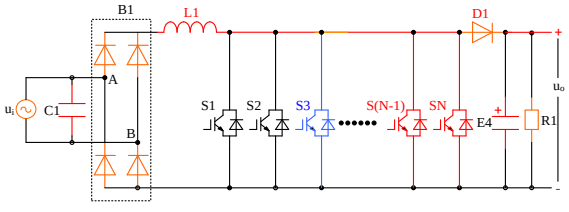

Fig.3 Power stage of single-channel N-device paralleling APFC

The single-channel APFC has a voltage control outer loop and a current control inner loop. The topology has only one final control signal and two available control methods:

(1) It employs one carrier signal and produces the first driving pulse, then produces the other N-1 driving pulses by shifting first driving pulse.

(2) It employs N carrier signals shifted by 360°/N to one another and produces the N driving pulses accordingly.

Under the former two circumstances, the voltage transfer ratio of single-channel APFC between output side and input side can be derived as equation 1. The maximum duty cycle of power device approaches one. However the power devices are switched on/off in an interleaved manner, it is easy to draw the conclusion that the maximum duty cycle of each device is less than 1/N, otherwise the sum of duty cycle of each-device would be larger than one, which would bring about the consequence that the inductor is charged successively, and it has no time to release energy into the post-stage electrolysis capacitor bank.

$$U_{dc}/\left|u_{in}\right|=1/\quad 1\text{-}ND \qquad (2)$$

Theoretically, the maximum duty cycle of each power device is 1/N. Of course, the valid upper limit of duty cycle is less than 1/N. Accordingly, the current ripple frequency of boost inductor increases by N times. The resultant current ripple is relevant to the variation of the input AC voltage.

Assuming the power devices connected in-parallel are of the same characteristic, each of them takes the power by P_o/N, therefore the total conduction current of power device is identical to that of the boost inductor. The conduction time of each power device decrease by N times, while at the same time their current stresses remain unchanged basically.

2.4 MxN APFC (Driven in phase-shift manner)

The general M-channel interleaved N-switch paralleled power factor corrector (MxN APFC) is shown in Fig.1. Each channel of APFC is regulated by T_s/M, where T_s represents switching period. At switching-period/M of each-channel, the N devices belonging to one channel of APFC are driven in a staggering manner of phase-shift by 360°/MN or of

time-shift by T_s/MN. Each channel of APFC takes the power of P_o/M. The current ripple frequency of boost inductor is Nf_s, the synthesis current ripple frequency of inductors is MNf_s, and the conduction current of power device is 1/M of overall current of boost inductor.

According to the above analysis, two driving approaches are put forwards:

(1) One switching period is divided into M equal parts, and each channel of APFC makes use of one appropriate part. Within one part, the belonged N devices are switched on/off in turn. The phase shift is 360°/MN, and the maximum duty cycle of power device is (1-1/MN).

(2) One switching period is divided into M equal parts, and the N devices of each-channel APFC are scattered into the M parts. The phase shift is 360°/M, and the maximum duty cycle of power device is (1-1/M).

Take 2-channel interleaved 2-switch paralleled power factor corrector (2x2 APFC) for instance, which is shown in Fig.4. For driving method 1, within one entire switching-period, the switching-on order of the power device is $S_{11}\rightarrow S_{12}\rightarrow S_{21}\rightarrow S_{22}$. The maximum duty cycle of power device is 0.75. While for driving method 2, the order is $S_{11}\rightarrow S_{21}\rightarrow S_{12}\rightarrow S_{22}$. The maximum duty cycle of power device is 0.5.

Take 3-channel interleaved 2-switch paralleled power factor corrector (3x2 APFC) for instance, , which is shown in Fig.5. For driving method 1, within one entire switching-period, the switching-on order of the power device is $S_{11}\rightarrow S_{12}\rightarrow S_{21}\rightarrow S_{22}\rightarrow S_{31}\rightarrow S_{32}$. The maximum duty cycle of power device is 0.75. While for driving method 2, the order is $S_{11}\rightarrow S_{21}\rightarrow S_{31}\rightarrow S_{12}\rightarrow S_{22}\rightarrow S_{32}$. The maximum duty cycle of power device is 0.33.

It is clear that each channel of APFC has only one final control signal, two control approaches are put forwards:

(1) To employ one carrier signal, and to get one driving pulse by comparing it with the final current inner loop control signal, then to get the other N-1 driving pulses by phase-shifting the pulse.

(2) To employ N phase-shifted carrier signals and to get the other N driving pulses by comparing them with the final current inner loop control signal one by one.

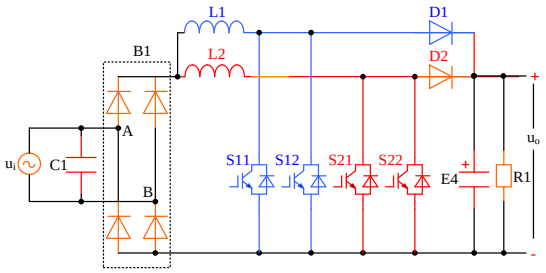

Fig.4 Power stage of two-channel N-device paralleling APFC

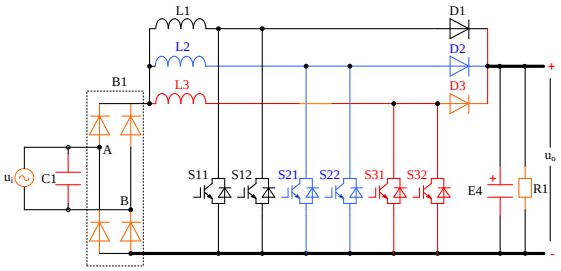

Fig.5 Power stage of three-channel 2-device paralleling APFC

In this paper, the first driving approach and second control approach are employed. For 3x2 APFC, the phase shift of the four power devices is 90°, the switching states are listed as below:

(1) When D falls into the interval [0, 1/4), the number of the switched-on devices is 1、0、1、0 … … in time domain, where D represents the duty cycle of a single power device ;

(2) When D is 1/4, the number of the switched-on devices is 1、1、1、1 …… in time domain;

(3) When D falls into the interval [1/4, 1/2), the number of the switched-on devices is 2, 1, 2, 1 …… in time domain;

(4) When D is 1/2, the number of the switched-on devices is 2, 2, 2, 2 …… in time domain;

(5) When D falls into the interval [1/2, 3/4), the number the switched-on devices is 3, 2, 3, 2 …… in time domain;

(6) When D is 3/4, the number of the switched-on devices is 3, 3, 3, 3 …… in time domain;

(7) D falls into the interval [3/4, 1], the number of the switched-on devices is 4, 3, 4, 3… in time domain;

When D falls into the interval [3/4, 1], it can be

easily seen that the inductor has no time to release its stored energy and the APFC fails to work, so it doesn't have practical significance in the situation.

Given U_{dc} is the average output DC voltage with a small ripple, u_{in} is the instantaneous input AC voltage. When D falls into the interval [1/4, 3/4], take branch L_1 for instance, the switching states are shown in Fig.6.

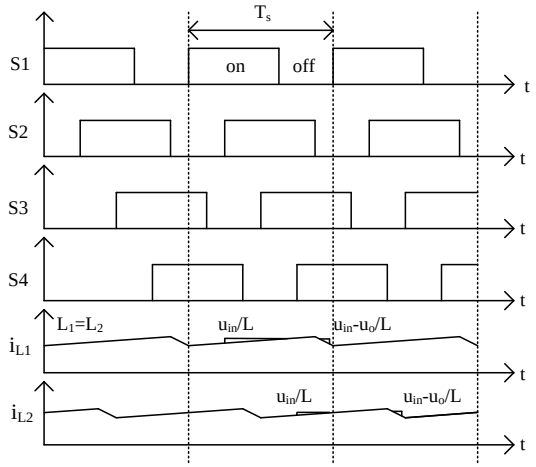

Fig.6 Waveforms of inductor currents and driving pulses when $1/4 < D < 3/4$

When $(1/4+D)T_s$,

$$u_{in} = \mathrm{L}_1 \frac{di_{L1}}{dt} \tag{3}$$

When $(3/4-D)T_s$,

$$u_{in} = \mathrm{L}_1 \frac{di_{L1}}{dt} + U_{dc} \tag{4}$$

According to the balance equation of volt-second product,

$$u_{in}(D+1/4)T_s = (U_{dc} - u_{in})(3/4-D)T_s \tag{5}$$

$$\frac{U_{dc}}{|u_{in}|} = \frac{1}{3/4-D} \tag{6}$$

While D falls into the interval [0, 1/4], the switching states are shown in Fig.7.

When $2DT_s$,

$$u_{in} = \mathrm{L}_1 \frac{di_{L1}}{dt} \tag{7}$$

When $(1-2D)T_s$,

$$u_{in} = \mathrm{L}_1 \frac{di_{L1}}{dt} + U_{dc} \tag{8}$$

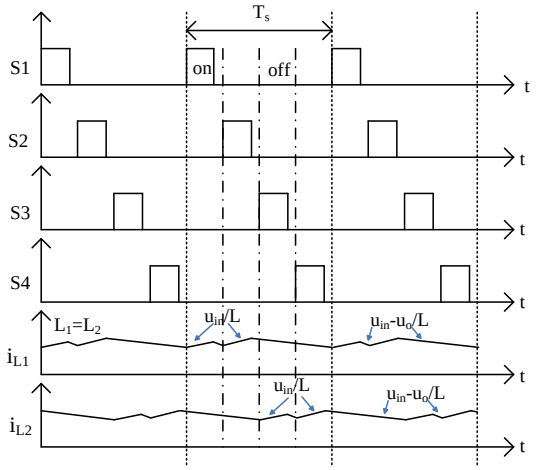

Fig.7 Waveforms of inductor current and driving pulse when $0 < D < 1/4$

According to the balance equation of volt-second product,

$$2DT_s u_{in} = (U_{dc} - u_{in})(1-2D)T_s \tag{9}$$

$$\frac{U_{dc}}{|u_{in}|} = \frac{1}{1-2D} \tag{10}$$

Take single-channel and single-device APFC, i.e. the traditional APFC, as the reference, the different performance indexes of the above mentioned APFCs' are shown in table 1.

Table 1. Performance comparison of different APFC's

	M-channel APFC	Single-channel N-paralleled (synchronous driving)	Single-channel N-paralleled (phase-shift driving)	MN APFC
Ripple frequency of inductor current	unchanged	unchanged	N times	N times
Ripple frequency of synthesized	M times	unchanged	N times	MN times

current				
Ripple amplitude of synthesized current	fall	unchanged	fall	fall
switching frequency of power device	unchanged	unchanged	unchanged	unchanged
current amplitude of power device	1/M	1/N	unchanged	1/M
Conduction loss of power device	fall	fall	Approx. 1/N	Approx. 1/N
switching loss of power device	Approx. 1/N	Approx. 1/N	unchanged	Approx. 1/N

It is evident that the performances of the M-channel interleaved APFC and the single-channel N-power device paralleled APFC which is driven in phase-shift are superior to the single-channel single-device APFC and single-channel N-power device paralleled APFC which is driven in the synchronous way.

By integrating the two circuit topologies, a new topology is proposed, which is M-channel interleaved and N-switch paralleled APFC driven by means of phase-shift. This circuit meets the requirements of high power applications. For high-power APFC, there are three available application schemes stated as below:

(1) For single-channel and single-device APFC, at present, its power rating reaches above 8kW, nevertheless the performance cost ratio is low, and the boost inductor can only be mounted off the print circuit board (PCB).

(2) For multi-channel interleaved single-device APFC, including two-channel, three-channel and four-channel, etc. their power rating can exceed 10kW. The performance cost ratio is high, and the boost inductors can be mounted on the print circuit board (PCB).

(3) For single-channel interleaved multi-switch paralleled APFC, there are all three selected schemes as bellow:

A) Maintaining the current ripple frequency of boost inductor constant and decreasing carrier frequency by many times, the conduction loss and switching loss of power device can be reduced correspondingly.

B) Maintaining the carrier frequency constant and increasing current ripple frequency of boost inductor by many times, the inductance of boost inductor can be reduced correspondingly.

C) Making balance between these two above schemes, by decreasing carrier frequency appropriately and increasing current ripple frequency of boost inductor appropriately, the conduction loss and switching loss of power device can be reduced dramatically, while at the same time the inductance of boost inductor can be reduced.

2.5 Analysis of inductor's current ripple

Considering the relationship between the inductor current of each-channel and the synthesized current, there are two situations in view of the duty cycle of each IGBT as below:

$$D_i = 4D \qquad (0<D<1/4) \tag{11}$$

$$D_i = 2D - 1/2 \qquad (1/4<D<3/4) \tag{12}$$

where D represents the duty cycle of IGBT, and D_i represents the duty cycle of synthesis current.

When 0<D<1/4, the inductor current of each-channel and synthesis current is shown in Fig.8. The waveforms and data come from the simulation analysis by means of MATLAB/Simulink. The ripple frequency of synthesized current behaves as the four times of the carrier frequency.

As shown in Fig.8, the decreased input current ripple profits from the reasonable current phase-shift of L1 and L2. Assuming the inductances of L1 and L2 are L, and the switching period is T_s, then

$$\Delta i_{L1} = \frac{u_{in}(t)}{L} \cdot 4D(t) \cdot \frac{T_s}{4} \tag{13}$$

$$\Delta i_{L2} = \frac{u_{in}(t) - U_o}{L} \cdot 4D(t) \cdot \frac{T_s}{4} \tag{14}$$

$$u_{in}(t) = U_o[1-2D(t)] \quad (15)$$

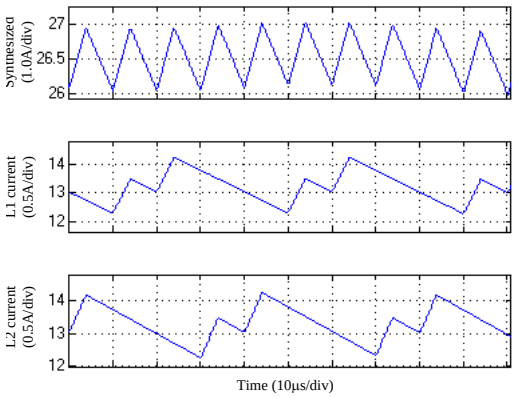

Fig.8 Waveforms of synthesized inductor current $(0<D<1/4)$

Add equations 9, 10, 11 and 12 together, according to equation 13, when 0<D<1/4, the peak value of ripple current of inductor is written as below:

$$\Delta i_{in} = \frac{T_s U_o}{L}(-4D^2 + D) \quad (16)$$

Likewise, when 1/4<D<3/4, the peak of ripple current of whole inductor is written as below:

$$\Delta i_{in} = \frac{T_s U_o}{2L}(-4D^2 + D) \quad (17)$$

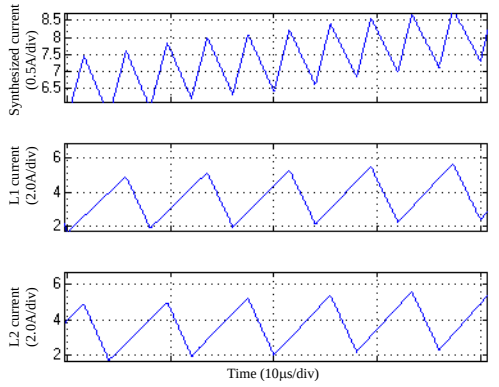

Fig.9 Waveform of total inductor current **(**1/4<D<3/4**)**

Obviously, the input ripple current of interleaved APFC is less than those of any inductors. When D=1/4, the ripple currents of inductors cancel out each other, the input ripple current is zero. When D=1/8, the peak of ripple current is greatest.

3 Passive control theories

3. 1 EL model of 2x2 APFC

Considering the conduction resistances of boost inductors, power devices and fast recovery diodes and sense resistors, which are connected in series with the power devices at the emitter, a modified topology of 2x2 APFC is shown in Fig.10, where R1 and R2 are the equivalent series resistance of inductors L1 and L2 respectively. Assuming the each inductor is linear and omitting the inductor saturation, R_{s11}, R_{s12}, R_{s21}, R_{s22} is the sum of conduction resistance and sense resistance of power switches. Sense resistance is 10mΩ, and R_c is the equivalent resistance of electrolysis capacitors at output side. R' refers to the parallel equivalent resistance of R and R_C, $R' = RR_c/(R+R_c)$.

Define S_i (i=1, 2, 3, 4) is binary logic switching function, S_i=1 indicates that the device is switched on and S_i=0 indicates that the device is switched off. i_1, i_2, i_3, i_4 of power devices and u_c of electrolysis capacitors are chosen state variables.

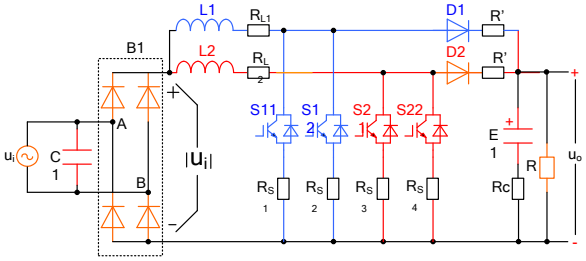

Fig.10 Power circuit of 2x2 APFC

According to Fig.10, the state space functions are written as follow:

$$\begin{cases} L_1\dfrac{di_{11}}{dt} = u_i - [R_1 + R_{s11}S_{11} + \dfrac{RR_c}{R+R_c}(1-S_{11})]i_{11} - (1-S_{11})U_o \\ L_1\dfrac{di_{12}}{dt} = u_i - [R_1 + R_{s12}S_{12} + \dfrac{RR_c}{R+R_c}(1-S_{12})]i_{12} - (1-S_{12})U_o \\ L_2\dfrac{di_{21}}{dt} = u_i - [R_2 + R_{s21}S_{21} + \dfrac{RR_c}{R+R_c}(1-S_{21})]i_{21} - (1-S_{21})U_o \\ L_2\dfrac{di_{22}}{dt} = u_i - [R_2 + R_{s22}S_{22} + \dfrac{RR_c}{R+R_c}(1-S_{22})]i_{22} - (1-S_{22})U_o \\ C\dfrac{du_C}{dt} = (1-S_{11})i_{11} + (1-S_{12})i_{12} + (1-S_{21})i_{21} + (1-S_{22})i_{22} - \dfrac{U_o}{R} \end{cases} \quad (18)$$

where u_i denotes the rectified input voltage just after the single-phase rectifier, change equation 18 into EL model:

$$\mathbf{M\dot{x} + Cx + Rx = u} \quad (19)$$

where M denotes a defined positive diagonal matrix; C denotes a anti-symmetrical matrix, $\mathbf{C = -C^T}$, indicating the interconnection inside the system; R denotes the

system dissipation element matrix, reflecting system dissipation characteristics; u denotes system outer in put vector; x denotes system state variables.

The above matrices are expressed as below:

$$\mathbf{M}=\begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_1 & 0 & 0 & 0 \\ 0 & 0 & L_2 & 0 & 0 \\ 0 & 0 & 0 & L_2 & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix}$$

$$\mathbf{C}=\frac{R}{R+R_C}\begin{bmatrix} 0 & 0 & 0 & 0 & (1-S_1) \\ 0 & 0 & 0 & 0 & (1-S_2) \\ 0 & 0 & 0 & 0 & (1-S_3) \\ 0 & 0 & 0 & 0 & (1-S_4) \\ -(1-S_1) & -(1-S_2) & -(1-S_3) & -(1-S_4) & 0 \end{bmatrix}$$

$$\mathbf{R}=\begin{bmatrix} \phi_1 & 0 & 0 & 0 & 0 \\ 0 & \phi_2 & 0 & 0 & 0 \\ 0 & 0 & \phi_3 & 0 & 0 \\ 0 & 0 & 0 & \phi_4 & 0 \\ 0 & 0 & 0 & 0 & \dfrac{1}{R+R_C} \end{bmatrix}$$

$$\phi_i = R_i + R_{Si}S_i + \frac{RR_C(1-S_i)}{R+R_C} \text{ (i=1、2、3、4)}$$

$$\mathbf{u}=\begin{bmatrix} u_i & u_i & u_i & u_i & 0 \end{bmatrix}^T$$

$$\mathbf{x}=\begin{bmatrix} i_1 & i_2 & i_3 & i_4 & u_C \end{bmatrix}^T$$

3.2 Passivity control method and system passivity proof

For a non-linear system S,

$$S:\begin{cases} \dot{\mathbf{x}} = \mathbf{f(x)} + \mathbf{g(x)u} \\ \mathbf{y} = \mathbf{h(x)} \end{cases}$$

where $x \in R^n$, $u \in R^m$ is the input, $y \in R^m$ is the output. If the semi-defined positive energy storage function exists H(x) and defined positive function Q(x) exists, if $\forall t > 0$ makes the dissipation inequality

$$\dot{\mathbf{H}} \le \mathbf{u^T y} - \mathbf{Q(x)} \tag{20}$$

come into being, where $\mathbf{u^T y}$ denotes the system energy supply rate, then the system is strictly passive. The dissipation inequality indicates the passive system operates in accompany with the energy losses, therefore if smooth differential defined positive energy storage function H(x) exists, $\dot{\mathbf{x}} = \mathbf{f(x)} + \mathbf{g(x)u}$ is stable at origin, and the function can be used as Lyapunov function[14].

The involved converter system in the paper is 2x2 APFC, where the two paralleled power devices works as a power device equivalently, therefore the system could treated as two-channel interleaved APFC (IPFC). Also considering the individual strict passive systems after interleaved is also a strict passive system, so it is only required to proof that single-channel APFC is strict passive.

To select the energy function $\mathbf{H} = \mathbf{x^T M x}/2$, then $\dot{\mathbf{H}} = \mathbf{x^T M \dot{x}} = \mathbf{x^T u - x^T R x}$.

Let y=x, $\mathbf{Q}(x) = \mathbf{x^T R x}$.

Apparently, The single-channel APFC and 2x2 APFC is strictly passive.

3.3 Determination of the desired balance point for passivity controller design

When 2x2 APFC operates, it can obtain unitary input power factor and constant DC voltage U_{DC}. According to the steady state operation characteristics of BOOST converter, APFC's steady state equations can be derived:

$$\begin{cases} I_{in}^* = \dfrac{U_{in}}{(1-2d)^2 R} \\ U_o^* = \dfrac{U_{in}}{1-2d} \end{cases} \quad (0 < d < \frac{1}{4}) \tag{21}$$

$$\begin{cases} I_{in}^* = \dfrac{U_{in}}{(\frac{3}{4}-d)^2 R} \\ U_o^* = \dfrac{U_{in}}{\frac{3}{4}-d} \end{cases} \quad (\frac{1}{4} < d < \frac{3}{4}) \tag{22}$$

where I_{in}^* and U_o^* refers to the average input current and average output voltage when the converter works at equilibrium point; U_{in} refers to average input voltage.

Given the input current I_{in}^*, then

$$I_{in}^* = \frac{U_o^{*2}}{U_{in} R} \tag{23}$$

Based on the above equation, near equilibrium point, it is possible to keep the output voltage unchanged by regulating the input current. So system desired stable equilibrium point can be

$$\begin{aligned} x_1^* &= x_2^* = x_3^* = x_4^* \\ &= \frac{1}{4} I_{in}^* \left|\sin \omega t\right| = \frac{U_o^{*2}}{4U_{in} R} \left|\sin \omega t\right| \end{aligned} \tag{24}$$

$$x_5^* = U_{DC} \tag{25}$$

3.4 Passivity controller design

The basic concept of passivity controller is from Euler-Lagrange equation of the system, to extract the matrix structure of the system, to separate the matrix C of the system which reflects the passive power term

Since passive power term does not work and consumes no power loss, it can simplify system's controller design by means of proper configuration. Injection of damping term can force the total system energy track desired energy function and make the system's output error gradually approach zero.

To design state feedback control law, make x gradually track desired value x*. Let x_e= x -x*, to select system's error energy storage function

$$\mathbf{H_e} = \frac{\mathbf{1}}{\mathbf{2}}\mathbf{x_e}^{\mathbf{T}}\mathbf{M}\mathbf{x_e} \tag{26}$$

In order to make the system quickly converge to the desired point, to make error energy quickly converge to zero, it is needed to inject damping to speed up the system's energy dissipation. While at the same time in order to realize the dynamic and static performance decoupling control, to design it in the following manner:

To set $\mathbf{R_d x_e} = \mathbf{(R + R_a)x_e}$, where Ra stands for damping injection defined positive matrix. Then equation 19 can be rewritten as:

$$\begin{aligned}&\mathbf{M\dot{x}_e + R_d x_e} = \\ &\mathbf{u} - [\mathbf{M\dot{x}^* + C(x^* + x_e) + Rx^* - R_a x_e}]\end{aligned} \tag{27}$$

To select the control law,

$$\mathbf{u = M\dot{x}^* + Cx + Rx^* - R_a x_e} \tag{28}$$

The control law 26 can make

$$\dot{\mathbf{H}}_\mathbf{e} = -\mathbf{x_e}^{\mathbf{T}}\mathbf{(R + R_a)x_e} < 0 \tag{29}$$

To substitute equation 19 for equation27, then

$$\begin{bmatrix} u_i \\ u_i \\ u_i \\ u_i \\ 0 \end{bmatrix} = \begin{bmatrix} L_1 & 0 & 0 & 0 & 0 \\ 0 & L_1 & 0 & 0 & 0 \\ 0 & 0 & L_2 & 0 & 0 \\ 0 & 0 & 0 & L_2 & 0 \\ 0 & 0 & 0 & 0 & C \end{bmatrix} \begin{bmatrix} \dot{x}_1^* \\ \dot{x}_2^* \\ \dot{x}_3^* \\ \dot{x}_4^* \\ \dot{x}_5^* \end{bmatrix} + \frac{R}{R+R_C} \begin{bmatrix} 0 & 0 & 0 & 0 & (1-S_1) \\ 0 & 0 & 0 & 0 & (1-S_2) \\ 0 & 0 & 0 & 0 & (1-S_3) \\ 0 & 0 & 0 & 0 & (1-S_4) \\ -(1-S_1) & -(1-S_2) & -(1-S_3) & -(1-S_4) & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \end{bmatrix} + \begin{bmatrix} \phi_1 & 0 & 0 & 0 & 0 \\ 0 & \phi_2 & 0 & 0 & 0 \\ 0 & 0 & \phi_3 & 0 & 0 \\ 0 & 0 & 0 & \phi_4 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{R+R_C} \end{bmatrix} \begin{bmatrix} x_1^* \\ x_2^* \\ x_3^* \\ x_4^* \\ x_5^* \end{bmatrix} + \begin{bmatrix} R_{a1} & 0 & 0 & 0 & 0 \\ 0 & R_{a2} & 0 & 0 & 0 \\ 0 & 0 & R_{a3} & 0 & 0 \\ 0 & 0 & 0 & R_{a4} & 0 \\ 0 & 0 & 0 & 0 & R_{a5} \end{bmatrix} \begin{bmatrix} x_1 - x_1^* \\ x_2 - x_2^* \\ x_3 - x_3^* \\ x_4 - x_4^* \\ x_5 - x_5^* \end{bmatrix} \tag{30}$$

According to control law equation 29, the switching functions of power devices can be derived as:

$$\begin{cases} S_1 = \dfrac{u_i - L_1\dot{x}_1^* - (R_1 + \dfrac{RR_C}{R+R_C})x_1^* - R_{a1}x_{1e} - \dfrac{Rx_5}{R+R_C}}{R_{s11}x_1^* - (Rx_5 + RR_C x_1^*)/(R+R_C)} \\ S_2 = \dfrac{u_i - L_1\dot{x}_2^* - (R_2 + \dfrac{RR_C}{R+R_C})x_2^* - R_{a2}x_{2e} - \dfrac{Rx_5}{R+R_C}}{R_{s12}x_2^* - (Rx_5 + RR_C x_2^*)/(R+R_C)} \\ S_3 = \dfrac{u_i - L_2\dot{x}_3^* - (R_3 + \dfrac{RR_C}{R+R_C})x_3^* - R_{a3}x_{3e} - \dfrac{Rx_5}{R+R_C}}{R_{s21}x_3^* - (Rx_5 + RR_C x_3^*)/(R+R_C)} \\ S_4 = \dfrac{u_i - L_2\dot{x}_4^* - (R_4 + \dfrac{RR_C}{R+R_C})x_4^* - R_{a4}x_{4e} - \dfrac{Rx_5}{R+R_C}}{R_{s22}x_4^* - (Rx_5 + RR_C x_4^*)/(R+R_C)} \end{cases} \tag{31}$$

Different duty cycle can bring about different switching functions.

3.5 Design of online identification load observer

On the basis of the above analysis, passivity control needs information of load, inclusive of output voltage, output current and output power. For the applications with heavy load disturbance, in order to enhance the robustness of the system, designing an appropriate online identification load observer can obtain satisfactory dynamic and static characteristics under the disturbance of nearly 50% rated load. The observer mathematical model is given as below:

$$R = \begin{cases} U_o / I & \dfrac{2}{3}R_0 \le U_o / I \\ \dfrac{2}{3}R_0 & \dfrac{2}{3}R_0 > U_o / I \end{cases} \tag{32}$$

where R_o represents rated load, U_o represents output DC voltage, and I represents load current.

The aforesaid description can be in support of the implementation of 2x2 APFC, as is also proved by the follow up simulation analysis and experimental research.

4 Simulation analysis and experimental research

4.1 Simulation analysis

As a practical APFC, using passivity control strategy, 2x2 APFC is simulated by means of MATLAB/Simulink and. As a typical case, the driving pulse generation principle for any channel APFC is shown in Fig.11, and the entire simulation platform of 2x2 APFC is shown in Fig.12, where the power stage and control stage are included.

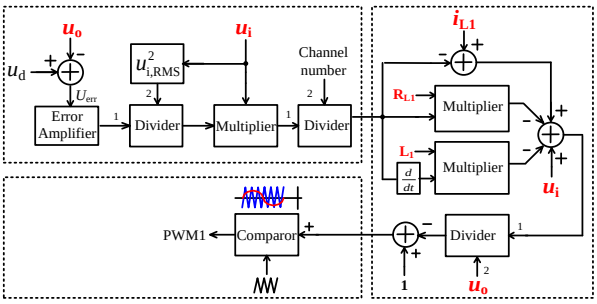

Fig.11 Principle diagram of passivity-controlled 2x2 APFC
when D∈(1/4, 3/4)

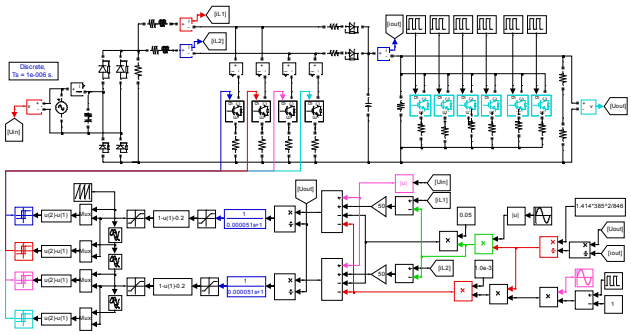

Fig.12 Simulation circuit of passivity-controlled 2x2 APFC
when D∈(1/4, 3/4)

Simulation parameters and conditions are stated as follows: the input is single-phase AC sinusoidal voltage, the desired output voltage is 385V, the inductances of L1 and L2 is 1.0mH, and their equivalent series resistance is 0.05Ω, the switching frequency is 25kHz, the load resistance is 42.35Ω, the rated load is 3.5kW. As a consequence, the RMS value of fundamental mains current is 15.91A, i.e. its peak value is 22.5A.

In the course of simulation, in order to imitate the practical situations, let the voltage drop of FRD be 1.5V, the conduction voltage drop of power device IGBT be 1.5V, the conduction resistance be 0.1Ω, the voltage drop of rectifier diode be 1.5V, AC capacitor be 2.2μF and its ESR be 5mΩ, electrolysis capacitor be 2.2μF and its ESR be 0.1Ω. Further, the damping resistances Ra1 and Ra2 are selected as 50Ω,

Under the rated output power, waveforms of the mains voltage and mains current are shown in Fig. 13. Evidently, they are all sinusoidal and in phase with each other, which indicates the unitary input power factor. The THD of mains current is only 2.33%. Additionally, duo to the direct current control, the current responds to the given conditions very fast. Waveforms of the boost inductor currents are shown in Fig. 14, and those of power devices S_{11}, S_{12}, S_{21} and S_{22} are shown in Fig. 15, and waveform of output voltage is shown in Fig. 16. It is not difficult to draw the conclusion that the simulated results are identical to those from the theoretical analysis.

APFC can gain better current and voltage tracking capability with passivity control method. When the load is changed, the system behaves with fast dynamic response. When the variation of load power is 1.0kW every 0.1s, the waveforms of the mains voltage and mains current are shown in Fig. 17, and the waveform of output voltage is shown in Fig. 18. It is can be observed that the average output voltage keeps constant without large voltage drop, and the output voltage ripple becomes large with the increase of load power. It is natural for voltage ripple to turn larger under heavier load. The output voltage ripple can be suppressed by increasing the capacitance or speeding up the response of voltage loop.

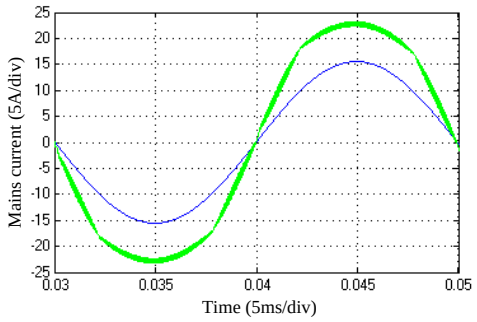

Fig.13 Waveforms of mains voltage and mains current under rated load

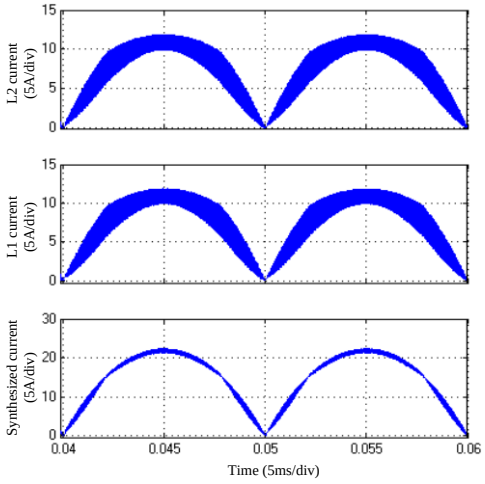

Fig.14 Waveforms of individual inductor current and synthesized inductor current (when identical

inductances)

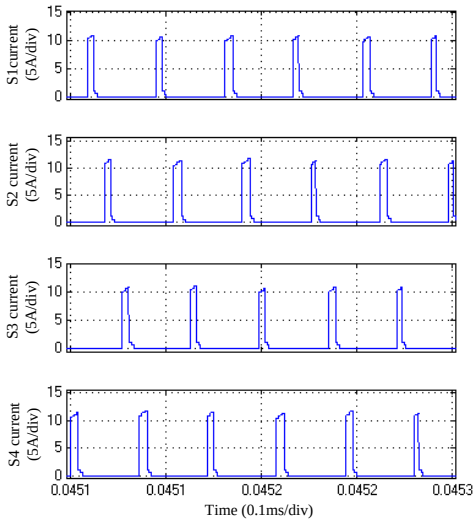

Fig.15 Waveforms of power devices S11, S12, S21 and S22

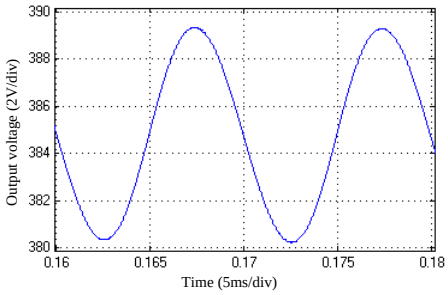

Fig.16 Waveform of DC output voltage

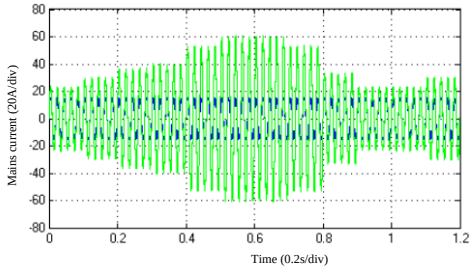

Fig.17 Waveforms of mail voltage and mains current under varying load

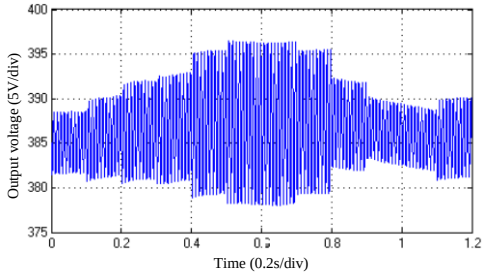

Fig.18 Waveform of DC output voltage under varying load

Also from the simulated results, with the premise of the steady system, to increase appropriate injection damping, the THD of mains current can be reduced, and the rising time of output voltage can also decline.

2x2 APFC can make the design of boost inductor easier and the total input current ripple lower. But for a practical APFC system, the currents of boost inductors are likely to be unbalanced, due to different device parameters and line impedances. The APFC will malfunction when the situation becomes more serious.

In order to expose the robustness of passivity control method for 2x2 APFC, some of the major parameters are changed. Take the boost inductors for instance, their inductances deviate at 20% of the rated inductance, i.e. L1 is 0.8mH, and L2 is 1.2mH.

Fig.19 shows the waveforms of inductor currents and their synthesized current for the 2x2 APFC. Intuitively, the two inductor currents are basically consistent in view of form and amplitude, and the average values in every switching period are identical. The ripple of synthesized current behind the diode rectifier is reduced dramatically, which lowers the difficulty of design of the inductor. Obviously, passivity control methods can bring about satisfactory effect on current sharing. Though the inductor with larger inductance can lead to lower peak to peak ripple, they deliveries the same energy in any switching period.

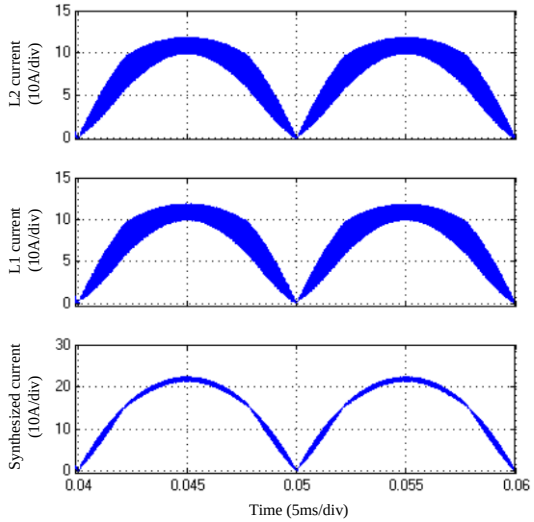

Fig.19 Waveforms of individual inductor current and total inductor current (when different inductance)

4.2 Experimental research

Experimental parameters and conditions are

stated as follows: the input is single-phase AC sinusoidal voltage, the desired output voltage is 385V, the rated load is 3.5kW, and the estimated overall efficiency is 95%,

As a consequence, the maximum RMS value of fundamental mains current is 16.75A, i.e. its peak value is 23.68A. DSP TMS320F28335 is selected as the kernel controller, and the switching frequency is 25kHz. The two inductors is made of magnetic material FeSiAl in the form of 2 in 1, and their inductances are 0.35mH under rated load and rated switching frequency. The AC capacitor is 2.2μF.

The electrolysis capacitor is 5x680μF/450V, IGTB is IKW50N60H3: 50A/100°C/600V, buried with FWD. FRD is FFAF60UA60DN: 2x30A/45°C/600V. The diode rectifier is D50XB80. The driver of IGBT is TPS2812, powered by +15V single channel power supply.

Eventually the whole 2x2 APFC platform with passivity control is implemented after repeated experiments, including hardware design and software completion. The overall efficiency is not less than 0.98 under light load and higher than 0.98 under rated load.

The mains current is almost perfect with only small ripple, and the average output DC voltage is 385V under light load and 385V with only 10V peak to peak ripple under rated load.

Fig.20 shows the waveforms of mains current of 11.4A RMS value and one of the two driving pulse train for the 2x2 APFC. Fig.21 shows the waveforms of mains voltage and current of 8.69A RMS value and its current spectrum for the 2x2 APFC. Fig.22 shows the waveforms of mains voltage, mains current and relevant data for the 2x2 APFC, when the output power is 3.83kW. Evidently, 2x2 APFC has a better correction results.

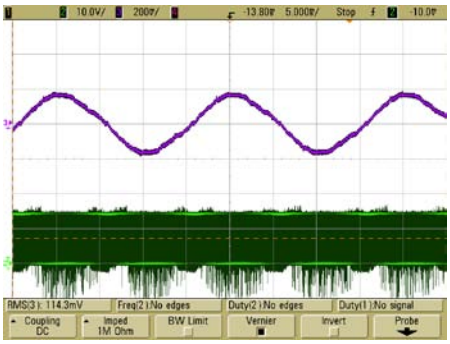

Fig.20 Waveforms of mains current and driving pulse

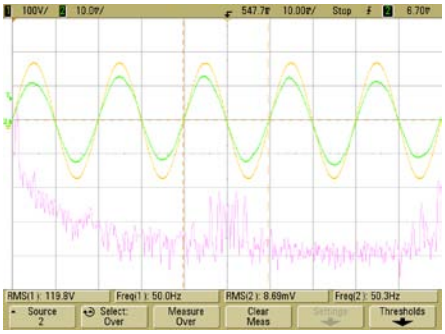

Fig.21 Measured waveforms of mains voltage and mains current

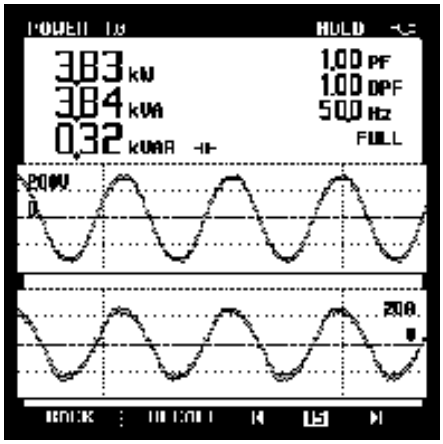

Fig.22 Measured waveforms of mains voltage and mains current

5 Conclusion

In the paper, a M-channel interleaved N-power device paralleling APFC (MxN APFC) is researched, and the phase-shift operation theory is described, including voltage transfer ratio, driving method and control method, which either can help to lower switching frequency of power device and keep unchanged that of boost inductor at the same time, or can help to keep unchanged switching frequency of power device and lower the that of boost inductor at the same time. MxN APFC can solve the IGBT's current sharing when connected in parallel, which can meet the requirements for high power applications.

The EL mathematical model of 2x2 APFC is established, and passivity power controller is designed using damping injection method. The simulation of 2x2 APFC by MATLAB/ SIMULINK is built up, and the 2x2 APFC is proved using F28335, showing the validity of the entire scheme. Passivity control strategy is characteristic of quick response of inductor current and track capability of output voltage. Dynamic

response is fast under the circumstance of fluctuated load. The average output voltage is reluctant to vary, and the mains current keeps in good sinusoidal waveform. Due to direct current control, each channel APFC still undertakes the same delivered power, showing a good current sharing.

Using phase-shift driving and passivity control strategy can simplify the design of 2x2 APFC to a degree, and the overcome the demerits of existing APFC's control strategies.

References

[1] IEC61000-3-2: 1995. Electromagnetic compatibility Part3: limits-set.2: limits for harmonic current emission (equipment input current≤16A per phase) [M].

[2] IEC61000-3-12: 2005. Electromagnetic compatibility (EMC) Part3-2: limits-limits for harmonic currents produced by equipment connected to public low-voltage systems with input current > 16 A and ≤75 A per phase [M].

[3] Thomas Nussbaumer, Johann W. Kolar. Design Guidelines for Interleaved Single-Phase Boost PFC Circuits [J]. IEEE Trans, power electron, vol.56, no.7, pp. 2559-2573, July 2009.

[4] Vinaya Skanada, Anusheel Nahar. Interleaved Power Factor Correction (IPFC) Using the dsPIC DSC[J] Microchip Technology Inc, 2009.

[5] José R. Pinheiro, Hilton A. Gründling, Dalton L. R. Vidor and José E Baggio. Control Strategy of an Interleaved Boost Power Factor Correction Converter[J]. Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE, pp. 137-42.

[6] Jin-song Zhu, Annabelle Pratt. Capacitor Ripple Current in an Interleaved PFC Converter [J]. IEEE Power Electronics Specialists Conference, 2008, pp.3444-3450.

[7] Pit-Leong Wong and Fred C. Lee. Interleaving to Reduce Reverse Recovery Loss in Power Factor Correction Circuits [J]. Industry Applications Conference, 2000. Conference Record of the 2000 IEEE, pp. 2311-2316.

[8] Fei Zhang, Jianping Xu. A Novel PCCM Boost PFC Converter With Fast Dynamic Response[C]. Industrial Electronics, IEEE Transactions on 2011, volume: 58 issue: 9, pages: 4207-4216.

[9] Bor-Ren Lin and Hsin-Hung Lu. Single-phase Three-Level PWM Rectifier. IEEE 1999 International Conference on Power Electronics and Drive System, PEDS'99, July 1999, Hong Kong.

[10] Michael T. Zhang et al, Single phase three-level boost power factor correct converter [C].Proc. IEEE APEC'95：434-439.

[11] José R. Pinheiro, Hilton A. Gründling, Dalton L. R. Vidor and José E Baggio. Control Strategy of an Interleaved BOOST Power Factor Correction Converter [J]. Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE, pp. 137-142.

[12] R. W. Erickson and D. Maksimovic. Fundamentals of Power Electronics [M]. 2nd ed. New York: Springer Verlag, 2000.

[13] Thomas Nussbaumer, Johann W. Kolar. Design Guidelines for Interleaved Single-Phase Boost PFC Circuits [J]. IEEE Trans. on power electron, vol.56, no.7, pp. 2559 – 2573, July 2009.

[14] Wang Jiu-he, Li Hua-de, Wang Li-ming. Direct power control system of three phase boost type PWM rectifiers[J].Proceedings of the CSEE, 2006, 26(18)：54-60(in Chinese).

[15] Qiao Shu-tong, Jiang Jian-guo. Output error passivity control of three-phase boost-type PWM rectifiers[J].Transactions of China Electro-technical Society, 2007, 22(2): 68-73(in Chinese).

[16] Sira-Ramirez H, Perez-Moreno R A, Otega R, et al. Passivity-based controllers for the stabilization of DC to DC power converters [J]. Automatica, 1997, 33(4): 499-513.

[17] Qiao Shu-tong,Wu Xiao-jie, Jiang Jian-guo. Application of Passivity based Sliding Mode Control in DC/ DC Converters [J]. Transactions of China Electro-technical Society, 2003, 18(4): 41-45 (in Chinese).

[18] Wu Lei-tao, Yang Zhao-hua, Xu Bu-gong. Investigation of Passivity-Based Control of DC/DC Converter.[J]. Transactions of China Electro-technical Society, 2004, 19(4): 66-69 (in Chinese).

[19] Xue Hua, Jiang Jian-guo. Study on adaptive passivity-based control strategies of shunt active filters[J].Proceedings of the CSEE, 2007, 27(25): 114-118(in Chinese).

[20] Zhang Zhen-huan, Liu Huijin, Li Qiong-lin, et al.A novel passivity based control algorithm for single-phase active power filter using Euler-Lagrange model[J].Proceedings of the CSEE,2008,28(9): 37-44 (in Chinese).

[21] Wang Jiu-he. Passivity-based control theory and its application[M]. Beijing: Publishing House of Electronics Industry, Nov. 2010 (in Chinese).