New Models of a Z-Source Inverter Built of Standard MATLAB-Simulink Blocks

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Abstract: In this paper, two new simulation models of a Z-Source inverter (ZSI) system are proposed. These models have been built only out of standard MATLAB-Simulink blocks. The proposed models have been developed using two sets of differential equations – for the non-shoot-through and shoot-through states – which are alternately executed, depending on the ZSI state. In the first model, this is done by alternately triggering two separate subsystems, each corresponding to one of the ZSI states. In contrast, in the second model, both ZSI states are programmed by using the same Simulink blocks, contained within a single unified subsystem; the interaction between the blocks is, however, altered based on the same trigger signal. For comparison, another model of the ZSI system has been developed in additional MATLAB SimPowerSystems toolbox. Results for various types of loads for all three models have been compared and discussed.

Key-Words: Impedance-Source inverters, Z-Source inverter, Modulation techniques, Maximum constant boost control, MATLAB-Simulink, SimPowerSystems

1 Introduction

In recent years, there has been a rapid development of the various topologies of the impedance-source inverter and their control methods [1], [2]. The Z-source inverter (ZSI) [3], belonging to this group, offers the opportunity to both buck and boost the voltage supplied to the inverter bridge, without the additional power switches. The special Z-network, consisting of two capacitors and two inductors connected in a unique way to the inverter bridge, provides these possibilities. Boost capabilities are enabled by the advantageous usage of the shoot-through (ST) state which is achieved by gating on both the upper and lower switches of one or more inverter phase legs. Moreover, the danger from the electromagnetic interference (EMI) noise misgating on both inverter leg switches is not present because this state is not forbidden during normal operation of the ZSI.

After the first design has been proposed in [3], various ZSI topologies have emerged [1], such as quasi Z-source inverter [4], [5]. Also, a number of modulation control techniques for the ZSI have been proposed in recent years [2], such as the maximum constant boost control (MCBC) [6], [7], the maximum boost control [8], and the modified space vector PWM control [9]. MCBC method has lower voltage stress [7] and greater maximum voltage boost in comparison with the simple boost control, and it also provides constant boost unlike the maximum boost control. In this paper, the conventional ZSI topology [3] is analyzed, with the maximum constant boost method including third harmonic injection [7] used for the control of the ST state.

In [10] and [11], various models of electrical machinery and drives developed using only standard Simulink blocks were presented. The motivation for and benefits of the development of ZSI models using only standard Simulink blocks despite the existing SimPowerSystems (SPS) toolbox are numerous

- greater control over the model
- the SPS toolbox represents an extra purchase in addition to the basic MATLAB
- SPS is a closed environment – it cannot be combined with models (e.g., electrical machine, photovoltaic cell, fuel cell) developed outside of SPS nor can the constituent components be upgraded to more advanced versions

In [3]-[9], simulations of the ZSI system were performed, but the models have not been clearly explained in terms of the software used for simulation and interior design. To the best of authors' knowledge, in this paper, detailed and clearly explained model of the ZSI system built

exclusively out of standard MATLAB-Simulink blocks is proposed for the first time. The two models of the ZSI, explained in sections 3.1.1 and 3.1.2, are developed based on the differential equations of the system, presented in the next section. Moreover, for comparison, a model of the ZSI system has been constructed using the additional SPS toolbox in MATLAB-Simulink. All three models were tested for different types of load and their results are compared in section 4.

2 Z-Source Inverter System

The basic configuration of the analyzed system is shown in Fig. 1. DC battery source feeding the ZSI is connected to the three-phase inverter bridge supplying a three-phase passive RL load.

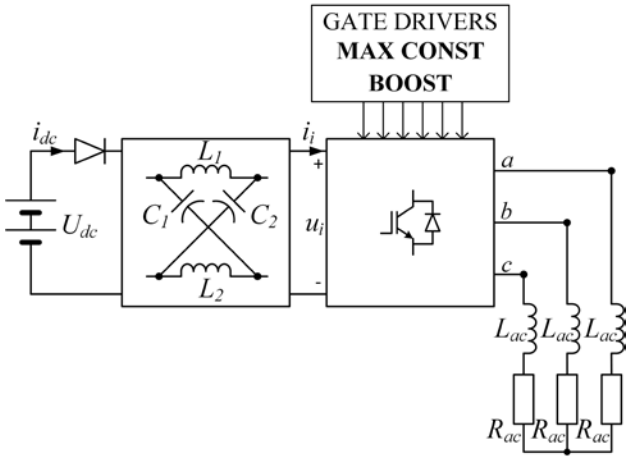


Fig. 1 Basic configuration of the ZSI system.

The diode connected in series to the DC source ensures that the source is disconnected from the Z-network when the system is in the ST state. The ST state is achieved when both the upper and lower switches in the same phase leg are gated on. The modulation method used for controlling the ST state is MCBC [6], [7]. The *Gate drivers* block consists of the circuitry responsible for producing the gate signals for the switches. These signals are formed by integrating the ST states into the sinusoidal pulse-width modulation (SPWM) signals with injected third harmonic (1/6 of the fundamental component amplitude), according to the MCBC method [7].

The boost factor B and the voltage gain G can be calculated as follows:

$$B = \frac{1}{1-2\frac{T_0}{T}} = \frac{1}{1-2D_0} \tag{1}$$

$$G = \frac{\hat{U}_{ac}}{U_{dc}/2} = M \cdot B \tag{2}$$

where: T_0 – ST state period
T – switching period
M – modulation index
$\hat{U}_{ac}$ - maximum value of the fundamental harmonic of the inverter output phase voltage
U_{dc} – DC source voltage
D_0 – shoot-through duty ratio.

The ratio between the average values of the capacitor and the DC source voltages over one switching period T is given by

$$U_C = \frac{1-D_0}{1-2D_0} U_{dc} \tag{3}$$

With the MCBC method implemented, the shoot-through duty ratio D_0 is given as a function of the modulation index M [7]

$$D_0 = 1 - \frac{\sqrt{3}}{2} M \tag{4}$$

From (4), and using (1) and (2), B and G can be determined as a function of M

$$B = \frac{1}{\sqrt{3}M - 1} \tag{5}$$

$$G = \frac{M}{\sqrt{3}M - 1} \tag{6}$$

From (2) and (6), with $\hat{U}_{ac} = \sqrt{2}U^*_{ac}$ for sinusoidal voltages, the modulation index is calculated as a function of the DC source voltage U_{dc} and the desired RMS value of the fundamental harmonic of the phase voltage across the load terminals U^*_{ac}

$$M = \frac{2\sqrt{2}U^*_{ac}}{2\sqrt{6}U^*_{ac} - U_{dc}} \tag{7}$$

With a given T, and using M from (7), the shoot-through duty ratio D_0, and subsequently the ST state period T_0, can be calculated using (4). This is necessary data for the gate drivers in order for the MCBC method to be implemented in the proposed manner.

The *non-shoot-through* (Non-ST) state is illustrated in Fig. 2. In this state, the input diode is forward biased, and the DC source is coupled with the inverter, which can be modelled as an equivalent current source. The capacitors in the Z-network are being charged from the DC source, while the inductors act as an additional current source, boosting the inverter DC side voltage u_i.

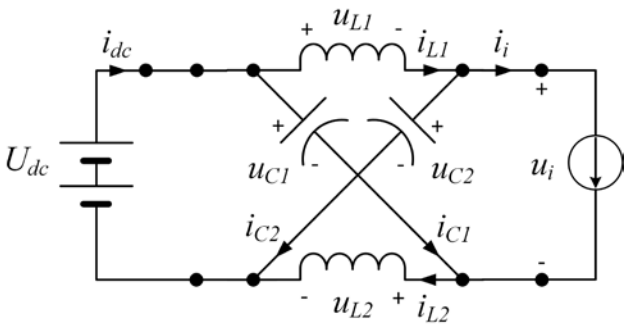


Fig. 2 Equivalent circuit of the ZSI during the Non-ST state.

The capacitor current i_{C1} and the inductor voltage u_{L2} can be described by the following differential equations:

$$i_{C1} = C_1 \frac{du_{C1}}{dt} = i_{L2} - i_i \tag{8}$$

$$u_{L2} = L_2 \frac{di_{L2}}{dt} = U_{dc} - u_{C1} \tag{9}$$

Equations (8) and (9) are transformed into integral form, which is more appropriate for model development in Simulink

$$u_{C1} = \frac{1}{C_1}\int_0^t (i_{L2} - i_i)dt + u_{C1}(0) \tag{10}$$

$$i_{L2} = \frac{1}{L_2}\int_0^t (U_{dc} - u_{C1})dt + i_{L2}(0) \tag{11}$$

Similarly to (10) and (11), we have

$$u_{C2} = \frac{1}{C_2}\int_0^t (i_{L1} - i_i)dt + u_{C2}(0) \tag{12}$$

$$i_{L1} = \frac{1}{L_1}\int_0^t (U_{dc} - u_{C2})dt + i_{L1}(0) \tag{13}$$

The inverter DC-side voltage in the Non-ST state is given below

$$u_i = u_{C1} - u_{L1} = u_{C2} - u_{L2} \tag{14}$$

Because the voltage over the inductors L_1 and L_2 is actually negative during this period, u_i becomes greater than the capacitor voltage u_{C1} (u_{C2}). With (10) – (14), the Z-network is completely described in the Non-ST state.

When the ZSI is in the *shoot-through* state, it is equivalent to a circuit shown in Fig. 3, so the inverter DC side voltage u_i is zero during that period. The input diode becomes reverse biased and disconnects the DC source from the Z-network.

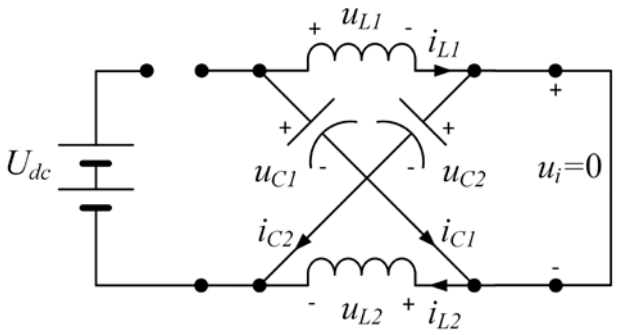


Fig. 3 Equivalent circuit of the ZSI during the ST state.

The capacitors C_1 and C_2 in the Z-network transfer the energy received during the Non-ST period over to the inductors L_1 and L_2, respectively. That means that the current through the capacitors has changed direction. This change of direction is described by the following term:

$$i_{C1} = C_1 \frac{du_{C1}}{dt} = -i_{L1} \tag{15}$$

Because of $u_i = 0$, the voltage over the inductor L_1 is

$$u_{L1} = L_1 \frac{di_{L1}}{dt} = u_{C1} \tag{16}$$

Equations (15) and (16) are transformed into integral form

$$u_{C1} = -\frac{1}{C_1}\int_0^t i_{L1}dt + u_{C1}(0) \tag{17}$$

$$i_{L1} = \frac{1}{L_1}\int_0^t u_{C1}dt + i_{L1}(0) \tag{18}$$

Similarly to (17) and (18), we have

$$u_{C2} = -\frac{1}{C_2}\int_0^t i_{L2}dt + u_{C2}(0) \tag{19}$$

$$i_{L2} = \frac{1}{L_2}\int_0^t u_{C2}dt + i_{L2}(0) \tag{20}$$

Equations (14) and (17) – (20) completely describe the Z-network during the ST state.

The inverter bridge is modelled with ideal switches, and its voltage equations are as follows [12]:

$$u_a = \frac{u_i}{3}(2S_a - S_b - S_c) \tag{21}$$

$$u_b = \frac{u_i}{3}(2S_b - S_a - S_c) \tag{22}$$

$$u_c = \frac{u_i}{3}(2S_c - S_a - S_b) \tag{23}$$

where: u_a, u_b, u_c – load phase voltages
S_a, S_b, S_c – inverter switching signals.

The inverter input current i_i during the Non-ST state can be derived from the inverter output phase currents and switching signals. Combined with (8), a single expression encompassing both the Non-ST state (i_i') and the ST state (i_i'') is obtained

$$\begin{aligned} i_i &= (i_a \cdot S_a + i_b \cdot S_b + i_c \cdot S_c)\cdot \overline{ST} + \\ &+ (i_{L2} - i_{C1})\cdot ST \\ &= i_i' \cdot \overline{ST} + i_i'' \cdot ST \end{aligned} \tag{24}$$

where ST and $\overline{ST}$ are logical signals enabled in the ST state and Non-ST state, respectively.

Similarly, an expression for the inverter input voltage u_i encompassing both ZSI states can be formed as follows:

$$u_i = (u_{C1} - u_{L1})\cdot \overline{ST} + 0 \cdot ST \tag{25}$$

Note that (24) and (25) hold true when i_{C1} and i_{L2} are replaced with i_{C2} and i_{L1}, or u_{C1} and u_{L1} with u_{C2} and u_{L2}, respectively.

3 Models of the Z-Source inverter in MATLAB

3.1 Models with basic Simulink elements

The two proposed models have been derived based on the equations given in the previous section. The configuration of the proposed models is shown in Fig. 4. It consists of six blocks: *DC SOURCE*, *SPWM*, *MCB PWM*, *Z-SOURCE*, *INVERTER* and *3ph RL LOAD*.

The *DC SOURCE* block is represented by a constant, and five other blocks are actually subsystems. The *SPWM* subsystem represents SPWM pulses generation with integrated third harmonic injection, while the *MCB PWM* subsystem injects ST states into the gate pulses according to the MCBC method. The Z-network is represented by the *Z-SOURCE* subsystem which is discussed later on. The *INVERTER* subsystem represents the three-phase inverter bridge with ideal switches. The *3ph RL LOAD* subsystem represents the three-phase passive RL load and is based on models from [13].

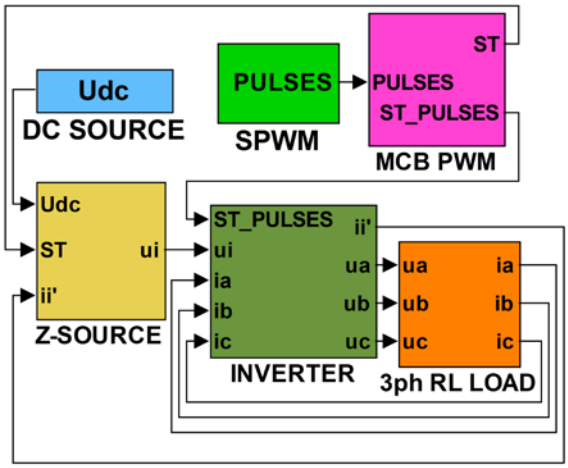


Fig. 4 Proposed model of the ZSI system in Simulink.

The interior of the *MCB PWM* subsystem is shown in Fig. 5. With the presented combination of the logical blocks, the reset input of the *N-Sample Switch* block is true only during the zero states occurring in the traditional carrier-based PWM, i.e., while the upper three or the lower three switches of the inverter are turned on simultaneously. In that case, the *N-Sample Switch* block changes all pulses to high level (ST state), but only for a fixed amount of time samples N_0 ($N_0T \approx T_0/2$). Therefore, N_0 is calculated by using the MATLAB *round* function as follows:

$$N_0 = round\left(\frac{T_0}{2T}\right) \quad (26)$$

The *ST_PULSES* signal combines the output of the *N-Sample Switch* block with the SPWM pulses into the resulting gate pulses according to the MCBC method. The *Rate Transition* blocks are implemented in order to obtain the possibility to run the models with different sampling frequencies for the gate driver pulses and rest of the model, respectively.

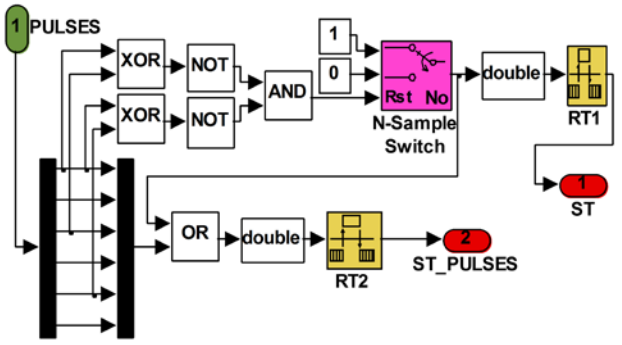


Fig. 5 Inside of the MCB PWM subsystem.

The proposed models differ only with respect to the *Z-SOURCE* subsystem. In one of the models, further referred to as "Two-Block" model, the Non-ST and ST states are programmed within the *Z-SOURCE* subsystem by means of two additional separate subsystems; in the other model, further referred to as "One-Block" model, both states are programmed within a single subsystem, as explained in the following subsections.

3.1.1 "Two-Block" model

The interior of the *Z-SOURCE* subsystem for the "Two-Block" model is shown in Fig. 6. It consists of two main parts – blocks *Non-ST* and *S-T*, which represent the Z-network during the Non-ST and ST states, respectively. The *ST* signal is 1 when the ZSI is in the ST state, thus enabling the *S-T* block, whereas it is 0 when the ZSI is in the Non-ST state, thus enabling the *Non-ST* block. The same signal is also used for calculation of both the *ui* voltage output signal and the *ii* current signal according to (24) and (25), respectively. The *Unit Delay* block before the *ui* output is in this case mandatory in order to avoid entering an unsolvable algebraic loop. Consequently, the model requires to be run at high sampling frequencies (several hundred kHz) in order to provide accurate results.

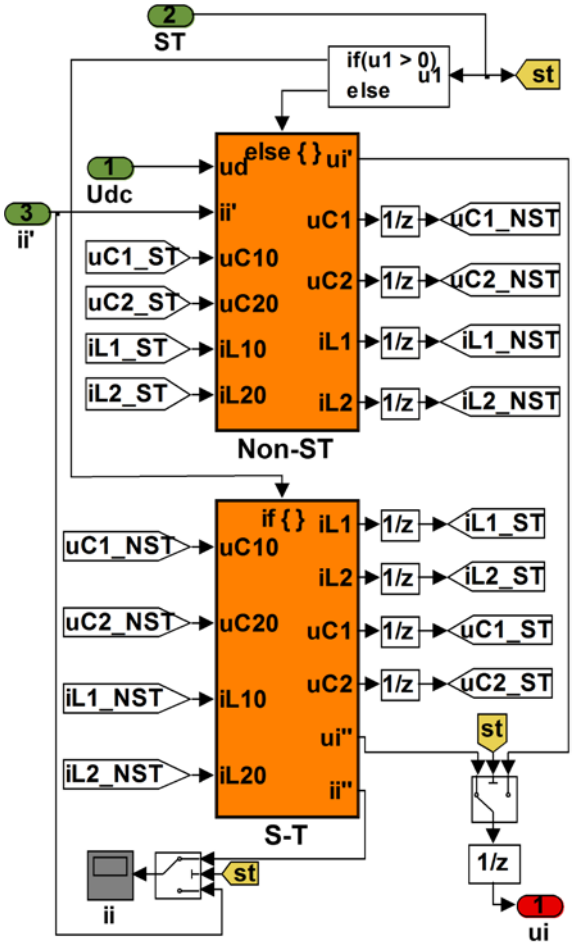


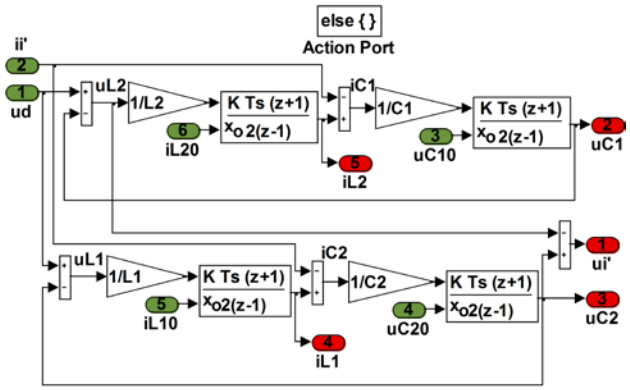
Fig. 6 Inside of the Z-SOURCE subsystem.

The two switches in Fig. 6, controlled by the *ST* signal, are set to pass input 1 when the *ST* signal is greater than 0, or pass input 3 otherwise.

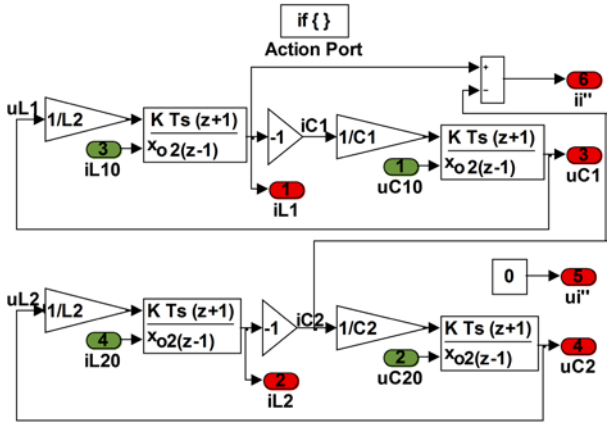
The main blocks – *Non-ST* and *S-T* – are mutually coupled by their capacitor voltage and inductor current values from the previous integration step. This is because discontinuities in capacitor voltages and inductor currents cannot be allowed. Those signals are each taken through the respective *Unit Delay* block and connected to the input of the block for the opposite state.

Fig. 7 shows the interiors of the *Non-ST* block (7a) and the *S-T* block (7b). It is important to point out that the action blocks in Fig. 7 are set to reset value after each integration step in order to avoid the accumulation of previous values of u_C and i_L.

The subsystem in Fig. 7a was derived based on (10) – (13), whereas the subsystem in Fig. 7b was derived based on (17) – (20). The *Discrete Integrator* blocks in both Fig. 7a and 7b are all set to trapezoidal integration type because it is arguably the most accurate method of all the available discrete integration methods in Simulink.



a)



b)

Fig. 7 Inside of the Non-ST (a) and S-T (b) blocks.

3.1.2 "One-Block" model

The "One-Block" model is based on the same equations as the "Two-Block" model. The only difference is the internal design of the *Z-SOURCE* subsystem, which is presented in Fig. 8.

The *inv* signal, colored orange in Fig. 8, is responsible for inverting the sign of the capacitor voltages and currents based on the state of the ZSI, hence the name *inv*. When the ZSI is in the ST state, the *inv* signal becomes -1, which causes the mentioned change of sign, thus performing the switch from (10) – (13) to (17) – (20). In this way, use of the same blocks representing two different sets of equations is enabled. Because of this, the "One-Block" model does not need *Unit Delay* blocks, which allows it to work accurately with much lower sampling frequencies than the "Two-Block" model, but at the cost of inability to model asymmetrical Z-networks. Namely, the same parameters are used in different equations between the Non-ST and ST states.

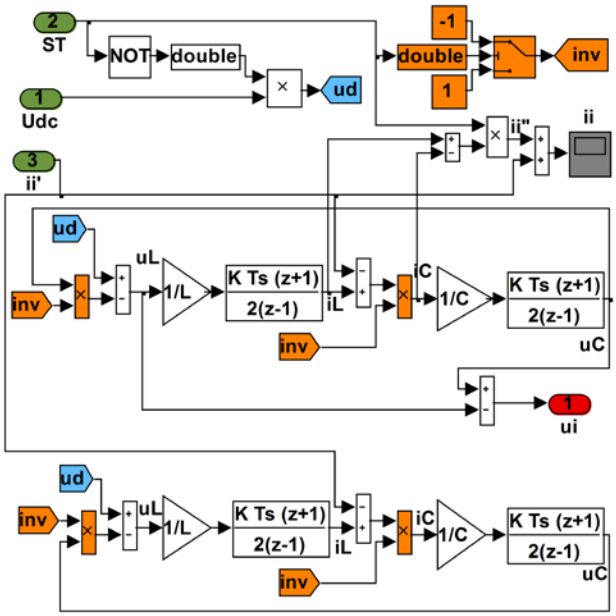


Fig. 8 Inside of the Z-SOURCE subsystem for the "One-Block" model.

The *ud* signal simulates the reverse-biasing of the input diode and decoupling of the DC source during the ST period; it is equal to U_{dc} only during the Non-ST period, otherwise it is zero (i.e., equal to u_i). The switch in Fig. 8 controlled by the *ST* signal is set to pass input 1 when the *ST* signal is greater than 0, or pass input 3 otherwise. This model demands the capacitors and the inductors to be symmetrical ($C_1 = C_2 = C$ and $L_1 = L_2 = L$), because they switch equations depending on the ZSI state.

3.2 SimPowerSystems model

The model of the ZSI system developed by using the SPS toolbox in Simulink is presented in Fig. 9. The model consists of the same elements that comprise the physical setup of the ZSI: a DC source, a diode, two capacitors, two inductors, an inverter, a three-phase RL load, and gate driver pulses. These are all available as separate blocks in the SPS library apart from the *SPWM* and *MCB PWM* subsystems, which are the same as in the other two models (Fig. 4).

The main advantage of this model is in the ease of assembling the whole model out of known building blocks from the supported library. Indeed, the model of the system in Fig. 9 retains the appearance of the basic system configuration in Fig. 1. One of the advantages over the "Two-Block" model is that it does not require *Unit Delay* blocks, hence it provides accurate results at much lower sampling frequencies, but this advantage is shared with the "One-Block" model.

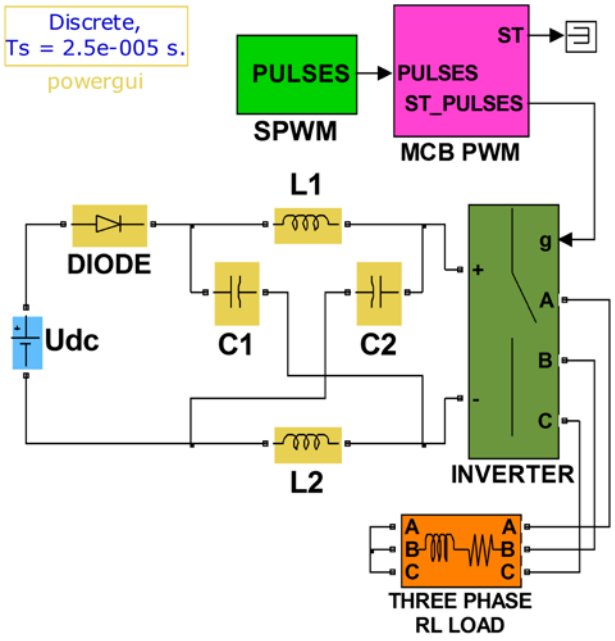


Fig. 9 Model of the ZSI system in SPS.

Furthermore, the SPS model, unlike the "One-Block" model, allows for the asymmetry in Z-network capacitance and inductance values. This advantage is shared with the "Two-Block" model.

The disadvantages of this model are the inability to be combined with models developed outside of the SPS or to upgrade its constituent components to more advanced versions. Furthermore, a snubber resistor has to be present in the *INVERTER* block regardless of the type of the semiconductor switches used. However, inappropriate choice of the snubber parameters may largely affect the results, as discussed later.

4 Results and Discussion

The inductance of the Z-network inductors has been set to 17 mH, and the capacitance of the Z-network capacitors has been calculated according to the following expression [14]:

$$C \geq \frac{D_0 I_L}{2 f_{sw} \Delta U_C} \tag{27}$$

where: I_L, U_C – average values of inductor current and capacitor voltage, respectively
f_{sw} – switching frequency of the inverter
ΔU_C – desired capacitor voltage ripple.

The capacitance has been set to 80 μF in order to obtain the capacitor voltage with less than 5 % ripple. The DC source voltage U_{dc} has been set to 50 V, and the desired RMS value of the fundamental harmonic of the phase voltage U_{ac}^* has been set to 36 V, which provides satisfactory accuracy given that N_0 has to be rounded to the integer multiple of the sample time T = 25 μs, as in (26). M and D_0 were calculated from (4) and (7), respectively, leading to N_0 = 3.

The models have been tested with three types of load with the following power factors at 50 Hz: 1, 0.85 and 0.63. Parameters for these loads are as follows: *R load* (R_{ac} = 22 Ω, L_{ac} = 0 mH), *RL1 load* (R_{ac} = 9.22 Ω, L_{ac} = 18 mH), and *RL2 load* (R_{ac} = 9.22 Ω, L_{ac} = 36 mH).

In this paper, the sampling frequency of both the SPS and "One-Block" models was set to 40 kHz. For the "Two-Block" model, due to the *Unit Delay* block before the *ui* output (Fig. 6), gate driver pulses were run at the sampling frequency 40 kHz, while the sampling frequency of the rest of the model was set to 1 MHz.

Simulation results from all three models are shown in Table 1. The recorded values of U_C and I_L have been averaged with the 1/20 s averaging period. The simulation stop time was set to 0.2 s, which is sufficiently long for the ZSI to enter a steady state. For the SPS model, the overall average execution time was 0.6334 s, whereas for the "One-Block" model it was 1.0845 s, and for the "Two-Block" model 9.3552 s.

Table 1 Comparison of the simulation results for all models (U_{dc} = 50 V, U_{ac}^* = 36 V).

		SPS	Two-Block	One-Block
R load	U_{ac} [V]	36.29	35.79	36.17
	U_C [V]	87.23	86.77	87.27
	I_L [A]	6.431	6.321	6.428
RL1 load	U_{ac} [V]	36.46	35.79	36.13
	U_C [V]	87.27	86.82	87.30
	I_L [A]	6.237	6.142	6.277
RL2 load	U_{ac} [V]	36.57	35.76	35.93
	U_C [V]	87.35	86.87	87.37
	I_L [A]	3.431	3.375	3.451

As can be seen in Table 1, both proposed models closely match the results of the SPS model for all tested loads. It can also be noted that the "One-Block" model has shown even better match in results than the "Two-Block" model, presumably because of lack of the *Unit Delay* blocks in the "One-Block" model.

The most prominent advantage of the "Two-Block" model over the "One-Block" model is the ability to implement asymmetric Z-network elements. This feature has been tested with the ZSI

loaded with the *R load* and using the following parameters: L_1 = 0.8 · 17 mH, L_2 = 1.2 · 17 mH, C_1 = 1.2 · 80 μF, C_2 = 0.8 · 17 μF. These values were chosen as the worst case scenario that could happen in real Z-network, based on the tolerances of some inductor and capacitor manufacturers. Simulation results obtained by testing the asymmetry with the mentioned parameters are presented in Fig. 10.

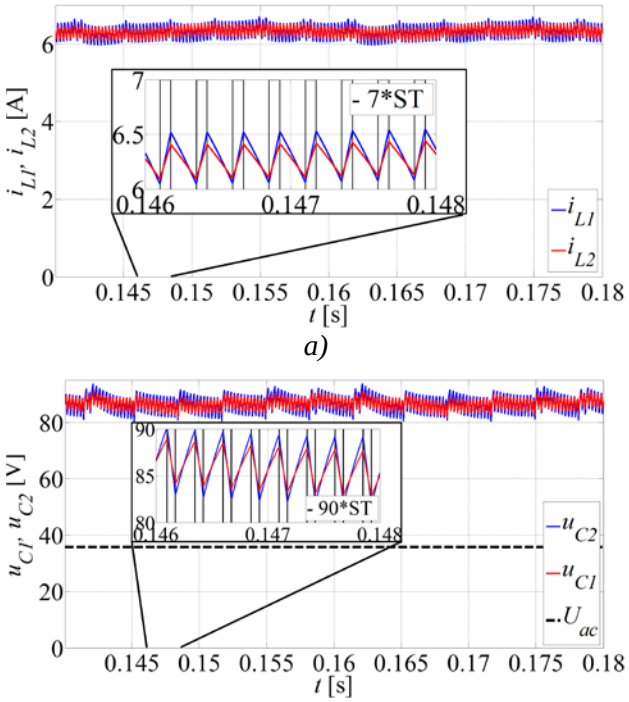


Fig. 10 Simulation waveforms achieved with the "Two-Block" model illustrating asymmetry in inductor currents (a) and capacitor voltages (b).

In Fig. 10a, it can be seen that the maximum difference between i_{L1} and i_{L2} is 0.15 A at any given moment. Also, from Fig. 10b, it can be observed that the maximum difference between u_{C1} and u_{C2} is approximately 2 V (less than 3 % of U_C). In magnified parts of the Fig. 10, the *ST* signal has been multiplied by 7 and 90, respectively, in order to be comparable to the recorded signals. In this way, it is visible when the ZSI switches states. Since the ZSI is evidently robust to tested asymmetries and given the previously mentioned advantages of the "One-Block" model, it can be concluded that the ability to simulate asymmetry between components of the Z-network is not enough to validate further use of the "Two-Block" model. With that in mind, further analysis has been conducted using the "One-Block" model.

Simulation results for the "One-Block" model tested with *RL2 load* are shown in Fig. 11.

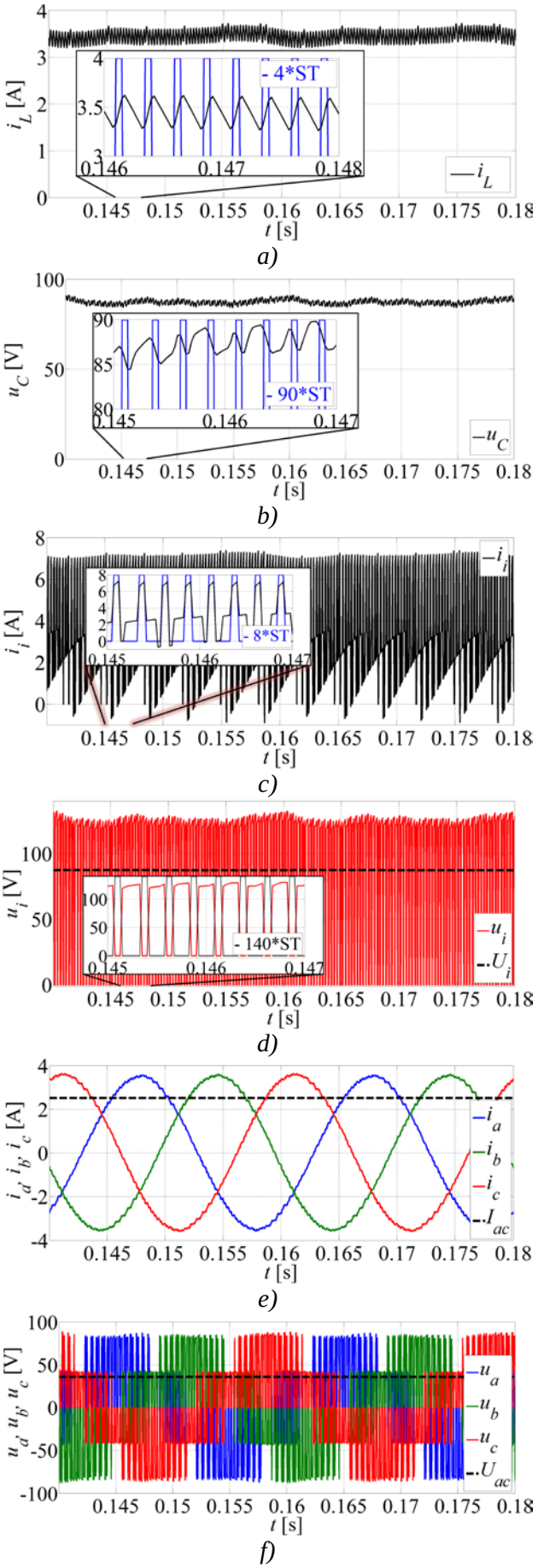


Fig. 11 Simulation results for the proposed model.

Inductor current is shown in Fig. 11a, with the zoomed in portion of the same signal shown alongside the *ST* signal. There, the process of magnetizing the inductor can be observed as the inductor current increases during the ST period. The opposite action happens for the capacitor voltage u_C – it decreases during the ST period, as shown in Fig. 11b. In Fig. 11c, the inverter DC side current i_i is shown. It can easily be observed that it is changing between $i_i^{'}$ and $i_i^{''}$, depending on the ST state, as described by (24). Fig. 11d shows the inverter DC side voltage u_i and its average value U_i, which corresponds to the average value of U_C, presented in Table 1. In magnified parts of the Figs 11a – 11d, the *ST* signal has been multiplied by 4, 90, 8 and 140, respectively, for the reasons explained earlier. In Figs 11e and 11f, three-phase load currents and voltages are shown, respectively, alongside the respective RMS values of the fundamental harmonic, denoted by dashed lines. This demonstrates that the proposed models correctly describe the ZSI system.

For the considered ZSI system, the SPS inverter model does not allow the elimination of the snubber. Although the snubber capacitance was set to *inf*, the same could not be applied for the snubber resistance. Setting the snubber resistance to a value lower than 10^4 Ω lead to overestimated values of the inductor current, whereas with values higher than 10^9 Ω, the simulation would not start. Consequently, the default value of 10^5 Ω was chosen. In addition, running the SPS model in Simulink multitasking mode produced results that are not physically meaningful.

5 Conclusion

In this paper two novel and simple models of the ZSI system have been successfully developed using only basic Simulink libraries. Based on the simulation results, it can be concluded that the proposed models closely match the results of the SPS model for all tested loads.

The "Two-Block", unlike the "One-Block" model, allows simulation of an asymmetrical Z-network. However, the ZSI was proven robust to such asymmetries. Faster performance and the ability of the "One-Block" model to provide accurate results at lower sampling frequencies makes it a better choice of the two proposed models.

The proposed models offer several important advantages over the SPS model such as greater control over model, lower cost, and upgradeability. Moreover, it was noted that the SPS model, unlike the proposed models, does not provide physically plausible results in the Simulink multitasking mode, and also mandates the implementation of a snubber. On the other hand, the SPS model has the advantage in accuracy when simulating the ZSI system supplying loads with power factor lower than 0.5 (although a very small percentage of actual loads fall into this group). This is because the input diode has been modelled as a mechanical switch in the proposed models so the input current is allowed to flow into the DC source, which is not the case in practice. This problem is the subject of the future research.

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