# Let Us Be Prepared in Defence against Counterfeit Integrated Circuits

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*Abstract:* - This paper deals with an important topic aimed at counterfeit electronic components and their detection. The preventive technical diagnostics methods for counterfeit components revealing before entering the assembly process are mentioned and described. There are discussed both nowadays common analytical methods and also methods containing counterfeit components revealing potential to be evaluated and applied. Some facts which may influence negatively the component evaluation result are also mentioned. Practical methods for semiconductor component genuineness evaluation are discussed and illustrated with examples based on our research activities in relation to cooperation with electronic devices assembly manufacturers. Those methods correspond with our current research laboratory equipment comprising analogue signature analyzer, electronic component oriented X-ray, fiber laser for component package decapsulation, scanning electron microscopy, confocal microscopy, polarization microscopy, Raman spectroscopy and Terahertz spectroscopy. The model case of counterfeit component discovery among spare parts and replaced parts in a company repairing measurement devices is given in the end of this paper.

*Key-Words:* - Counterfeit electronic component, Analogue Signature Analysis, pin print, I-V characteristics, X-ray inspection, delidding, decapsulation, laser ablation, final wet etching

## 1 Introduction

The electronic components genuineness threat has started a couple of years ago, and it is a nightmare for electronic assemblies until nowadays. There has elapsed a pretty long time period since the first occurrence detection of counterfeit components in application sensitive devices at the beginning of new millennium. The first shock has been step by step replaced with an increasing experience and with a joint effort of electronic components manufacturers and suppliers in the field of recognition and filtering methods [3].

The counterfeit electronic components represent basically a dual infringement aspect, a legal one and a technical specification one. The legal infringement aspect is important, nevertheless, less important than the technical specification and application aspect from the manufacturers´ point of view. The reason for such an opinion is quite understandable. The legal satisfaction is a time and money consuming long track run with an uncertain result. The application of the technical means and procedures of preventing counterfeit components entering the assembly process represents a more efficient and direct way how to keep the assembly process not to be infected by unreliable fakes. Many already experienced manufacturers prefer technical means and the fake components delivery write off to legal way of lost money compensation. Anyway such fake component delivery write off loss is much more modest than time and money losses in case of letting fake components penetrate the production process and start the legal compensation process only then.

## 2 Genuineness Evaluation Methods

The counterfeit components filtering methods are mostly based on a comparative analysis that means that a master authentic component features are used as a reference for a particular component evaluation. Various component attributes can serve as a reference characteristic feature. The evaluation or inspection methods are naturally related to those particular features [1].

Standard optical devices like magnifying lens or simple microscope belong to visual inspection methods aimed at electronic component basic optical features. These features are covering, for instance, by accompanying documentation, component design and appearance, component ink or laser marking which incorporates both the manufacturer's logo and the manufacturer's part number and also a manufacturing date code, component package material structure and homogeneity (blacktopping), component contact terminals condition, package imprints, terminal number one position marking, etc. It is necessary to have always either an original component manufacturer (OCM) documentation or the original component sample as a comparison reference specimen.

The visual inspection methods belong to the nondestructive group of evaluation methods. As other nondestructive evaluation methods, we can mention the Analog Signature Analysis (ASA) as a simplified parametric inspection method, X-Ray inspection of non-hermetic component internal structure, Raman spectroscopy, Terahertz spectroscopy, infrared spectroscopy, and any other physical method being able to reveal difference between the reference specimen and an inspected component [4].

The Analog Signature Analysis deserves a more detailed treatise. The ASA is a well known comparative method based on graphical representation of a current flowing between two nods in circuit which the alternating voltage waveform have been activated with. The modern hardware and software technologies have brushed up the ASA method that thanks to it could have been called to serve as an efficient means for counterfeit components tracing [2] [5]. The ASA based counterfeit IC detector was our first diagnostic tool when we started our counterfeit components prevention project about 6 years ago. As we also started immediately a learning cooperation with companies, we had a lucky opportunity to test our developing methods in the industrial field. We also had some possibilities to guest on X-ray equipment at the time we had no X-ray device in our research laboratory. Following figures are illustrating a tricky case of apparently counterfeited 4 bit microcontroller being reported as suspicious because of pin number 9 missing signal during the application module in-circuit test. That industrial field project has brought us about 3000 fakes for testing and learning. Such situations are very rare so that only a few fake components are a standard situation for authenticity evaluation. The analysis has to be well prepared then not a sample to be lost vainly. Even one suspicious sample can be processed efficiently to provide a wide range of interesting information and experience.

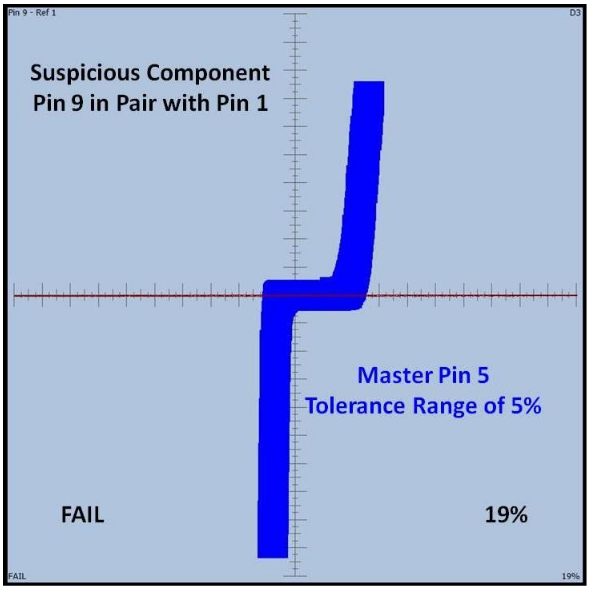



Fig.1 Open circuit I-V characteristics due to missing bond connection.

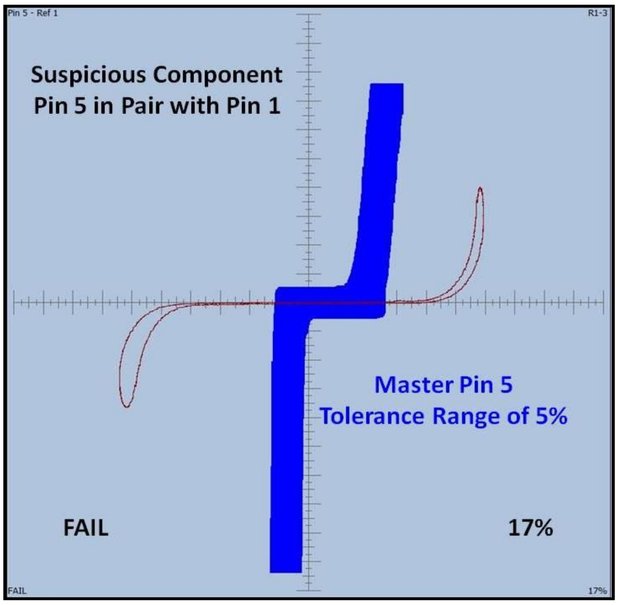



Fig.2 Pin 5 in pair with pin 1 I-V characteristics.

Also other pins evince higher threshold in both direction and higher contact resistance because of poor bonding technology. That poor bonding technology is well seen in the X-ray image of suspicious microcontroller (see Fig. 4). These fake component micro bonds did not have even the necessary mechanical connection stability, and they were releasing easily from the positions after decapsulation unlike at the original microcontrollers. Even the bonding direction and multi-wire backup for individual component terminal to SoC interconnection proves the immaturely poor technology seen already during ASA analysis and in the X-ray image afterwards.

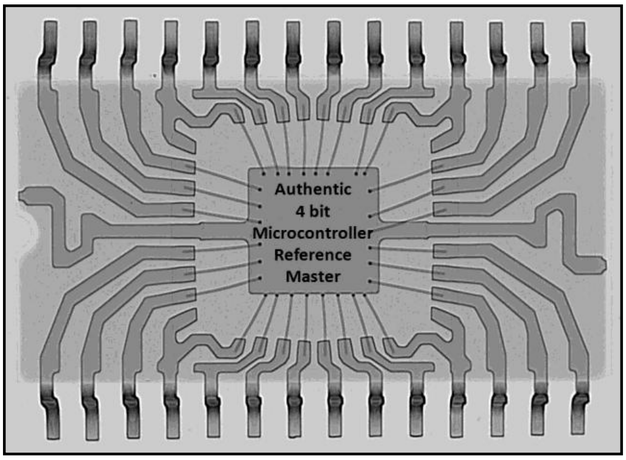



Fig.3 X-ray picture of the original component.

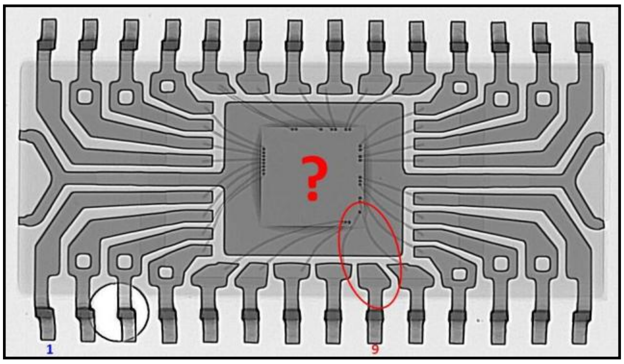



Fig.4 X-ray picture of one component from the suspicious delivery.

X-ray pictures in Figures 3, 4 and 5 have confirmed the missing bonding connection detected with Counterfeit IC detector earlier. X-ray inspection has also revealed a very poor bonding technology at suspicious, and broadly speaking, fake components delivery characteristics.

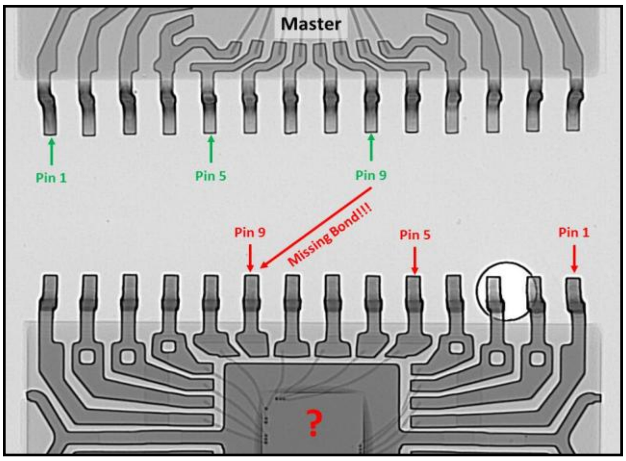



Fig.5 An illustrative comparison of master and suspicious microcontroller X-ray images.

Previous figures illustrate that even the simple and investment not demanding method like ASA can reveal a lot of counterfeit components occurrence cases. We have work out a concept of counterfeit components prevention with the help of devices based on ASA method for our industrial partners. The basic idea consists in cooperation between the product design department and production facility quality management. The product design department professionals can establish and extent step by step a master component model I-V characteristics (pin prints) database immediately when the product is starting in the prototype stage with verified original components. These experts can manage and prepare every reference component model for comparative tests at the very beginning so that any delivery or component supply alternatives can be checked very easily immediately at component arrival or even by a purchasing officer during delivery negotiation without necessity to understand the counterfeit IC detector checking process. Those people need just put the alternative delivery component samples in the counterfeit contact adaptor and start the comparison process.

The following figure shows our ASA workplace. The concept of our Counterfeit IC detector counts with a wide range of integrated circuit ranging from DIL package versions which are more common at components out of active production to modern SMT component packages. The detector inbuilt contact interface accepts DIL components up to 48 pins each. There is a wide range of contact adaptors using that 192 (4x48) DIL socket interface plus 64 pins cable interface what represents a 256 channels for a flexible testing.


Fig.6 Counterfeit IC detector with a variant of general-purpose contact adaptor.

The destructive analytical methods are aimed at opening the component package to reveal the chip. In case we need just to compare whether the component marking corresponds with chip marking, we do not need to preserve the system on chip (SoC) functionality. Nevertheless, we need to perform a function test and thermal field mapping after chip activation in a case of more detailed analysis. In such a case, we want not to damage chip during the package opening process [6].

There are two expert common notions expressing the way of component package opening process. The hermetic component package (metal, ceramic) opening is called “deliding”, the non hermetic package (plastic sorts) opening is called “decapsulation”. Deliding is performed with mechanical means like splitting, drilling, cutting, etc. The decapsulation process uses chemical wet etching with acids like nitric acid and sulfuric acid, package material computer controlled selective ablation with laser beam and dry etching with plasma [1]. Laser beam ablation is a very flexible method concerning opening shapes, patterns and even combining the ablation process with sample identification marking or numbering [8]. However, the SoC functionality preservation requirement limits the depth of ablation which must leave the safety layer of packaging material above chip. That is why the laser material ablation is combined with wet chemical etching as a final stage of chip revealing.

The plasma dry etching equipment is a most expensive method of package material ablation, and it is used very rarely in practical counterfeit component prevention. The plasma dry etching equipments are rather used in big universal analytic laboratories and integrated circuits manufacturers´ laboratories. It makes the sequential chip layer removal for analytical reasons.

# 3 ASA further application possibilities

We have discovered the Counterfeit IC detector another application opportunity during our package material ablation processing recipe creation and its refining for our fiber laser device. The goal of decapsulation and delidding is mostly to preserve the chip functionality for further failure analysis. The chip functionality damaging is tolerable only rarely when there is no further failure analysis supposed. That could be the case of just package and chip marking comparison, and it is again acceptable merely in case that the difference is remarkable. The laser ablation of non hermetic package material is very flexible on one side, but it can be merely used down to the chip surface because of melting influence destroying surface and even deeper structures. There are reported even cases when the chip damages occurred during just component package laser marking process because of glass globules of package plastic material filling [11]. These globules are in some cases chained creating a light way down to the chip and transferring the damaging laser beam energy there. Some sources are reporting the successful not harming package material laser ablation down to the chip without combining it with final wet etch process [12]. Nevertheless, that particular one referenced, is asserting that fact without any convincing proof. There are some pictures illustrating that assertion, but they are also not very convincing. That means that only own verification should precede the acceptance. It may be that the experience is related exclusively to that particular laser only.

Starting at the traditional experience that we need to stop the package material laser ablation at a certain depth and leaving a material safety layer above the chip, we prepared our fiber laser ablation recipe with the help of Counterfeit IC detector. The integrated circuit to be decapsulated step by step was the Master component for itself. We recorded pin prints at the very beginning, and we started the ablation process in small steps going slowly deeper and deeper. We tested the experimental component with the Counterfeit IC detector after each ablation step comparing current pin prints with original once. The ablation process was stopped when the pin prints differed more than set in tolerance range for that case. We could check and preserve the functionality of the component that way. It is necessary to stress that only a complete parametric test would have been a best tool for original functionality conservation, nevertheless, that much simpler ASA way of functionality checking was a well acceptable because we finalized the recipe by reducing a few ablation steps from the point where at least one pin print started to differ from the original one. Figure 7 illustrates the result of exclusively laser ablated package material down to the chip. The melted chip silicon nitride protection layer residual drops are nicely visible. The higher microscope magnification or SEM analysis can show more detailed proves of chip upper layers devastation. Providing the laser ablation is performed with a very carefully composed recipe, we can preserve some significant features like chip labeling with logo, chip model and accompanying numbers. The successful chip origin pinpointing depends on our experience and on our completeness of collected manufacturers´ database and on original manufacture documentation possession.

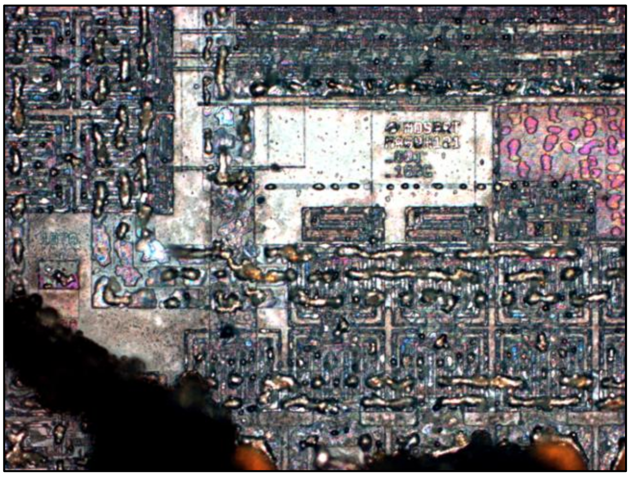


Fig. 7 Chip revealed only with fiber laser.

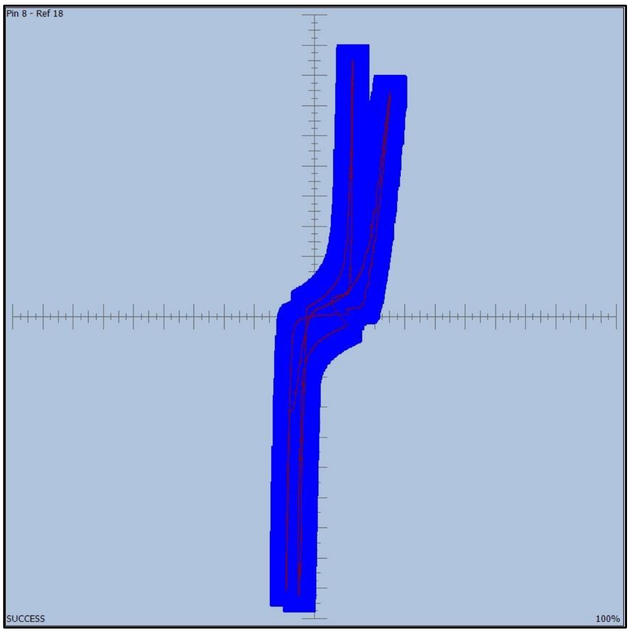



Fig. 8 Dual pin print mode before laser ablation process started.

The following pictures are illustrating the ablation process assisted with Counterfeit IC detector. The blue tolerance range can be set from 0.1% up to 5%. That very narrow tolerance range is applicable only for very special cases when we are tracing component production variance and batch variance at a group of components originating from one source. For unknown origin and suspicious components the 5% tolerance range is well acceptable. That tolerance range is sufficient also for our study of laser ablation influence on the components functionality. We can choose also 3% tolerance range for some cases as a more strict evaluation criterion, or when we need to check the deviations earlier. The test can be set as a single run, or we can choose a loop test to monitor and detect certain instability in I-V characteristics deviations.

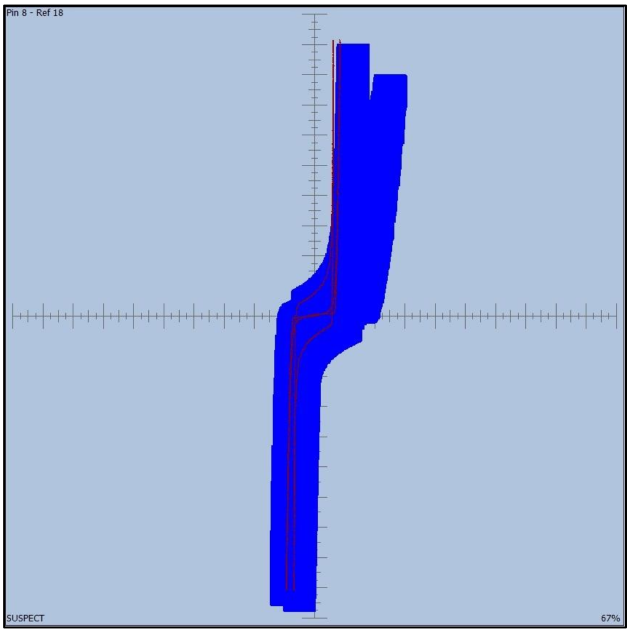
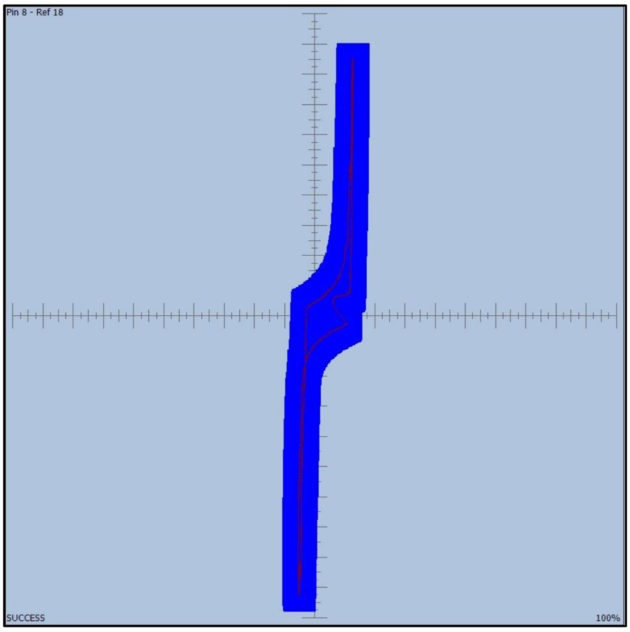



Fig. 9 Dual pin print affected by laser ablation process.




.Fig. 10 High sensitivity mode pin print before laser ablation process started.

Counterfeit IC detector has a wide range of variables to be set for testing. The automatic mode is a very easy one for starting with testing with only a little experience with ASA method. More experienced operators and test engineers can play with arbitrary adjustable parameters compositions. Each sort of components has its own requirements for customized test conditions. The integrated circuit technology plays also a very important role in a right test parameters choice for a successful verification, like for instance for CMOS technology.

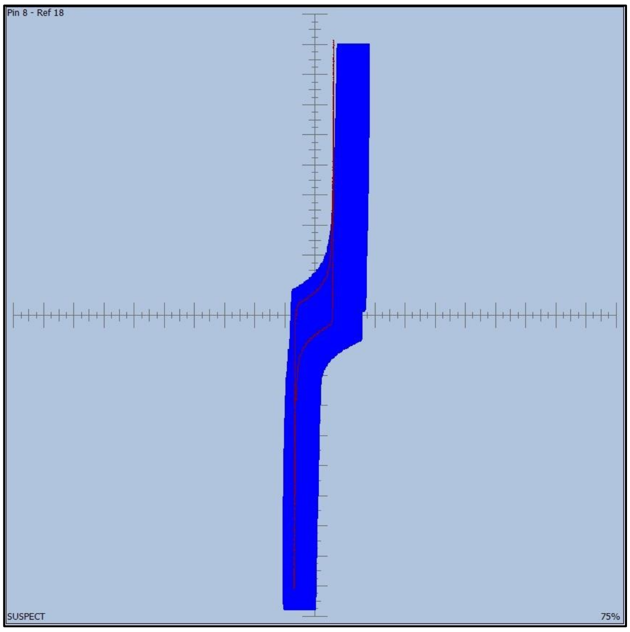



Fig. 11 High sensitivity mode pin print affected by laser ablation process.

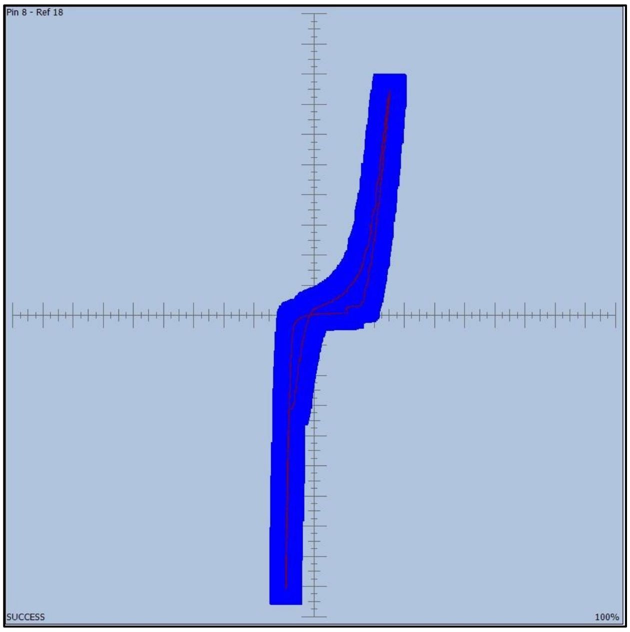



Fig. 12 High speed mode pin print before laser ablation process started.

There are three modes of testing at Counterfeit IC detector. The already mentioned Automatic mode which performs an automatic reference pin choice and scans with two parameters set prepared, the High speed mode and the High sensitivity mode together in one testing procedure what results in a dual pin print signature. That complex mode offers a quick and comprehensive overview about the component for beginners, or it can be very useful when a quick indicative evaluation is preferred. The sensitivity for component I-V characteristic deviations depends also on IC technology.

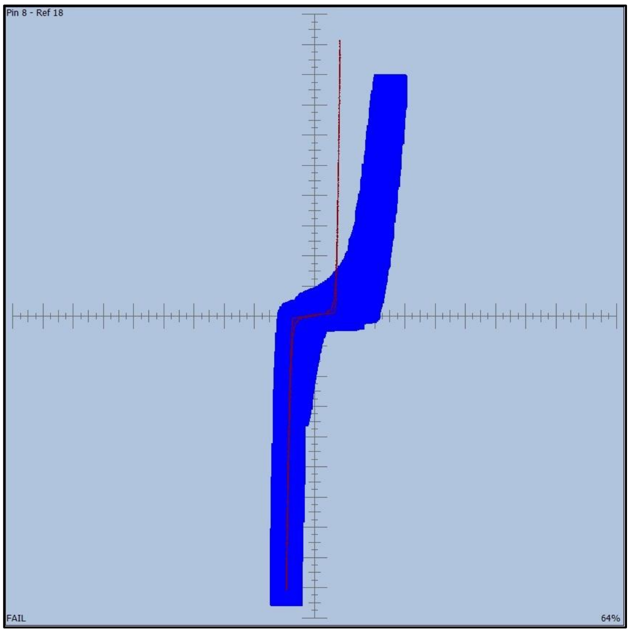



Fig. 13 High speed mode pin print affected by laser ablation process.

Nevertheless, there are many other test variables combinations and settings possible as we are illustrating with High sensitivity scan mode and with High speed scan mode in our illustrating figures. The detailed variables adjustment represents the manual reference pin choice what is mainly the IC ground pin or a Matrix mode which combines all possible pin pairs in course of testing. There is also possible to set scan voltage range, frequency and internal resistance connected in series with the pin pair under test.

## 4 Examples of genuineness evaluation

Our project analytic laboratories are equipped for a wider scope of sample objects that are to be analysed for authenticity, however, most devices and equipment are very useful also for integrated circuits and semiconductor devices in general genuineness. That ASA based equipment was already mentioned in previous section. We can rely on optical microscopy, on scanning electron microscopy with material element content evaluation module, on confocal microscopy, on a X-ray equipment designed especially for electronic non hermetic component packages inspection, and also on a fiber laser equipment for decapsulation and marking [8]. We also established a very fruitful cooperation in the field of final stage of non hermetic package decapsulation process with wet etching. Raman and terahertz spectrometry application possibilities are potentially also in the focus of our research interest. We would like to present illustrative examples of some mentioned

individual analytical methods application for suspicious or failing components from industrial production and also from measurement and metrological devices repair laboratories we are cooperating with.
In the following figures we present some illustrative pictures of our laboratory analytical and processing equipment.

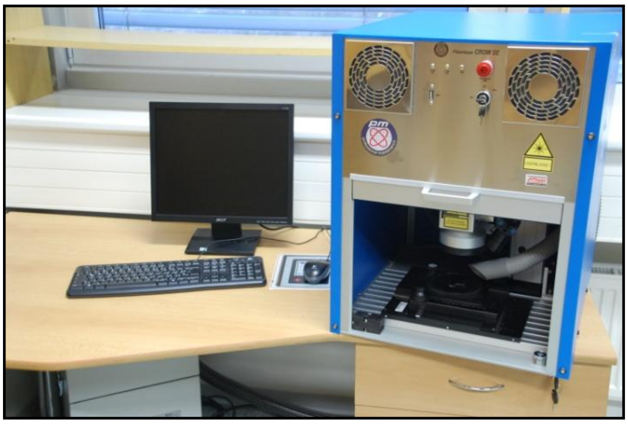


Fig.14 Fiber laser workstation with decapsulation and marking compartment open.

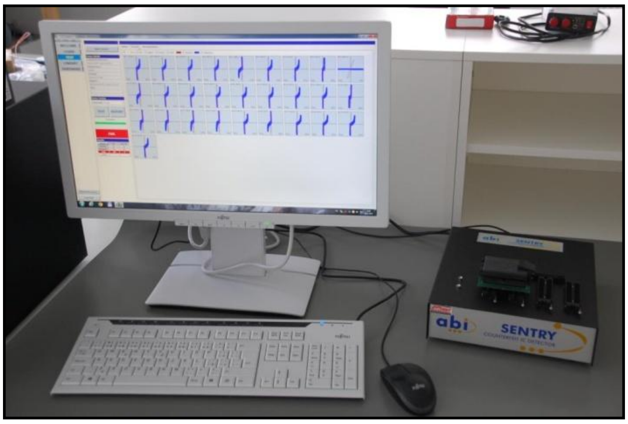



Fig. 15 ASA component pin print comparative evaluation workstation.

The laser ablation process and the following final wet etching procedure are depending also on package material, its filling material and bonding wires materials. The various modifications of epoxy resins filled with miniature glass balls or oxide powder like, like corundum powder for better thermal properties. Bonding wires material comprises mostly copper, gold and aluminum [7]. The package marking technology consists either of ink printing or laser marking. The chip labeling is more sophisticated from the technological point of view because it exploits semiconductor technologies and related materials like metal layers etc. The chip labeling technology is also an authenticity feature.

Fig. 16 X-ray equipment for components.

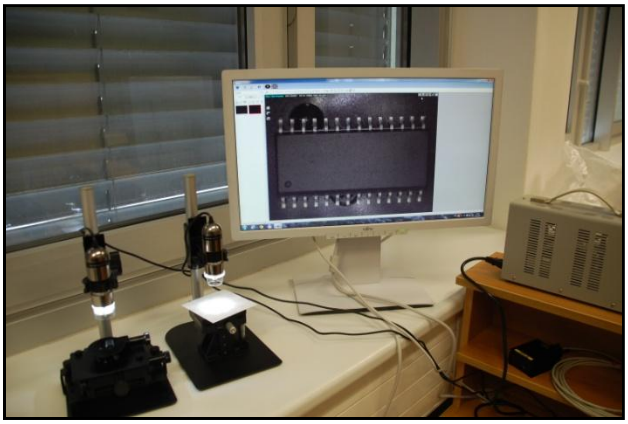


Fig. 17 Workstation for the first optical inspection of samples after laser ablation.

Workstation for the first and preliminary optical inspection is equipped with two small digital microscopes with micrometric XYZ tables and also with axial and radial lighting modules. One microscope has an adjustable magnification up to 200, the other microscope has adjustable magnification up to 400 for the more detailed inspection of package material structure, contact surface condition, and it serves also as an auxiliary inspection tool for detailed optical analysis during new component package ablation recipe development. The digital microscope with lower magnification serves for the package marking and imprint inspection and documentation. The different illumination units with different direction of illumination and different light color are indispensable accessories for optical inspection.

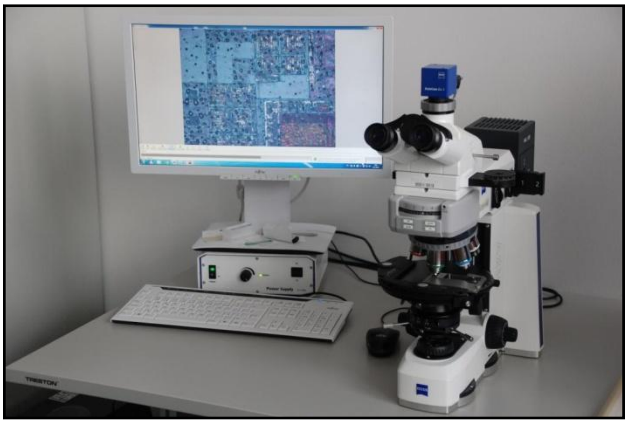


Fig. 18 Optical polarization microscope.

Fig. 19 Confocal microscope

The optical polarization microscope serves very well for SoC visual inspection, mainly for chip logo and marking inspection whether it corresponds with the package marking. We also test the chip surface purity after the final wet etching. The various oblique, radial and coaxial lighting could reveal some interesting markers.


Fig. 20 Radial white colour lighting.

Radial and coaxial object illumination can bring new and very interesting information about material structure, its granularity and also about so called blacktopping what is the counterfeiters´ way how to hide relabeling clues. Different illumination colors also help.


Fig. 21 Scanning Electron Microscope - SEM

## 2.1 Component package optical inspection

The following figures are illustrating the component package and marking inspection.


Fig. 22 Component package in a direct lighting.

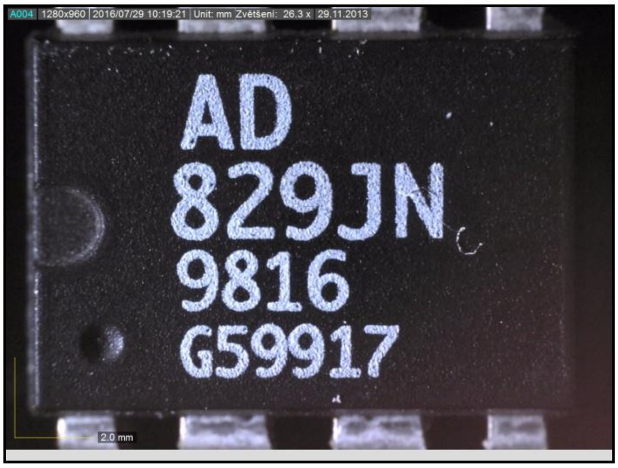



Fig. 23 Oblique lighting stressing surface and marking qualities.

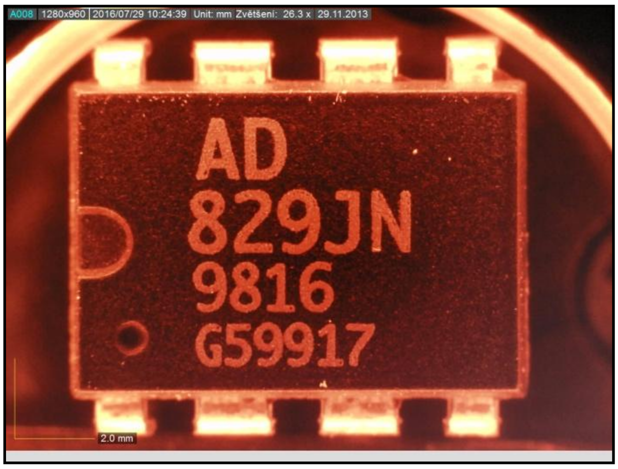



Fig. 24 Red or colour lighting can reveal some feature hidden in white lighting.


Fig. 25 Radial white colour lighting.

The corresponding lighting can very often reveal some new aspects of the component package features in relation to marking, package material structure and its homogeneity. The lighting choice depends either on marking technology (ink printing or laser marking), and also on package material appearance or imprints way of investigation. The lighting colour can also reveal important diversities.


Fig. 26 Radial white colour lighting in combination with direct vertical white lighting.

### 2.2 X-ray inspection

Our X-ray equipment has been designed as a special device for electronic component authenticity evaluation. It has the anode voltage adjustable up to 80 kilo Volts. The following figures are illustrating some component samples we were analysing in our research laboratory.

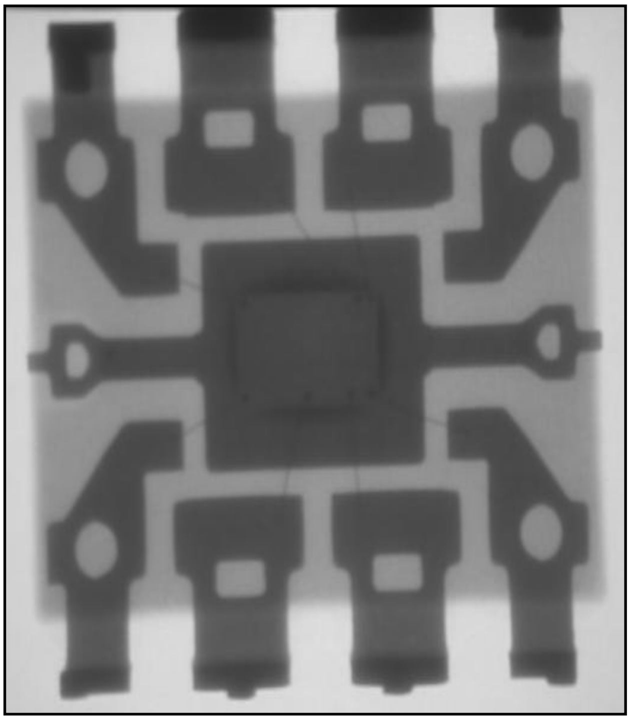


Fig. 27 Operational amplifier OP177 X-ray image.

The X-ray image of OP177 operational amplifier shows contact terminal system, bonding wires and

SoC cemented to the base plate. We may observe different contact terminal shapes and dimensions in one delivery batch what is always suspicious.

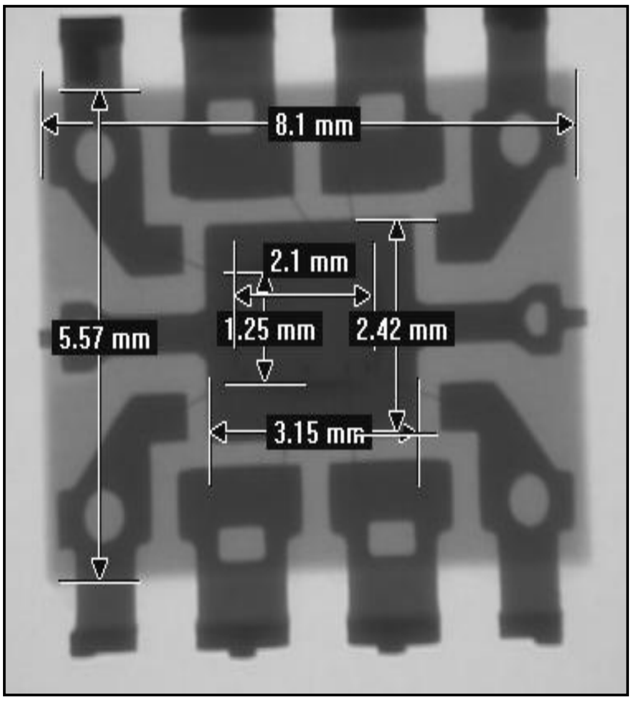



Fig. 28 Operational amplifier OP177 X-ray image with structural dimensions after scale calibration.

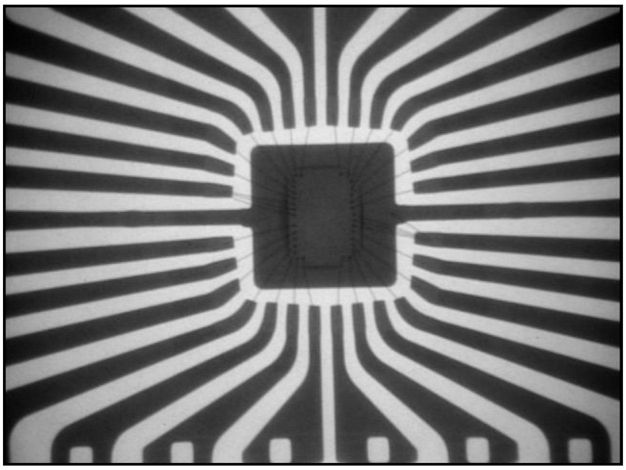


Fig. 29 EEPROM in DIL package X-ray image.

There is very often that the same component type group has a different structure and shape of internal lead frame structure. When the marking tells that these components are manufactured by the same producer and even in the same facility, it is possible to contact the original manufacturer and ask him whether some modifications were realized in course of serial production. If there is more than one component sample to be tested, the decapsulation process can give some answers. However, it is very unlikely that such differences originate from the authentic producer. In many cases, there is always important to set priorities and the detail depth of component analytical evaluation.

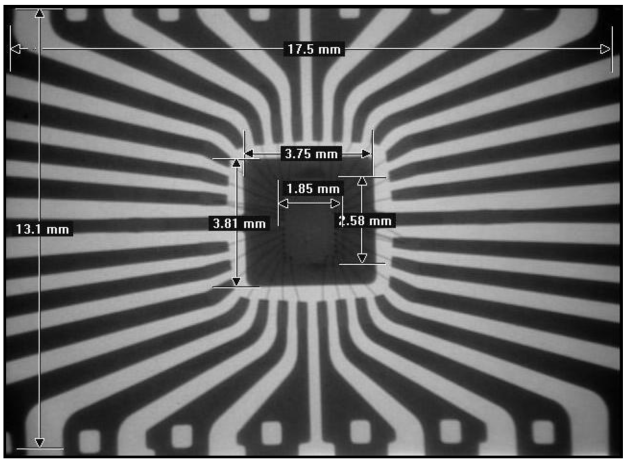



Fig. 30 EEPROM in DIL package X-ray image with dimensional values added.

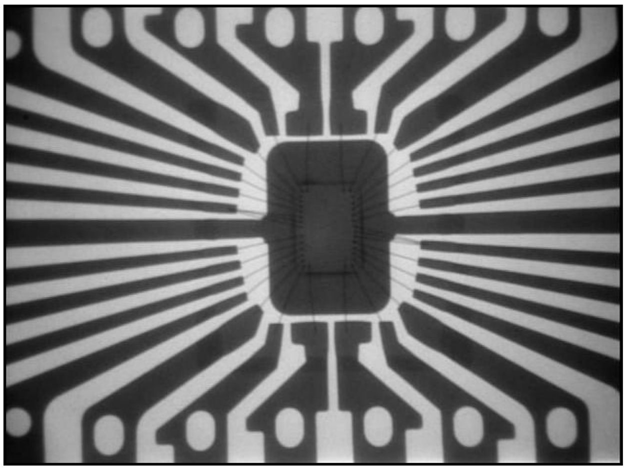


Fig. 31 Same type of EEPROM with distinct contact terminal system X-ray image.

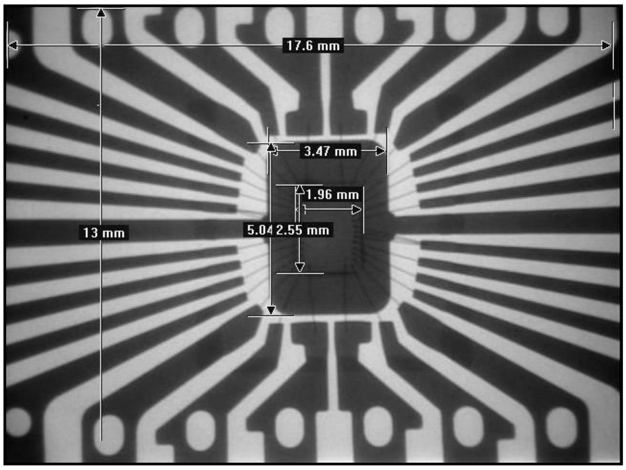



Fig. 32 Distinct EEPROM X-ray image with dimensional values added.

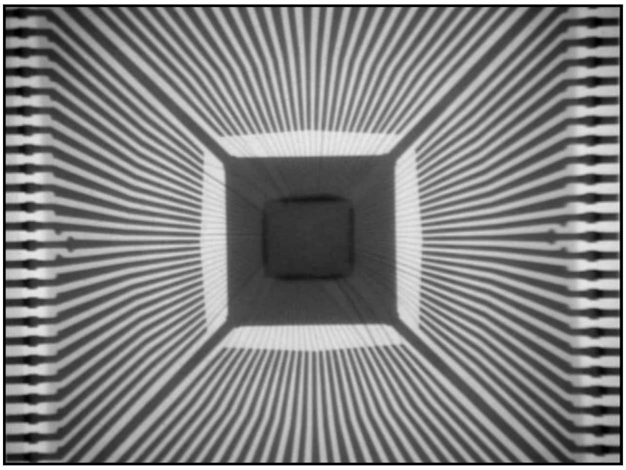


Fig. 33 Integrated circuit in QFP 100 and 0.5 mm pin pitch X-ray image.

The X-ray equipment image graphical processing makes possible to choose among some variants accentuating relevant features of the component internal structure. The scale calibration brings quite accurate structure parts measurement.

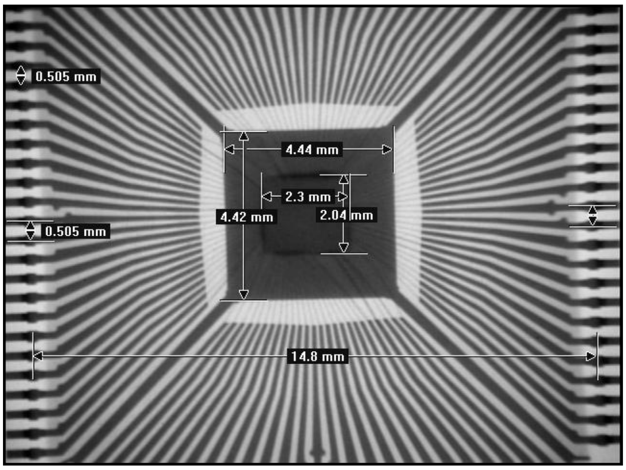



Fig. 34 Integrated circuit in QFP 100 and 0.5 mm pin pitch X-ray image with structural dimensions.

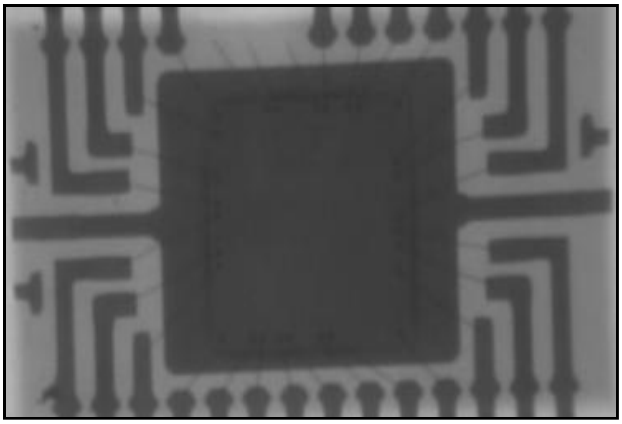


Fig. 35 MAX 211 in SOIC 28 package.

Example of SOIC package is shown in Fig. 35.

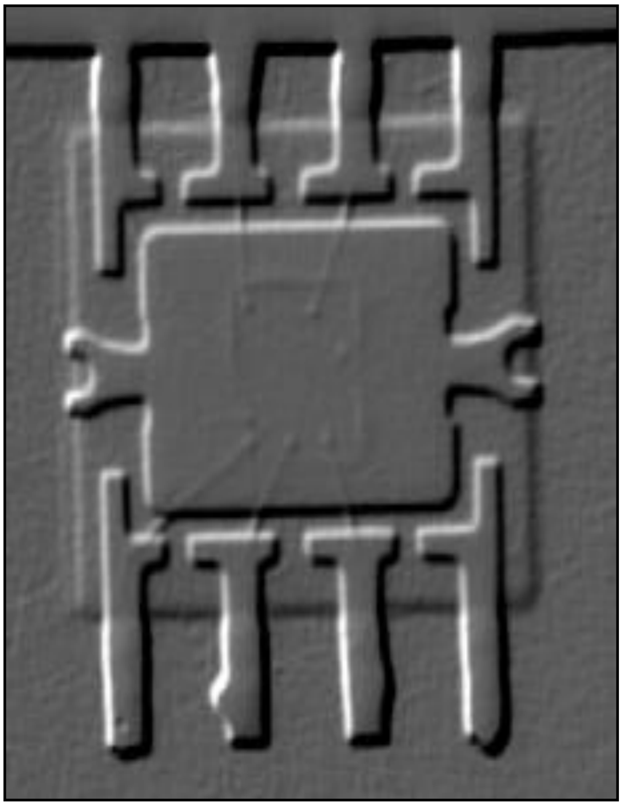


Fig. 36 Example of X-ray image internal structure graphical accentuation.

## 2.3 Laser ablation process

Fiber laser decapsulation process can combine and X-ray component internal structure image with the laser camera picture to aim the chip position for ablative process very accurately. This is very helpful at suspicious and fake component where the chip position is not properly centered so that the laser decapsulation opening can miss the chip right position. That example is illustrated in the Fig. 30. The circular opening is positioned exactly above the chip. The package material residual safety layer is left for final etching.

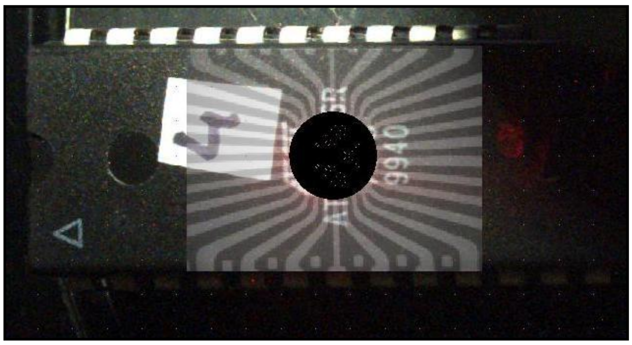


Fig. 37 X-ray picture combined with the laser camera picture.

Component positioning with X-ray picture helps.

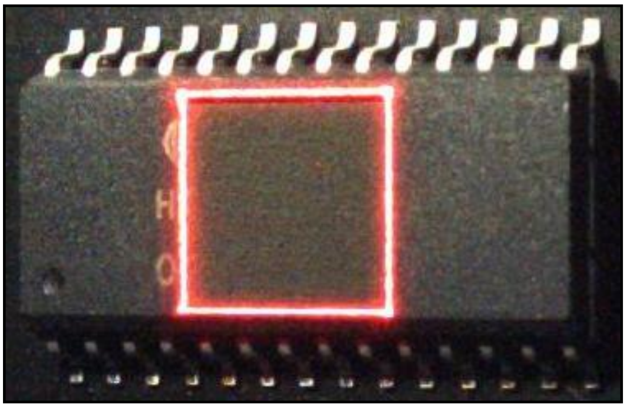


Fig. 38 Package material partially ablated with laser.

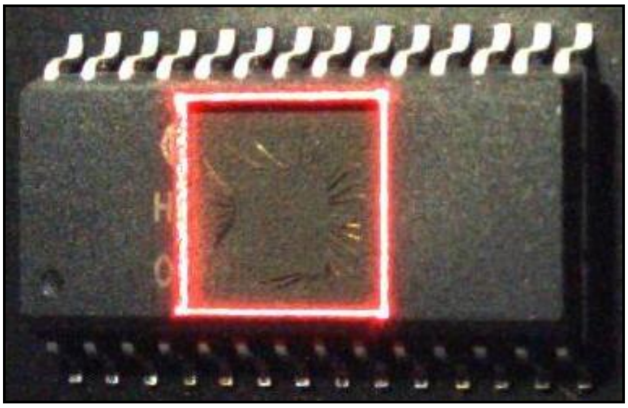


Fig. 39 Further package material ablated to reveal bonding gold wires.

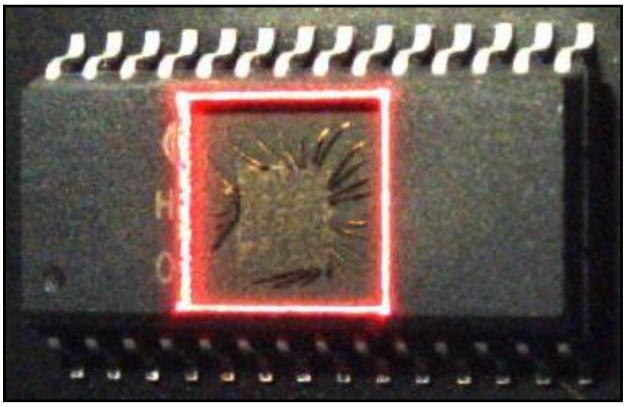


Fig. 40 Very thin protecting package material layer left.

The figures Fig, 38 to Fig. 42 are illustrating the fiber laser ablation process in coarse steps from first layer removal down to the last layer of package material which is finally removed by wet chemical etching with acid mixtures. That final chemical process reveals the chip, but it preserves its functionality and bonding wires continuity for further prospective testing and experimenting. The ablation process can be done exclusively only with laser where the chip logo and marking readability is possible to preserve unlike chip functionality.

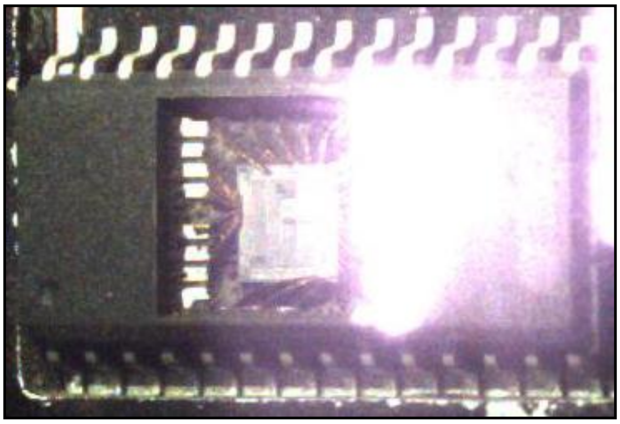


Fig. 41 Laser ablative action illustrated.

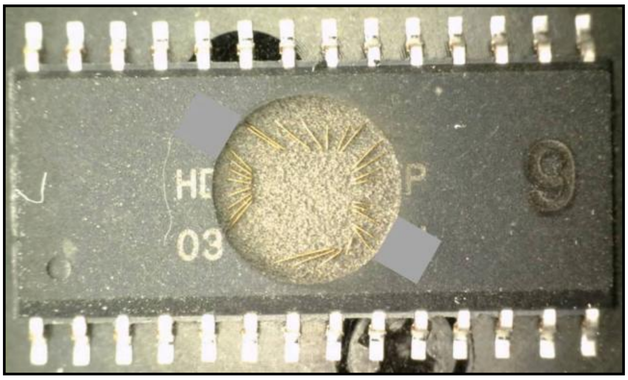


Fig. 42 Circular shape cavity decapsulated with laser for a final chemical etch.

### 2.4 Final chemical etching

Final wet etching has been developed including proper chemicals for a clean chip reveal.

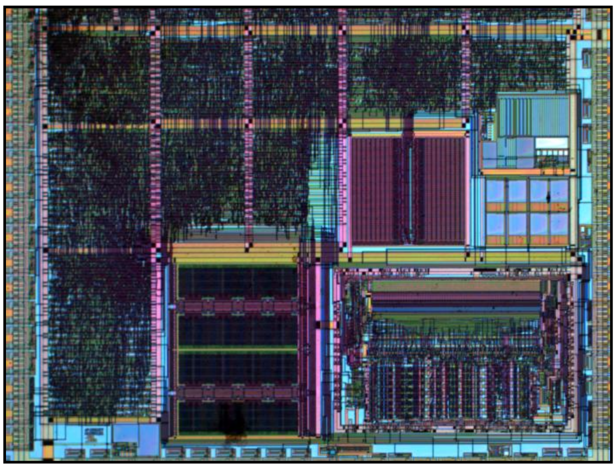


Fig. 43 The microscope magnification set to 50.

The final chemical etching is very often presented as a simple process with only a few drops of relevant concentrated acid. Nevertheless, the etching process is not so easy to be get under control. We had to develop both composition and the process.

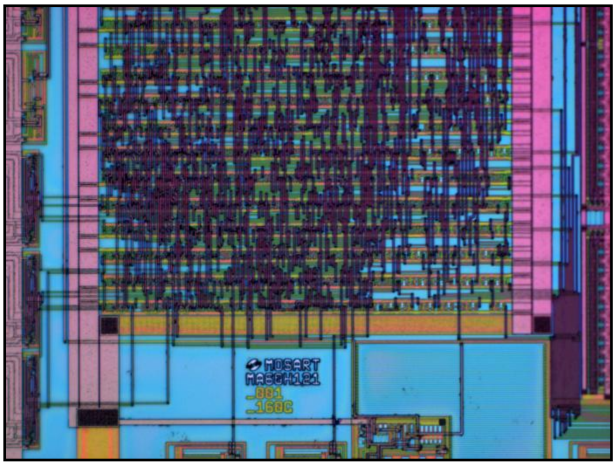



Fig. 44 Microscope set to magnification of 200.

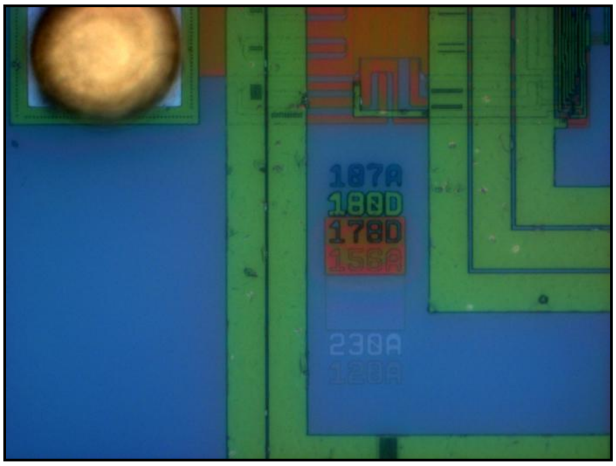



Fig. 45 Microscope set to magnification of 400.

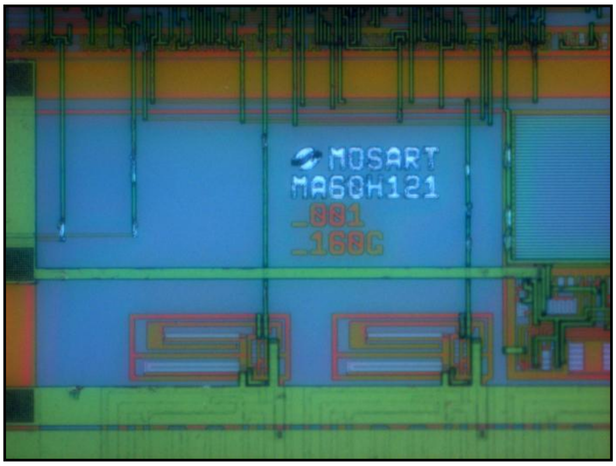



Fig. 46 Microscope set to magnification of 400.

The final etching results are documented with pictures taken on the polarization microscope in Fig. 43 to Fig. 46. The magnification starts at the value of 50 and goes up via magnification of 200 to the magnification of 400 with nicely readable details. The magnification of 400 is not very often accessible for higher components in DIL package. That magnification is easily reachable for low profile SMD packages.

### 2.5 Confocal microscope

Confocal microscope is a very helpful tool for much higher resolution and magnification. The big advantage is the profiling possibility what gives an illustrative idea about the chip surface structure with concave and convex areas.


Fig. 47 Chip logo and chip marking view.

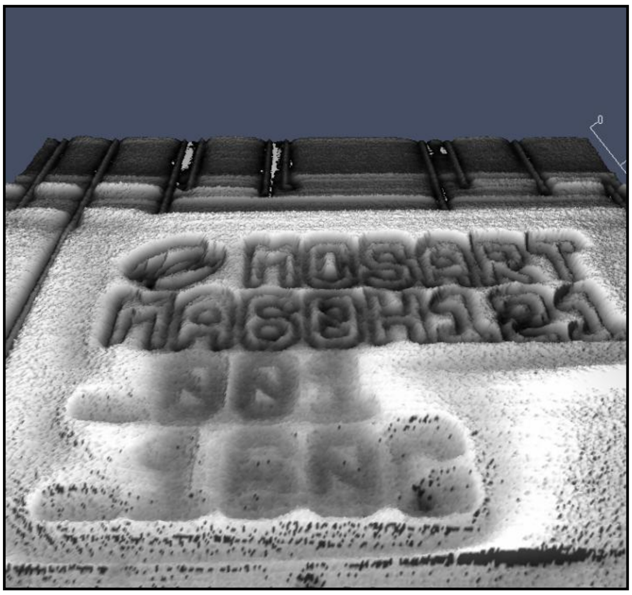



Fig. 48 Chip logo and chip marking side view.

Figures 47 and 48 are illustrating how we can approach details on the chip surface and its profile. That is very important not only for the surface analysis but also for logo and labeling technology.

Fig. 49 The chip logo detailed projection.

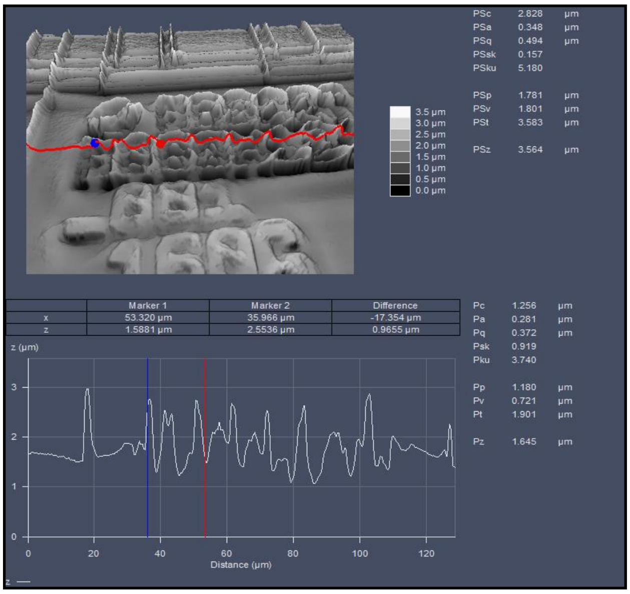



Fig. 50 The chip profile line with vertical differences.

## 2.6 Scanning electron microscopy

Scanning electron microscope (SEM) is a powerful tool for fine surface details imaging and study. The following figures, Fig. 51 to Fig. 53 displays different imaging modes and ways of stressing objects of interest. The only problem at SEM analysis is a good object grounding requirement for the sharp and readable picture. The mode and adjustment variables are giving a wide range of possibilities to adapt SEM for different analyzed objects [10]. The experience with all SEM functions matters so that our experiments are aimed at the verification of those functions how we can benefit from them in component evaluation process.

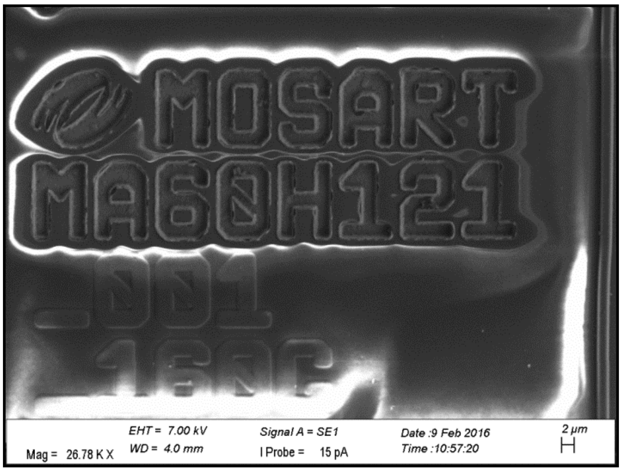



Fig. 51 The chip logo and chip labeling #I.

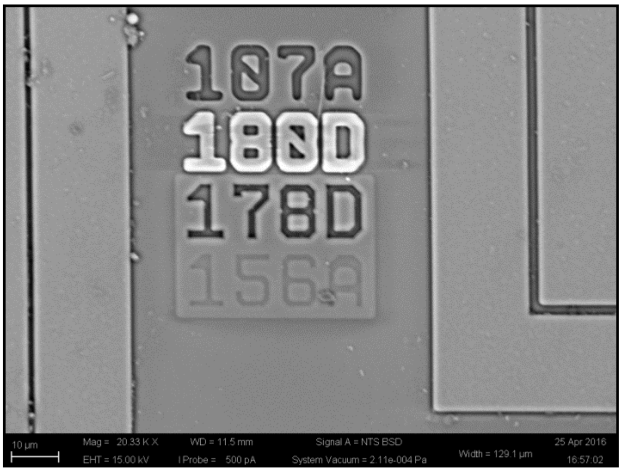



Fig. 52 The chip technology test numbers.


Fig. 53 The chip logo and chip labeling #II.

The scanning electron microscope has proved for many integrated component samples so far in spite of the fact that it has been delivered only recently. We are hard working on managing its functions, modes and adjustment ranges to be able to get most of it soon. All opportunities for various objects analysis are bringing the inspiration for application.

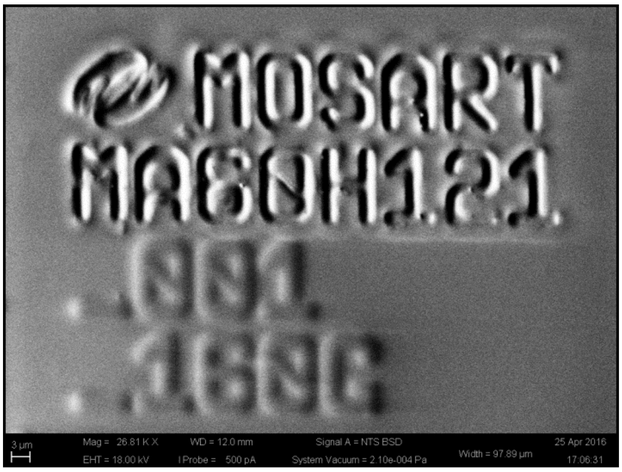



Fig. 54 The chip logo and chip labeling #III.


Fig. 55 The chip logo and chip labeling #IV.

#### 2.6.1 SEM material element analysing module

A very useful SEM extension module is the material composing chemical elements analyzing module.

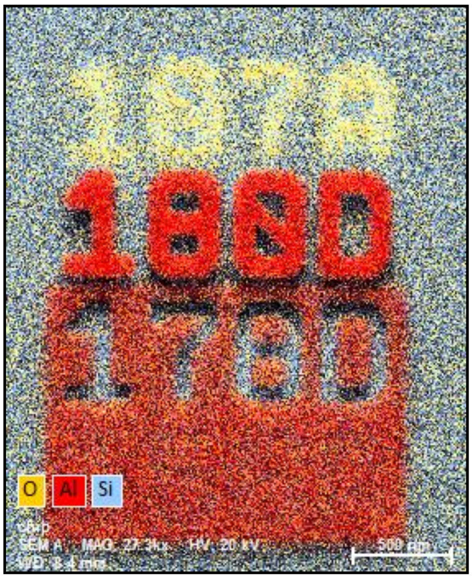



Fig. 56 Chip labeling material elements.

## 4 Fake component case example

The last section of our paper is devoted to a very interesting case when a cooperating company has provided us with defective components after having replaced them for spare ones during failed measurement system repair. It was meant for our training experiments or laboratory exercises. Our component genuineness testing obsession and curiosity made us to pass those components through our inspection procedures. We were very surprised when we found that in a DIL 8 package marked as an operational amplifier OP177 by Analog Devices was a chip by PMI brand, dated 1987.


Fig.57 OP177 component by alleged AD package illuminated with direct vertical lighting.

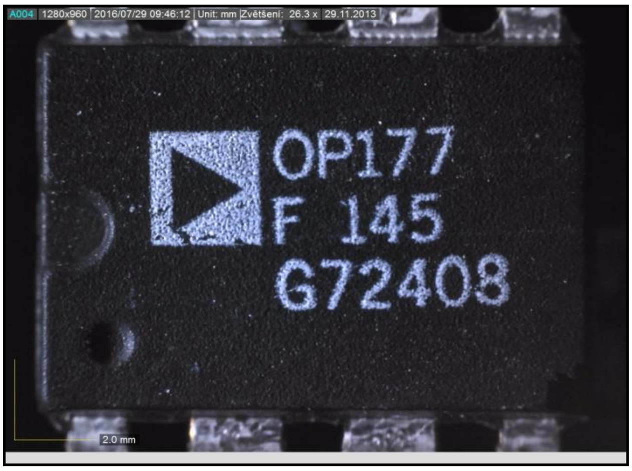



Fig. 58 OP177 component by alleged AD package labeling illuminated with oblique lighting.

The OP177 package marking pictures are showing the poor instable ink print marking with a very low adhesion to the package material what is out of question at original manufacture´s product. Succeeding pictures are confirming that poor adhesion because even the component careful treatment during inspection lead to further wiping the marking ink print off. Even the chip is cemented off component center what is also out of question for OEMs. The gold bonding wires were also very weakly fixed to the chip contacting pads.

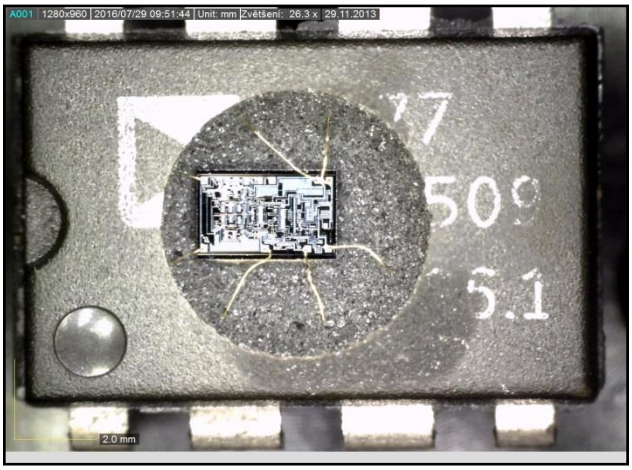


Fig.59 OP177 by Analog Devices package labeling illuminated with radial lighting.

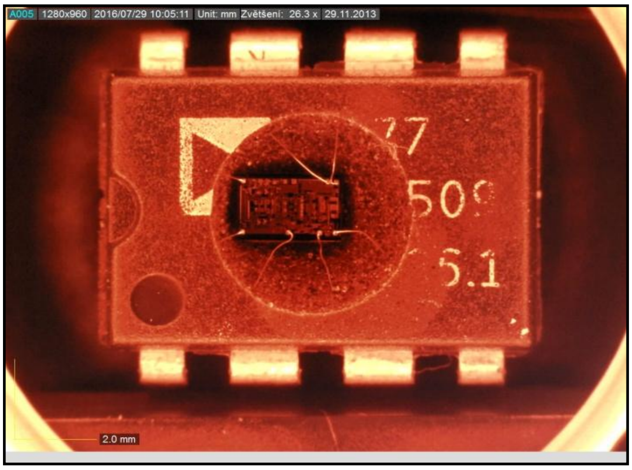


Fig. 60 OP177 component by AD package labeling illuminated with red radial lighting.

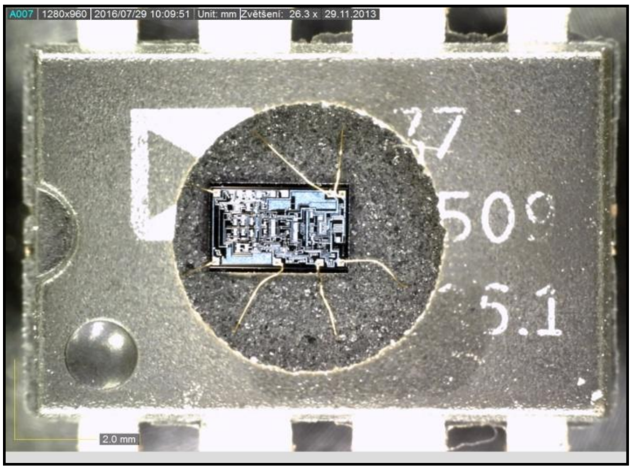


Fig. 61 OP177 by AD package marking in direct vertical lighting combined with radial lighting.

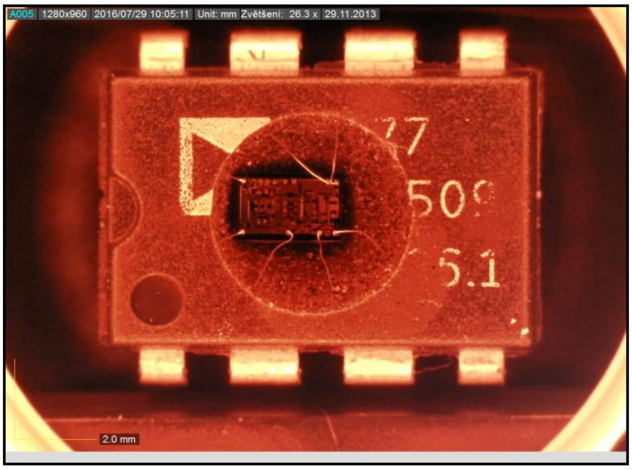


Fig. 62 OP177 by AD package labeling illuminated with red radial lighting combined with direct white vertical lighting.

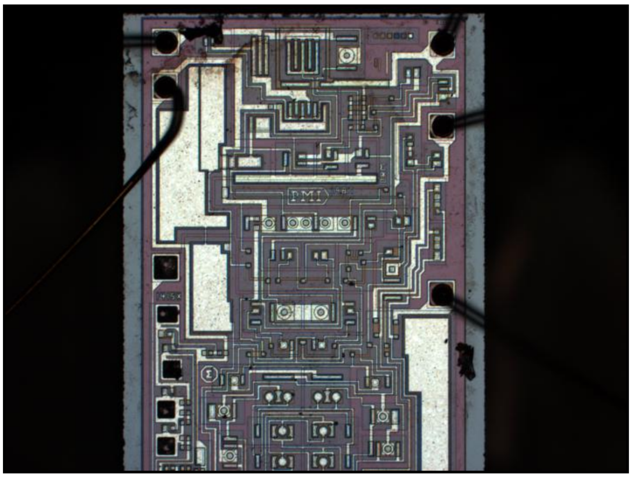


Fig. 63 The revealed PMI chip with polarization microscope magnification set to 50.

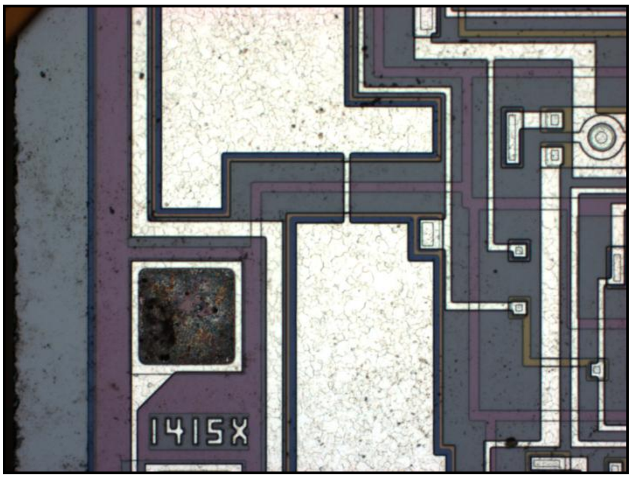



Fig. 64 Revealed PMI chip marking with polarization microscope magnification set to 200.

This finding has lead to an organizational means in purchasing spare parts and treating the failed components. All are to be tested in our laboratory.

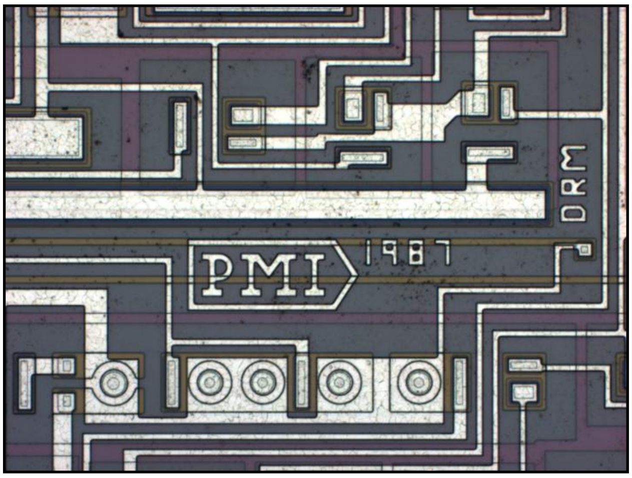


Fig. 65 Revealed PMI chip logo and date with polarization microscope magnification set to 200.

## 5 Conclusion

The inspection and component genuineness evaluation ability of our laboratories is developing continuously. The recent extension of our analytical equipment park is a promising flexibility for the close future when we want to extent our cooperation with industry as an experienced laboratory assisting at counterfeit components prevention from assembly process invasion. We also would like to verify how to involve Raman and terahertz spectroscopy, or alternatively and supplementary, other analytical method convenient for counterfeit semiconductor components and other fake electronic components detection and evaluation physical methods.

**ACKNOWLEDGMENTS**

Authors acknowledge support from Ministry of Education, Youth and Sports of the Czech Republic (CEBIA-Tech No. CZ.1.05/2.1.00/03.0089) and (LO1212) together with the European Commission (ALISI No. CZ.1.05/2.1.00/01.0017).

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