FPGA IMPLEMENTATION OF 3GPP-LTE PHYSICAL DOWNLINK CONTROL CHANNEL USING DIVERSITY TECHNIQUES

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Abstract- Long Term Evolution (LTE) of UMTS Terrestrial Radio Access and Radio Access Network is a Fourth Generation wireless broadband technology which is capable of providing backward compatibility with 2G (Second Generation) and 3G (Third Generation) technologies. LTE is able to deliver high data rate and low latency with reduced cost This paper proposes a novel architecture for Single Input Single Output(SISO) 1x1, Multiple Input Single Output (MISO) 4x1, Multiple Input Multiple Output (MIMO)4x2 for Physical Downlink Control Channels of LTE. The physical downlink channel processing involves as scrambling, modulation, layer mapping, precoding, data mapping to resource elements at transmitter and demapping from resource elements, decoding, delayer mapping, demodulation and descrambling at receiver. In the proposed architecture, these steps are carried out in a single architecture comprises of all the data and control channels. Based on simulation and implementation, results are discussed in terms of Register Transfer Level (RTL) design, Field Programmable Gate Arrays (FPGA) editor, power estimation and resource estimation. To simulate all the modules of all control channels, ModelSim is used. For synthesis and implementation of the above architecture PlanAhead 13.2 tool on Virtex-5, xc5vlx50tff1136-1 device board is used.

Keywords- **Long Term Evolution (LTE), Single Input Single Output (SISO), Multiple Input Single Output (MISO), Multiple Input Multiple Output (MIMO) Physical Downlink Shared Channel (PDSCH), Physical Broadcast Channel (PBCH) and Physical Multicast Channel (PMCH).**

1. Introduction

The 3GPP (Third Generation Partnership Project) has been motivated to work on the Long-Term Evolution (LTE) standard, due to heavy usage of mobile data with many new applications like multimedia online gaming, mobile TV, streaming of video contents etc. Now, LTE is a new wireless standard in mobile network technology. It is also referred to as Evolved UMTS Terrestrial Radio Access(EUTRA) or Evolved UMTS Terrestrial Radio Access Network (E-UTRAN). LTE standard fulfills the International Mobile Telecommunication- Union (IMT-U) requirements for data rate, capacity, spectrum efficiency and latency using new technical principles. LTE uses Orthogonal Frequency Division Multiple Access (OFDMA) in downlink and Single Carrier Frequency Division Multiple Access (SC-FDMA) in uplink for its air interface. Further, Multiple Input Multiple Output (MIMO) antenna schemes have become essential parts of LTE. In LTE, the protocol architecture is simple compared to the existing Universal Mobile Telecommunication System(UMTS) protocol concepts.

LTE standard has six physical layer channels namely, physical Hybrid ARQ Indicator Channel (PHICH), Physical Control format Indicator Channel(PCFICH), Physical Downlink Control Channel (PDCCH), Physical Broadcast channel (PBCH), Physical Multicast Channel (PMCH) and Physical Downlink Shared Channel (PDSCH) for downlink operation i.e., base station (usually referred to as eNodeB) to the user equipment (UE). All downlink physical channels get information from the higher layer. [2]. PHICH, PDCCH and PCFICH are the control channels in LTE downlink. These three channels are used for scheduling assignments. PDSCH, PBCH and PMCH are the downlink data channels of LTE and they are used for multicast and/or broadcast operations. LTE use two different frame structures namely Time Division Duplexing (TDD) and Frequency Division Duplexing (FDD) and their illustrations are given in [3]. FDD and TDD frame structures are represented as Type 1 and Type 2 in LTE standard. In this paper, FDD frame structure is followed. Though a number of research papers have been published in the implementation of LTE physical control channels, efficient and optimized design of LTE channels is still a research topics.

The objective of this paper is to propose a novel FPGA architecture for the implementation of LTE downlink control channels in MIMO environment. A brief out line of LTE downlink Control Channels is given in section 2; system model and its processing steps are explained in section 3; the concept of Alamouti's Space Frequency Block Codes is explained in section 4, the proposed architectures are elaborated in section 5; and the simulated and implemented results are discussed in section 6.

2. LTE Downlink Control Channels

The LTE downlink physical channels include three control channels and three transport channels. The control channels PDCCH, PCFICH and PHICH are essential for the successful reception, demodulation and decoding of the PDSCH, PBCH and PMCH data [1]. The signals for the control channels are transmitted at the start of each subframe. Channels are the slots where the information bits are placed after processing at the transmitter. The control channels are described in the following sections

2.1 Physical Downlink Control Channel

PDCCH carries the downlink resource allocation related to the transport channel PDSCH. The control information carried by PDCCH is known as Downlink Control Information (DCI) which is transmitted as an aggregation of Control Channel Elements (CCEs). CCEs consists of Resource Element Groups (REGs) each containing four Resource Elements (REs) with a RE carrying two bits. PDCCH carries information about the Resource Block (RB) allocation, modulation, coding scheme and power control information. PDCCH occupies the first 1, 2, 3 OFDM symbols of a subframe. The modulation employed in this channel is Quadrature Phase Shift Keying (QPSK) in which two bits are taken and modulated. The DCI and PDCCH are having specific formats. The PDCCH supports four formats numbered from 0, 1, 2, and 3 as shown in Table 1. Each CCE has 9 REGs in PDCCH. Format of 0 carries 72 PDCCH bits.

Table I : PDCCH Format

PDCCH Format	Number of CCEs	Number of REGs	Number of PDCCH bits
0	1	9	72
1	2	18	144
2	4	36	288
3	8	72	576

2.2 Physical Control Format Indicator Channel

PCFICH carries the information about the number of Orthogonal Frequency Division Multiplexing (OFDM) used for control channels [2]. Typically the control format indicator (CFI) value belongs to the set {1, 2, 3, 4}. 4 is reserved for future expansion. By estimating CFI, the UE identifies the OFDM symbols that contain control information. PCFICH lies in the first OFDM symbol and is the first information received by the receiver after the reference signal. It is mapped to REGs. The two bit CFI undergoes block coding first to become 32 bits and mapped to subcarriers after QPSK modulation. PCFICH is transmitted when the number of OFDM symbols used for PDCCH is greater than zero.

2.3 Physical Hybrid Indicator Channel

PHICH carries ACK/NACK data for the uplink channel PUSCH [2]. The positive acknowledgement is referred ACK and negative as NACK, depending upon whether the transmitted data is correctly received or not. If NACK is received, then retransmission should be done. In practice, many PHICHs are mapped to a PHICH group, with each group having a number. The PHICHs in a group are differentiated by orthogonal sequences. PHICH index number is used to identify each PHICH. For the FDD frame structure, the number of PHICH groups in a subframe is given as

$$N_{\mathrm{PHICH}}^{\mathrm{group}} = \left\lceil N_{\mathrm{g}} \left(N_{\mathrm{RB}}^{\mathrm{DL}} / 8 \right) \right\rceil \quad (1)$$

for normal cyclic prefix, where $N_g \in \{1/6,1/2,1,2\}$ is provided by higher layers and $N_{\mathrm{RB}}^{\mathrm{DL}}$ is the number of resource blocks in downlink transmission based on bandwidth configuration .

3.System Model

Combined architectures for all the three control channels for transmitter and receiver are proposed in this section. The channel processing steps that are required for transmitter and receiver are illustrated in Figure 1 and Figure 2 respectively.

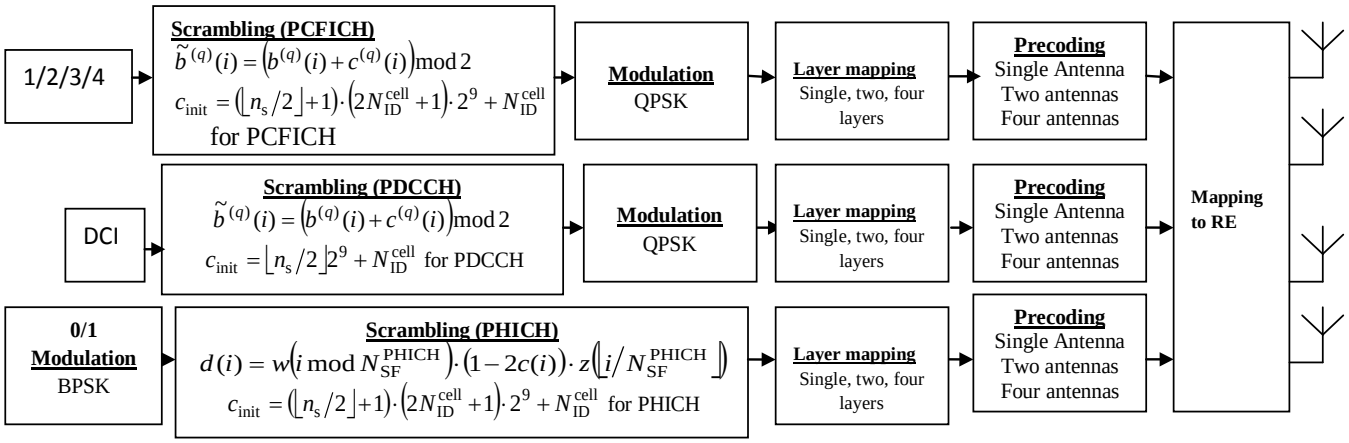


Figure 1 :Transmitter processing steps

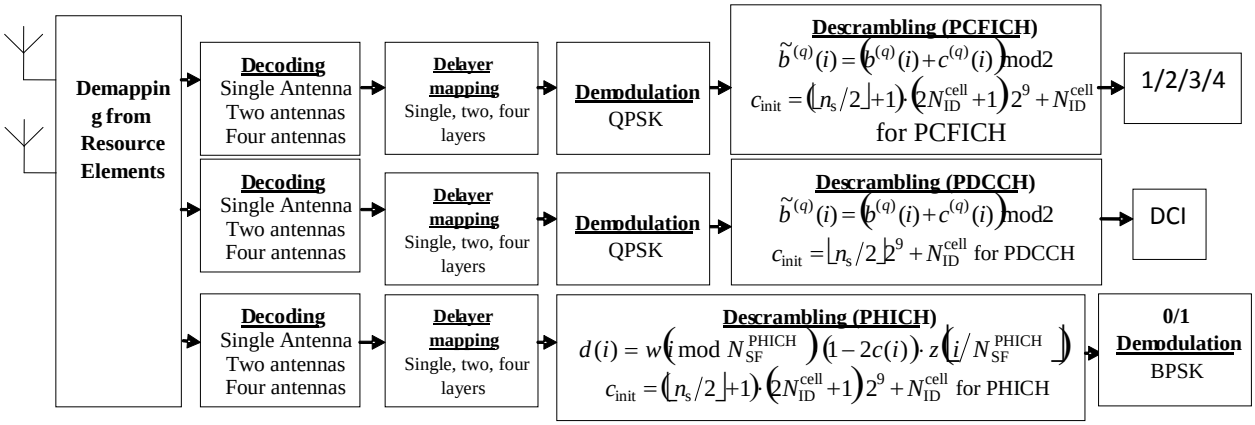


Figure 2: Receiver processing steps

3.1 Channel processing steps at Transmitter

Scrambling, modulation, layer mapping, precoding and mapping to resource elements are the important steps which are carried out by transmitter. Since mapped data is passed through the channel, estimation of channel is mandatory. All channels are done in this way at transmitter with their unique characteristics and specifications. Under this section each steps are explained for both channels.

3.1.1 Scrambling

Data to be transmitted are passed through this module initially. Significance of this module is making the data as unintelligible to the intruder. To achieve this, pseudo random Gold sequence is generated continuously at the transmitter. The incoming data and Gold sequence are logically combined using Exclusive-OR operation to generate the scrambled bits. Mathematically, it is given by [3]

$$\tilde{b}^{(q)}(i) = \left(b^{(q)}(i) + c^{(q)}(i)\right) \bmod 2 \quad (2)$$

where $b^{(q)}(i)$ is the original information and $c^{(q)}(i)$ is the initialization vector. $c^{(q)}(i)$ for PCFICH is given by

$$c_{\text{init}} = \left(\lfloor n_s/2 \rfloor + 1\right) \cdot \left(2N_{\text{ID}}^{\text{cell}} + 1\right) \cdot 2^9 + N_{\text{ID}}^{\text{cell}} \quad (3)$$

$c^{(q)}(i)$ for PDCCH is defined by equation (4)

$$c_{\text{init}} = \lfloor n_s/2 \rfloor 2^9 + N_{\text{ID}}^{\text{cell}} \quad (4)$$

In PHICH, the block of modulation symbols are symbol-wise multiplied with an orthogonal sequence and scrambled, resulting in a sequence of modulation symbols. It is represented as,

$$d(i) = w\left(i \bmod N_{\text{SF}}^{\text{PHICH}}\right) \cdot (1 - 2c(i)) \cdot z\left(\lfloor i / N_{\text{SF}}^{\text{PHICH}} \rfloor\right)$$
$$i = 0,.....M_{symb} - 1 \quad (5)$$

Where $M_{\text{symb}} = N_{\text{SF}}^{\text{PHICH}} \cdot M_{\text{s}}$ and

$$N_{\text{SF}}^{\text{PHICH}} = \begin{cases} 4 & \text{normal cyclic prefix} \\ 2 & \text{extended cyclic prefix} \end{cases}$$

and $c(i)$ is a cell-specific scrambling sequence. At the start of each subframe, it is generated using a scrambling sequence generator that are initialised with

$$c_{\text{init}} = \left(\lfloor n_{\text{s}}/2 \rfloor + 1\right) \cdot \left(2N_{\text{ID}}^{\text{cell}} + 1\right) \cdot 2^9 + N_{\text{ID}}^{\text{cell}} \quad (6)$$

3.1.2 Modulation

Downlink data channels of LTE use different modulation schemes such as QPSK, 16 QAM (Quadrature Amplitude Modulation) and 64 QAM. PCFICH and PDCCH use QPSK and PHICH uses BPSK modulation. In PHICH, modulation occurs before scrambling stage because it is considered to be important channel to give back the acknowledgement or no acknowledgement for the earlier data received. So such information is carefully modulated and transmitted. Predefined values for these modulations are tabulated in [3]. By using the given in-phase (I) and quadrature (Q) values all the scrambled bits are converted in to complex bit values.

3.1.3Layer Mapping

Modulated bits are mapped to the single or to the higher layers. Higher layers may be two or four. PDSCH is mapped to all higher layers by using transmitter diversity techniques and space diversity techniques [3]. For transmission on a single antenna port, a single layer is used and the mapping is defined by expression (7)

$$x^{(0)}(i) = d^{(0)}(i) \text{ with } M_{\text{symb}}^{\text{layer}} = M_{\text{symb}}^{(0)} \quad \text{....(7)}$$

3.1.4 Precoding

Precoding is the process of creating vectors for layer mapped data. Similar to layer mapping, precoding can be done on single, two or four layers. Precoded vectors are estimated by using mathematical expressions for both transmitter and space diversity techniques [3]. For transmission on a single antenna port, precoding is defined by equation (8)

$$y^{(p)}(i) = x^{(0)}(i), \quad i = 0,1,\ldots,M_{\text{symb}}^{\text{ap}} - 1, \quad M_{\text{symb}}^{\text{ap}} = M_{\text{symb}}^{\text{layer}} \quad (8)$$

For transmission on two antenna ports, the output $y(i) = \left[y^{(0)}(i) \quad y^{(1)}(i)\right]^T$, $i = 0,1,\ldots,M_{\text{symb}}^{\text{ap}} - 1$ of the precoding operation is defined by expression (9)

$$\begin{bmatrix} y^{(0)}(2i) \\ y^{(1)}(2i) \\ y^{(0)}(2i+1) \\ y^{(1)}(2i+1) \end{bmatrix} = \frac{1}{\sqrt{2}} \begin{bmatrix} 1 & 0 & j & 0 \\ 0 & -1 & 0 & j \\ 0 & 1 & 0 & j \\ 1 & 0 & -j & 0 \end{bmatrix} \begin{bmatrix} \text{Re}\left(x^{(0)}(i)\right) \\ \text{Re}\left(x^{(1)}(i)\right) \\ \text{Im}\left(x^{(0)}(i)\right) \\ \text{Im}\left(x^{(1)}(i)\right) \end{bmatrix} \quad (9)$$

for $i = 0,1,\ldots,M_{\text{symb}}^{\text{layer}} - 1$ with $M_{\text{symb}}^{\text{ap}} = 2M_{\text{symb}}^{\text{layer}}$

The precoding operations for all control channels under the transmission on four antenna ports is defined by expressions in [3]

3.1.5 Mapping to resource elements

Precoded data are mapped to the LTE grid structure as illustrated in [4]. This grid structure is designed to accommodate reference signals, unused signals, and all data and control channel information. Since LTE is the scalable bandwidth wireless technology (1.4 MHz to 20 MHz), this SISO architecture is done by taking the bandwidth as 1.4MHz. This grid structure has 72 rows and 10 subframes of 2 slots each. Each subframe has 14 columns [3]. Data should be arranged in their corresponding positions. To do this massive task as easier counter has placed, for row, column and slot identifications.

3.2 Channel processing steps at Receiver

Similar to transmitter, receiver has to perform some steps as illustrated in Figure 2 to get back the original data. The steps carried out by receiver are discussed in this section.

3.2.1 Demapping from resource elements*:*

After data get mapped to the grid, it passes through the channel. So estimation of channel is necessary. In this paper, channel estimation is done for all mapped data by taking 8 point FFT corresponding to their row (from 0 to 71) as given in Figure 2. While receiving the data receiver has to do the channel de-estimation process initially and then demap all the data from resource element group. In receiver side also counters are placed to find row, column and slot positions.

3.2.2 Decoding

Decoding at the transmitter side is done by using single antenna, two antennas or four antennas. All the

data from demapping from resource element module get decoded on the single layer, two or four layers.

3.2.2 Decoding and Detection

Decoding at the transmitter side is done by using single antenna, two antennas or four antennas. All the data from demapping from resource element module get decoded on the single layer, two or four layers. After decoding the data, Detection is performed by comparing the decoded results with the predefined modulation values [3] and generating the resultant bits corresponding to the modulation scheme. If it is QPSK, the resultant bits are 2, 4 for 16 QAM and 6 for 64 QAM.

3.2.3 Delayer Mapping

The two data paths received by the diversity enviroinment is concatenated to form a single layer in delayer mapping module.

3.2.4 Descrambling

Single layer data is then given to the descrambler module to make the data known to the receiver. At transmitter side pseudo random gold sequence is used to scramble the data. In descrambling the same pseudo random gold sequence is Ex-Or ed with the incoming bit of the descrambler module.

4. Alamouti Coding Scheme In Space Time Block Codes

Alamouti code proposed by S.M. Alamouti belong to the class of codes called Space Time Block Codes (STBC) which refers coding across Space by using multiple transmit and receive antennas and Time by using multiple symbol periods. Alamouti code operates on blocks of input bits having two dimensional code matrices [1],[2].Here, the same data is transmitted redundantly over two antennas. To generate a redundant signal, space-time codes are used. Alamouti developed the first codes for two antennas. Space-time codes additionally improve the Bit Error Rate (BER) performance and make spatial diversity usable. The signal copy is transmitted not only from a different antenna but also at a different time. This delayed transmission is called delayed diversity. Space-time codes combine spatial and temporal signal copies as illustrated in Figure (1). The signals s_1 and s_2 are multiplexed in two data chains. After that, a signal replication is added to create the Alamouti space-time block code. In this paper, this space time block code is implemented for 2x1 MISO systems and 2x2 MIMO systems.

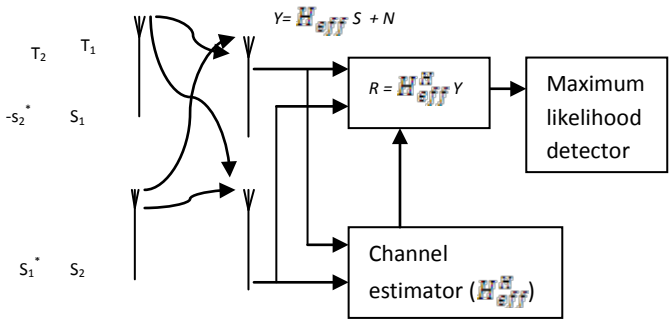


Figure.3 MIMO System Model Symbol Estimation

The received signals at time t_1 and $t_2 = t_1 + T$ is given by

$$y_1^{(1)} = h_{11}s_1 + h_{12}s_2 + n_1^{(1)} \quad (10)$$

$$y_2^{(1)} = h_{21}s_2 + h_{22}s_1 + n_2^{(1)} \quad (11)$$

$$y_1^{(2)} = h_{11}(-s_2^*) + h_{12}(s_1^*) + n_1^{(2)} \quad (12)$$

$$y_2^{(1)} = h_{21}(-s_2^*) + h_{22}(s_1^*) + n_2^{(2)} \quad (13)$$

Where T is the symbol duration, h_{ij} represents the channel impulse response between j^{th} transmission antenna and i^{th} receive antenna and n_1,n_2,n_3,n_4 are independent identically distributed Gaussian random variables representing noise with zero mean and variance σ^2.

Rearranging Eqn. (10)-(13) in matrix form,

$$\begin{bmatrix} y_1^{(1)} \\ y_2^{(1)} \\ y_1^{(2)*} \\ y_2^{(2)*} \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \\ h_{12}^* & -h_{11}^* \\ h_{22}^* & -h_{21}^* \end{bmatrix} \begin{bmatrix} s_1 \\ s_2 \end{bmatrix} + \begin{bmatrix} n_1^{(1)} \\ n_2^{(1)} \\ n_1^{(2)} \\ n_2^{(2)} \end{bmatrix} \quad (14)$$

H_{eff} is the channel from transmit antenna to receive antenna. The expression (14) can be simply represented as

$$\boldsymbol{Y} = \boldsymbol{H_{eff}}\,\boldsymbol{S} + \boldsymbol{N} \quad (15)$$

Assuming that the channel is perfectly estimated [7] at the receiver the decoder output is given by

$$\boldsymbol{R} = \boldsymbol{H_{eff}^{H}}\,\boldsymbol{Y} \quad (16)$$

This can be expanded as,

$$\begin{bmatrix} r_1 \\ r_2 \end{bmatrix} = \begin{bmatrix} h_{11}^* & h_{21}^* & h_{21} & h_{22} \\ h_{12}^* & h_{22}^* & -h_{11} & -h_{22} \end{bmatrix} \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \\ h_{12}^* & -h_{11}^* \\ h_{22}^* & -h_{21}^* \end{bmatrix} \begin{bmatrix} s_1 \\ s_2 \end{bmatrix} + \boldsymbol{H_{eff}^{H}}\boldsymbol{n} \quad (17)$$

The received signals r_1 and r_2 are determined by

$$r_1 = (|h_{11}|^2 + |h_{21}|^2 + |h_{12}|^2 + |h_{22}|^2)s_1 + w_1 \quad (18)$$

$$r_2 = (|h_{11}|^2 + |h_{21}|^2 + |h_{12}|^2 + |h_{22}|^2)s_2 + w_2 \quad (19)$$

Where $\begin{bmatrix} w_1 \\ w_2 \end{bmatrix} = \boldsymbol{H_{eff}^{H}}\boldsymbol{n}$

This can be interpreted as the following combination:

$$\hat{s}_1 = h^*_{11}y_{11} + h_{12}y^*_{12} + h^*_{21}y_{21} + h_{22}y^*_{22} \quad (20)$$

Likewise, the second symbol is estimated as:

$$\hat{s}_2 = h^*_{12}y_{11} + h_{11}y^*_{12} + h^*_{22}y_{21} + h_{21}y^*_{22} \quad \ldots\ldots\ldots (21)$$

5. Proposed Architecture

Combined architecture of transmitter for all three control channels is given in Figure 6. This is explained briefly in this section.

5.1 Transmitter architecture

Channel processing steps at transmitter side are done by using Figure 6. Initially, scrambling is performed by doing the Ex-Or operation between incoming bits and gold sequence bits. Gold sequence is generated by continuous Ex-Or operation of x_1 and x_2 sequences. The sequence x_1 is common to all channels while x_2 is an application specific sequence. This scrambled bit is given to the modulation module. Since PDCCH and PCFICH use QPSK modulation it takes two bits at a time and for PHICH, channel modulation occurs before scrambling stage. It uses BPSK modulation which takes either ACK/ NACK which is one bit at a time. Since it is considered to be an important channel for getting the acknowledgement for earlier information received it first uses the modulation with repetitive coding and then in scrambling module. For PHICH, in the scrambling module the gold sequence is generated using x_1 and x_2 and orthogonal sequence. Complex valued modulated bits are given to the layer mapping module. Since all the control channels able to support multi antennas, transmitter diversity is the control line for the layer mapping module. The antennas are selected according to the table IV when transmit diversity selected.

Table IV: Transmit diversity value to its type and port Nos.

Sl.No.	Transmit Diversity	Type	Port no. for Tx.	Port no. for Rx.
1.	000	(1 X 1) SISO	0	0
2.	010	(2 X 1)MISO	0,1	0
3.	011	(2 X 2)MIMO	0,1	0,1
4.	100	(4 X 1)MISO	0,1,2,3	0
5.	101	(4 X 2)MIMO	0,1,2,3	0,1

In precoding block, depending on antenna diversity the results are computed. If it is single antenna then the output of layer mapping is directly passed to the output. When two antennas are selected, data from to registers gets multiplied with $1/\sqrt{2}$ their real and imaginary parts are separated and their signs get changed accordingly and stored in registers as shown in the Figure 5. This sort of module is developed pertaining to the expression (9). Similarly for four antenna case the data for all the four antennas are precoded and the necessary zero padding is done pertaining to Eqn.(9).The layer mapping operation and precoding operation for two and four antennas had been shown in Figure 4. Finally, precoded data from all downlink channels are mapped to the single, two or four LTE grid structures. In order to set up a grid structure three counters viz column, row and slot are made. They are synchronized with the clock. As per the assumptions made in table 5, the channel bandwidth is 1.4 MHz the different slots for all the three control channels along with data channels and reference and unspecified signal slots are all studied [5].It should be noted that LTE grid structure varies with respect to different antennas and different bandwidth etc. A 10 ms radio frame has 20 slots and each slot is divided 14 rows with 72 columns each. To put up the architecture, a counter which counts from 0 to 71 for column is done then making the row to get incremented from 0 to 13, the slot number is incremented from 0 to 19.While the counter counts the respective channel outputs are brought out to the antenna. The resultant bits are used for channel estimation based on their row values.

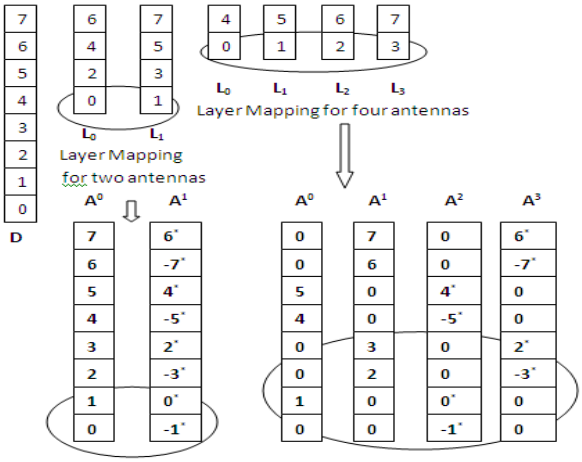


Figure 4: Layer mapping operation for 2 and 4 antennas

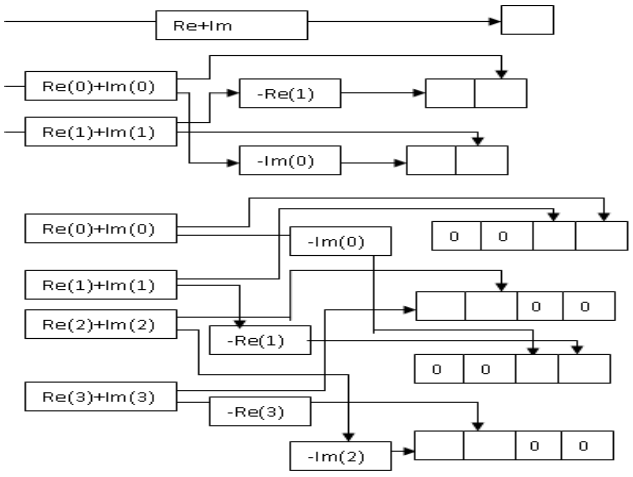


Figure 5:Precoding structure for single, two or four antennas

5.2 Receiver architecture

Realization of the receiver architecture is very important in communication hardware. It is because of the type of detection of information involved. Receiver architecture of all control channels is shown in Figure 7. In receiver side, channel de-estimation process is taken with same channel coefficients which are calculated by using 8-pt FFT used in channel estimation. Then all data are demapped from resource element grid by knowing the row, column and slot values. The information from all the antenna grid structure for all the control channels other than data channels are streamed to the respective registers from the grid structure. In decoding module, transmitter diversity and antenna selection are the control lines like precoding module. In the decoding module the depending on diversity the reverse operation of precoding is performed. Zero padding and redundant information are removed and concatenated. After decoding, the data have to be detected by demodulation method by selecting proper demodulation scheme which is used by transmitter. Data are detected by comparing the result of decoder with the predefined modulation values [2]. Value nearer to the optimal value is chosen in order to detect the original bits. So modulation selection is done through the control line for demodulation for multiplexer. These bits are concatenated to form a single layer in the delayer mapping module. Then descrambling is done by Ex-or operation by using the gold sequence generation to recover the original data. Since the information from channels PCFICH and PDCCH are demodulated by QPSK the scrambling part is modified for two bits at a time which involves parallel processing and the information is received from the receiver block.

6.Results and Discussions

Simulation and implementation were done by considering some assumptions among many LTE specifications. These assumptions are illustrated in Table V. The implementation of transmitter and receiver is done on the PlanAhead 13.2 Virtex-5, xc5vlx50tff1136-1 device.

The location for each input and output has to be assigned to this kit to perform implementation. In this device, output is viewed by LED pins. Clock signal can be given internally by assigning a specified pin pattern. The hardware description language HDL used is Verilog HDL. PlanAhead 13.2 is used to perform the Verilog HDL compilation and FPGA configurations.

Table V: Assumptions for developing the architecture

Parameter	Assumptions
Channel Bandwidth (MHz)	1.4
Number of Physical Resource Blocks (PRB)	6
Cyclic Prefix	Normal
Number of OFDM symbols per sub frame	14 (7 in each slot)
Frame Structure	Type I(FDD)
Transmit antenna port-, PCFICH,PDCCH,PHICH	1,2,4 antennas

6.1 Simulation Results

The simulation result of the transmitter of downlink for all control channels in SISO environment is shown in Figure 8 and simulation result for receiver for the same is shown in Figure 9. Clock, reset, transmitter diversity and modulation selection are the major inputs for the simulation. Transmitter can send the information if reset is disabled. If the variable 'reset' is enabled, all the channels are setting for their initial value again. In this case LTE grid structure starts from 0^{th} row, 0^{th} column and 0^{th} slot. According to the transmit diversity decided by upper layers (SISO,MISO or MIMO), respective antennas are selected in the physical layer. For example when the diversity is given as '000' the system undergoes SISO model. As in modulation, layers are mapped to single, two or four layers. If single layer is chosen, the output of modulation is directly mapped; otherwise buffers are required. These buffers are shown in Figure 6. Mapping to resource element grid also depends on transmit diversity variable. For SISO single antenna case is selected, (transmit_0) is enabled. Depending upon antenna selection, the channel estimation also varies. Demapping from resource elements, decoding, demodulation (detection), delayer mapping and descrambling results are shown in Figure 9. Process starts with the channel de-estimation process. Output of this module is passed to the grid structure. Again based on row, column and slot counters, the data which are mapped to the grid at the transmitter side are retrieved at its corresponding location. Then decoding and detection process is carried over based on transmit diversity for all antenna possibilities. Demodulation is performed by the decision-taking module in such a way that the incoming bits from the decoder have to be compared with the predefined modulation schemes value. The value nearer to the appropriate value is considered as the detected value (2 bits, 4 bits or 6 bits) by the receiver and delayer mapped to the single layer by concatenation method. Then the delayer mapped data are given to the descrambler module. Finally data become intelligible for the user

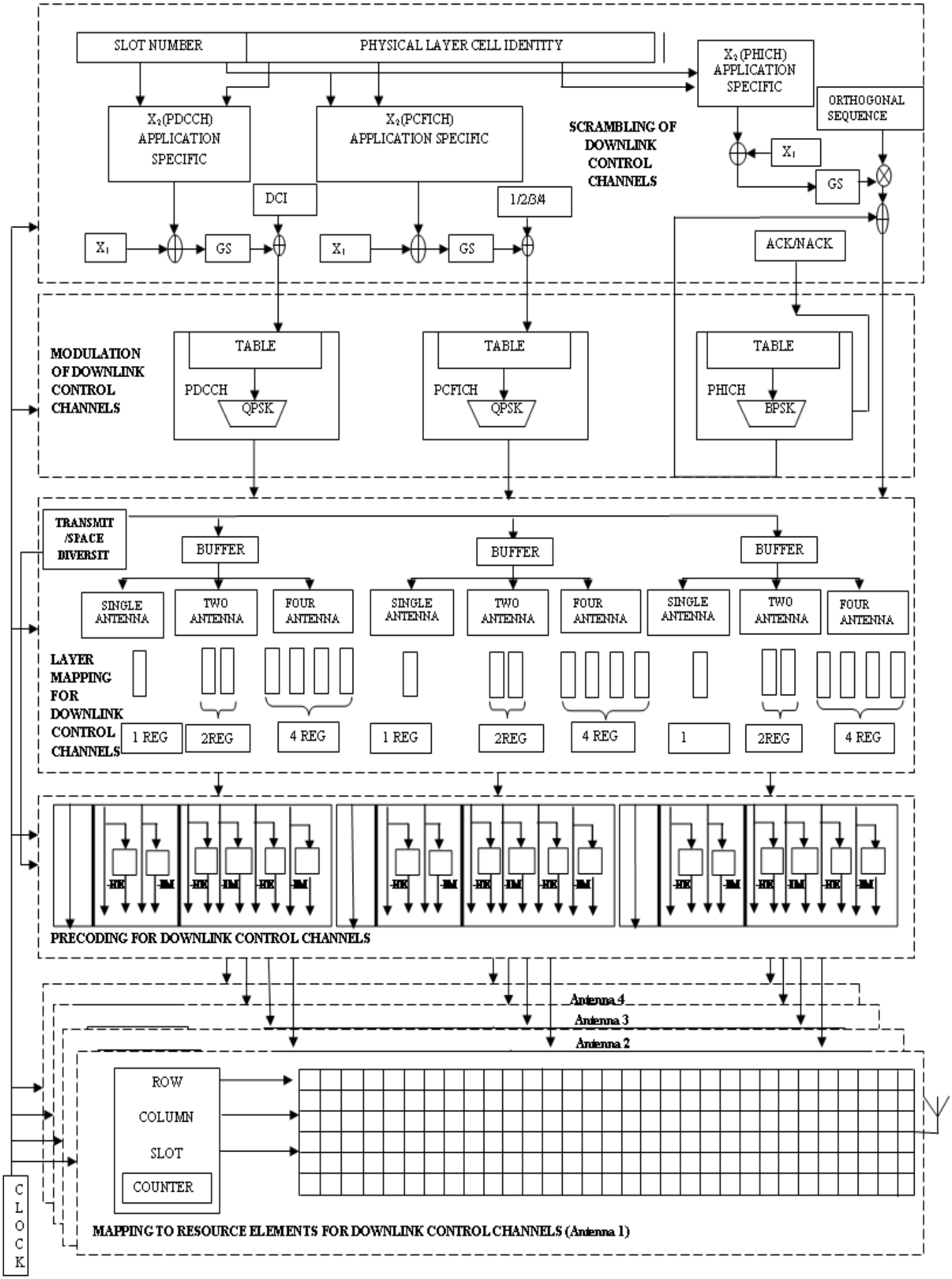


Figure 6: Transmitter architecture for all the control channels

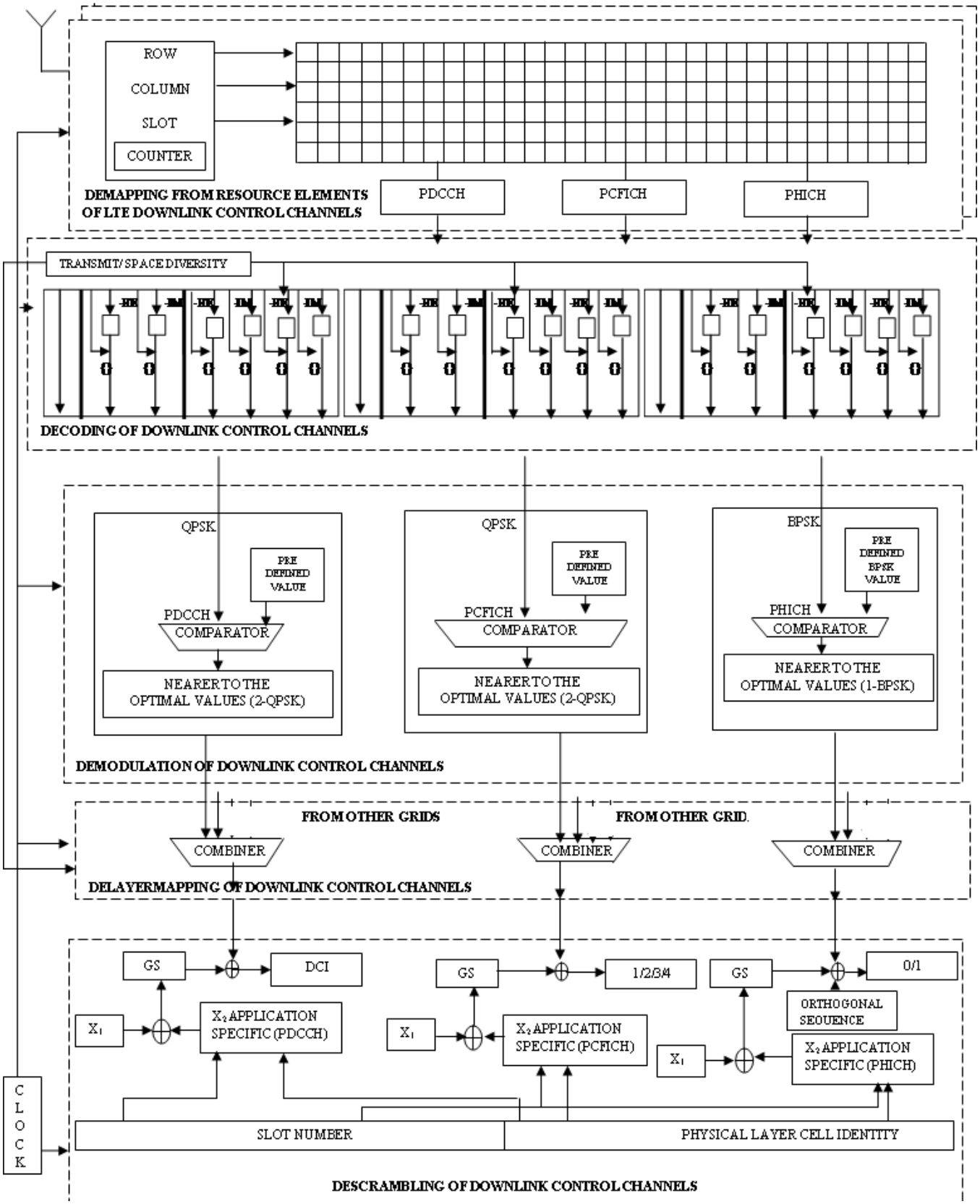


Figure 7: Receiver architecture for all the control channels

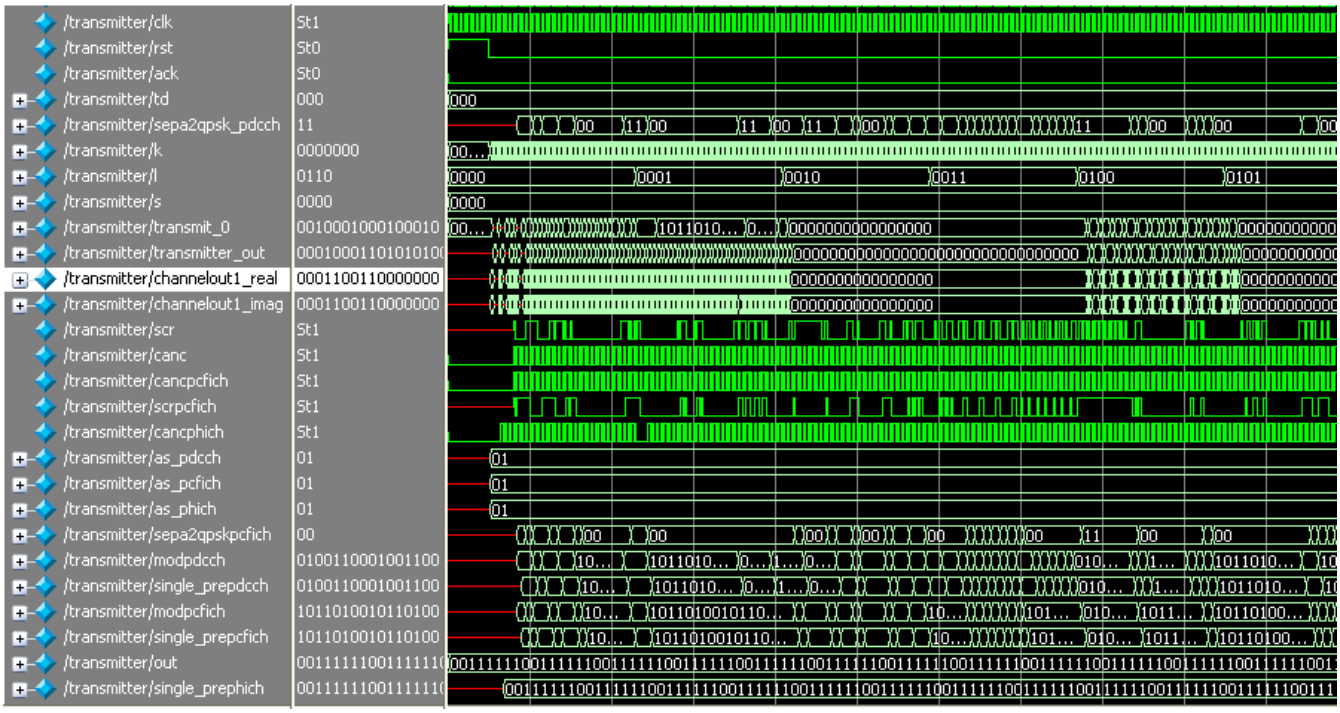


Figure 8: Simulated output for total module of transmitter under SISO environment.

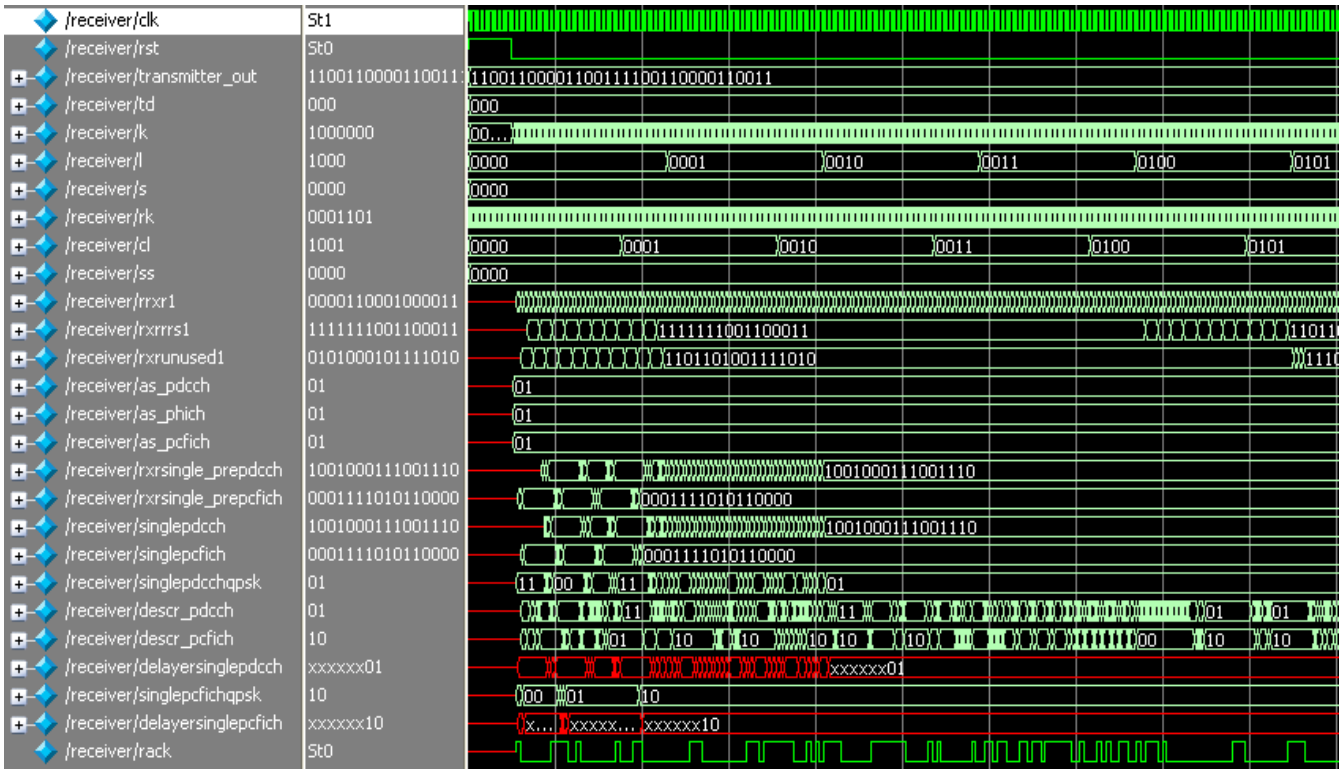


Figure 9: Simulated output for total module of Receiver under SISO environment.

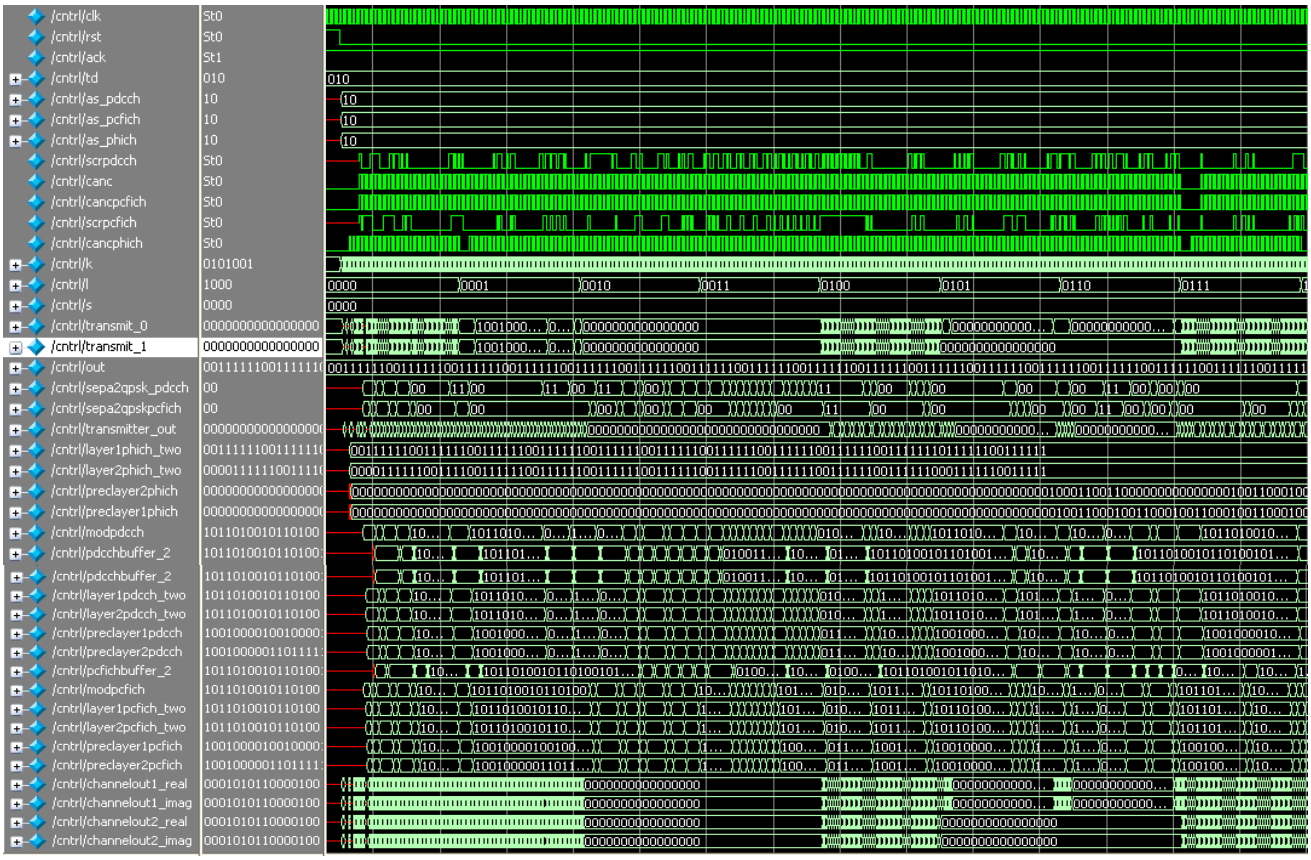


Figure 10: Simulated output for total module of transmitter under MISO (2 X1) environment.

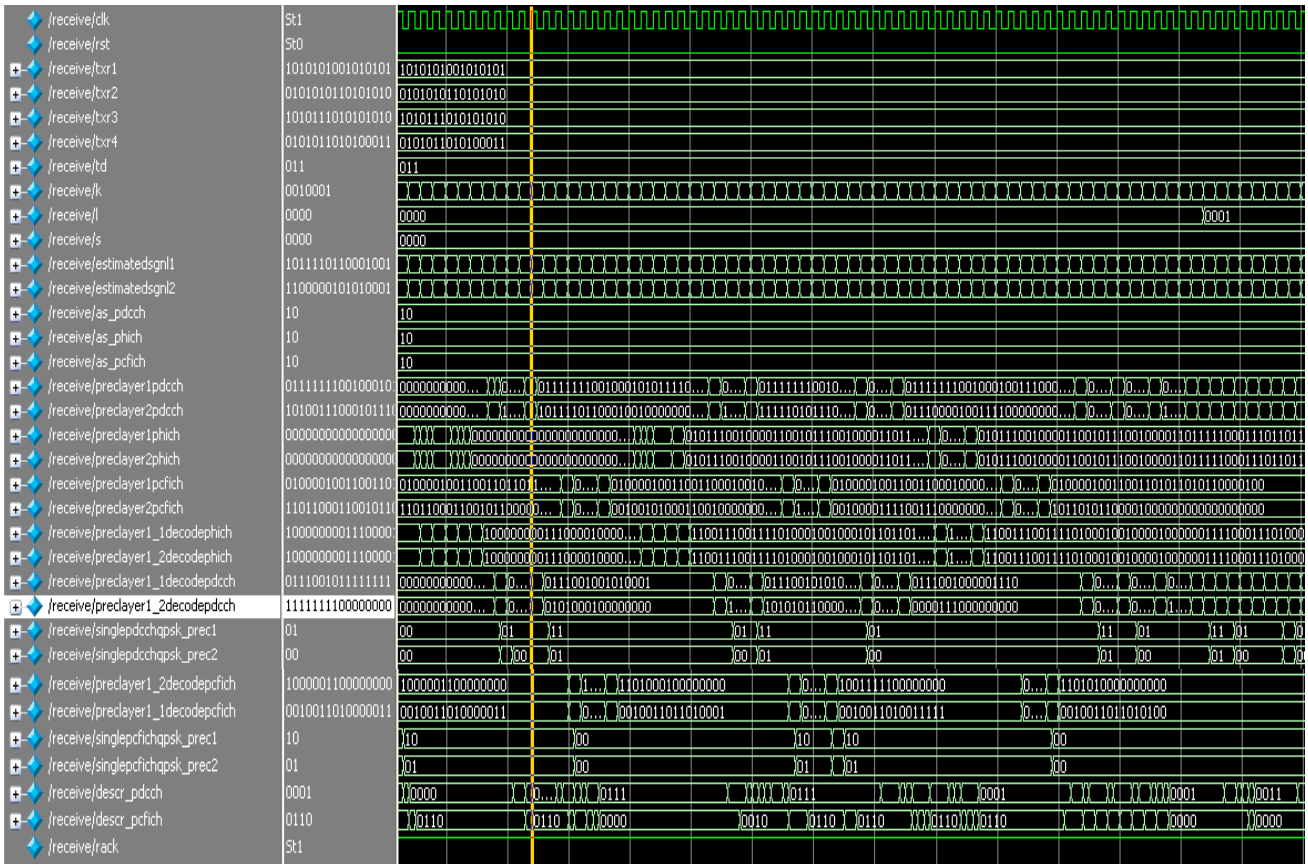


Figure 11: Simulated output for total module of receiver under MIMO (2 X 2) environment.

The simulation results for the same architecture under MISO(2X1)and MIMO(2X2) environment are shown in Figure 10 and Figure 11.The variable 'clk' is the clock of duration 10ms, 'rst' is the variable used to reset all the registers. The variable 'td' is the transmitter diversity variable used to select the antennas. For the MIMO (2 X2) it has value 011, the antenna selection variables for the three control channels 'as_pdcch', 'as_pcfich', 'as_phich' will be assigned "10" indicating 2 antenna case. Variable 'ack' is the input for the PHICH channel and is assigned 1. Variable 'canc', 'cancpcfich', 'cancphich' are the clock generated according to the LTE specifications. The variables 'k','l','s' are used to increment the rows, columns and slots. The 'transmit_0' and 'transmit_1' are the two transmit antenna outputs. Variables 'scrpdcch', scrpcfich' are scrambled outputs at for the two channels pdcch and pcfich. The variable 'out' is the output of channel PHICH after BPSK modulation and scrambling. Since single bit scrambling has been done for the channels a buffer is used before modulation to generate two bit input for the modulation for the channels PDCCH and PCFICH. Variable 'sepa2qpsk_pdcch' is the buffer output for the channel PDCCH. The modulation output for the channel PDCCH is 'modpdcch' similarly for PCFICH 'modpcfich'. A buffer is used to store the modulation symbols before layer mapping. The buffer is indicated by pdcchbuffer_2. Similarly for the other channels there are buffers. Thus the hardware works in pipelined approach.The variables layer1 and layer2 are the layermapped outputs with the corresponding suffixes. Variables 'preclayer1pdcch' and 'preclayer2pdcch' are the precoded outputs for the control channel PDCCH. Variables 'channelout1_real', 'channelout1_imag', 'channelout2_real', 'channelout2_imag' are the outputs after the channel coefficient multiplication. For the 2x2 MIMO receiver the four received signals are given by 'txr1', 'txr2'. The estimated signals are given by 'estimatedsgnl1', 'estimatedsgnl2'. The variables 'preclayer1pdcch', 'preclayer2pdcch' are outputs of the two demapping modules for the channel PDCCH. The demapped values for the other two channels are indicated by the same variable with corresponding suffixes. Variables 'preclayer1_1 decodepdcch' and 'preclayer1_2decodepdcch' are the variables of the decoding module. The variables 'singlepdcchqpsk_prec1' , 'singlepdcchqpsk_prec2' are detected values of the channel PDCCH. Finally the descrambled control information for the channels PDCCH, PCFICH, PHICH are given by 'descr_pdcch', 'descr_pcfich' and 'rack'.

6.2 Implementation Results

Simulated program is implemented on PlanAhead 13.2 Virtex-5, xc5vlx50tff1136-1 board. This board is useful to estimate the RTL design, power estimation and resource utilization and FPGA editor.

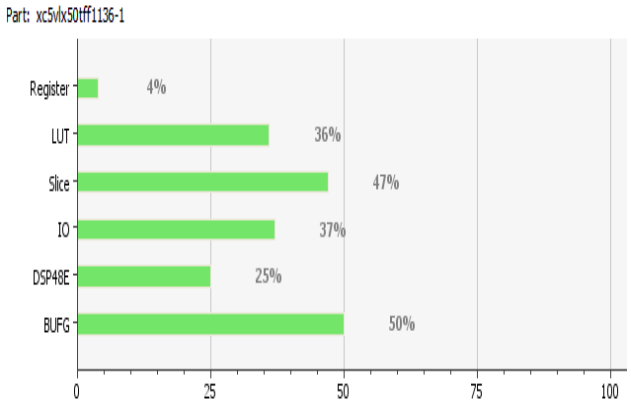


Figure 12:Resource estimation of downlink Transmitter with 4 antennas

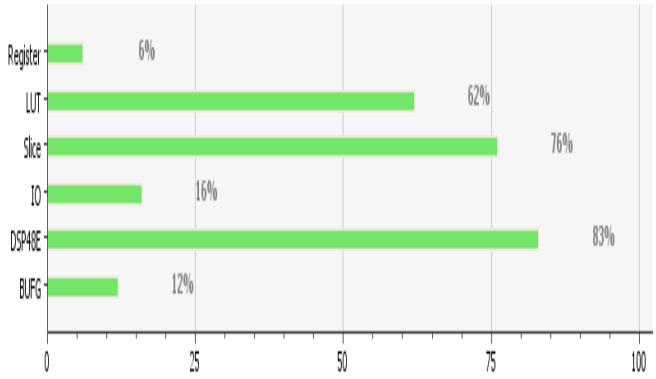


Figure 13:Resource estimation of downlink Receiver with 2 antennas

6.2.1 Resource estimation

Resource utilization of all channels for transmitter and receiver are shown in Figure 12 and 13. These graphs include the devices like registers, LUT (Look-Up Tables) and I/O. The consumption of LUTs, Slices and DSP Arithmetic are more in receiver due to calculation predefined values.

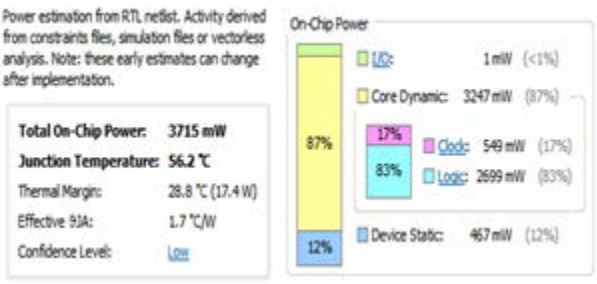


Figure 14: *Power estimation of downlink Transmitter for 4 antennas*

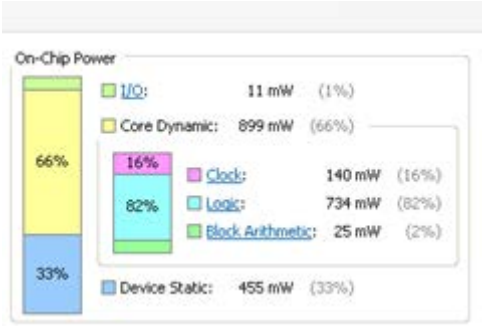
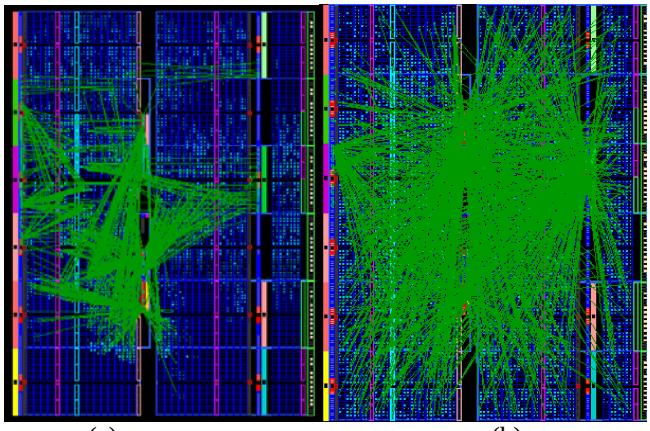


Figure 15: *Power estimation of downlink Receiver*

6.2.2 Power estimation

PlanAhead tool is also used to estimate the needed power for I/O devices, clock signals and logic signals. Figure 14 and Figure 15 show the power estimation for downlink of all channels transmitter and receiver. In transmitter, nearly 3247mW of power is consumed by dynamic core and 427 mW by device static and 1 mW by I/O. In the receiver module nearly 899mW of power is consumed by dynamic core and 455 mW by device static and 11 mW by I/O.



(a) (b)

Figure 16: FPGA editor of (a)Transmitter and (b)Receiver

6.2.3 FPGA editor

Routing between input and output in terms of connection is shown by FPGA editor. Figure 16 (a) and (b) illustrate the FPGA editor of all channels transmitter and receiver. These Figures give an idea of how the various components are placed, mapped and routed inside the Virtex-5 device. This done by using PlanAhead 13.4 tool from Xilinx..

6.2.4 RTL design

RTL design of downlink channel transmitter is shown in Figure 17 for four antennas and receiver with two antennas are shown in, Figure 18. It shows all the modules of the transmitter and receiver. By clicking on the particular module the utilized resources are clearly viewed by the designer.

7. CONCLUSION

In this paper, an optimized architecture for downlink for all control channels with transmitter and receiver which include scrambling, modulation, layer mapping, precoding and mapping to resource elements and demapping from resource elements, decoding, delayer mapping, demodulation and descrambling is done and implemented in Virtex -5 chip using PlanAhead13.4 tool. The summary of power estimation and resource estimation is discussed with RTL schematic. Power and resource utilization can be further reduced by using VLSI DSP techniques.

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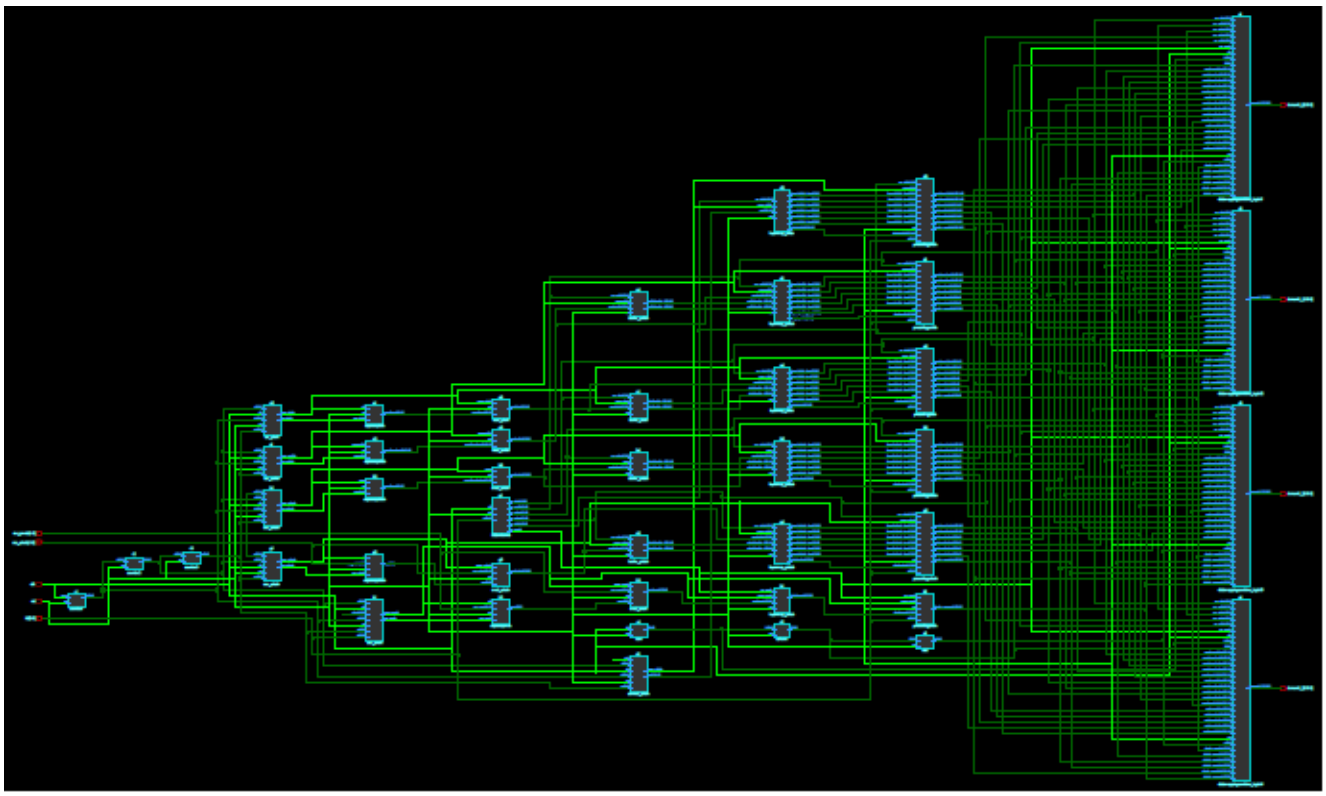

Figure 17. RTL design of downlink Transmitter for 4 antennas

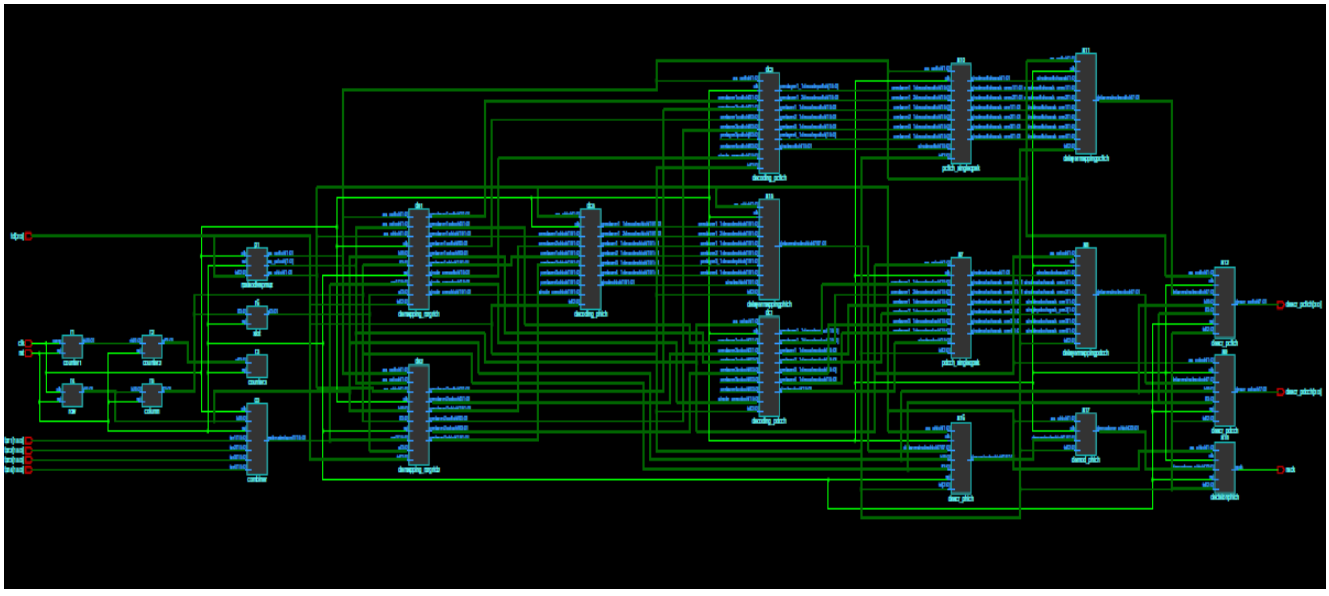

Figure 18. RTL design of downlink Receiver with 2 antennas